LTC1771

Low Quiescent Current High Efficiency Step-Down DC/DC Controller

February 2000

FEATURES

- **Very Low Standby Current: 10μA**
- **Available in Space-Saving 8-Lead MSOP Package**
- **High Output Currents**
- **Wide V_{IN} Range: 2.8V to 20V Operation**
- V_{OUT} Range: 1.23V to 18V
- High Efficiency: Over 93% Possible
- ±2% Output Accuracy
- Very Low Dropout Operation: 100% Duty Cycle
- Current Mode Operation for Excellent Line and Load Transient Response
- Defeatable Burst Mode™ Operation
- Short-Circuit Protected
- Optional Programmable Soft-Start
- Micropower Shutdown: I_Q = 2μA

APPLICATIONS

- Cellular Telephones and Wireless Modems
- 1- to 4-Cell Lithium-Ion-Powered Applications
- Portable Instruments
- Battery-Powered Equipment
- Battery Chargers
- Scanners

DESCRIPTION

The LTC®1771 is a high efficiency current mode step-down DC/DC controller that draws as little as 10μA DC supply current to regulate the output at no load while maintaining high efficiency for loads up to several amps.

The LTC1771 drives an external P-channel power MOSFET using a current mode, constant off-time architecture. An external sense resistor is used to program the operating current level. Current mode control provides short-circuit protection, excellent transient response and controlled start-up behavior. Burst Mode operation enables the LTC1771 to maintain high efficiency down to extremely low currents. Shutdown mode further reduces the supply current to a mere 2μA. For low noise applications, Burst Mode operation can be easily disabled with the MODE pin.

Wide input supply range of 2.8V to 18V (20V maximum) and 100% duty cycle operation for low dropout make the LTC1771 ideal for a wide variety of battery-powered applications where maximizing battery life is important.

The LTC1771's availability in both 8-lead MSOP and SO packages provides for a minimum area solution.

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Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

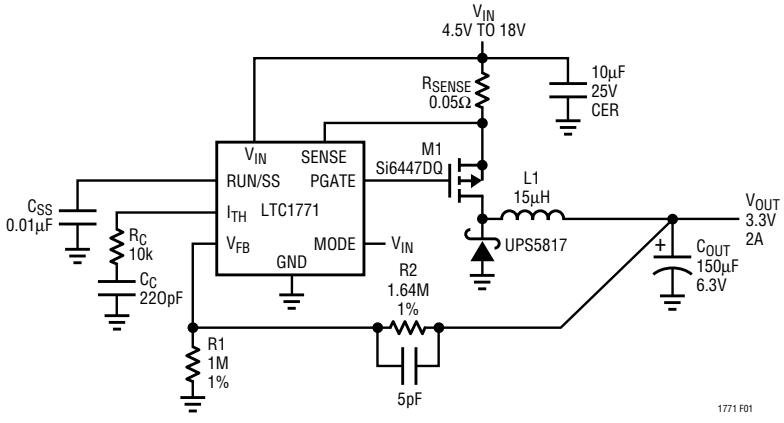
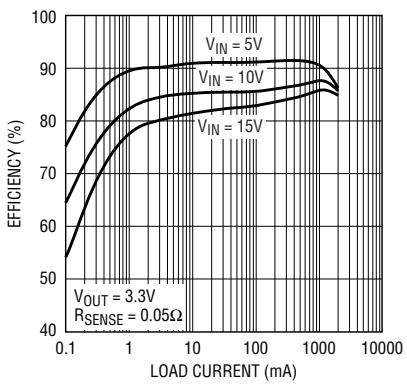


Figure 1. High Efficiency Step-Down Converter

LTC1771 Efficiency

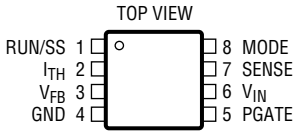


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ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 20V
Peak Driver Output Current < 10µs (PGATE) 1A
RUN/SS Voltage ..... –0.3V to (V_{IN} + 0.3V)
MODE Voltage ..... –0.3V to 20V
I_{TH}, V_{FB} Voltage ..... –0.3V to 5V
SENSE Voltage (V_{IN} > 12V) ... (V_{IN} – 12V) to (V_{IN} + 0.3V)
SENSE Voltage (V_{IN} ≤ 12V) ..... –0.3V to (V_{IN} + 0.3V)
Junction Temperature (Note 2) ..... 125°C
Operating Temperature Range (Note 3)
LTC1771E ..... –40°C to 85°C
LTC1771I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

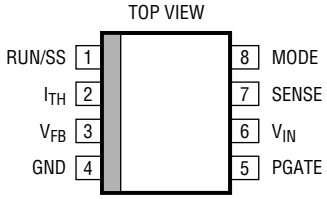
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1771EMS8
MS8 PART MARKING
LTKD



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1771ES8 LTC1771IS8
S8 PART MARKING
1771 1771I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 10V, V_{RUN} = open unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage	(Note 5)	●	1.205	1.230	1.255	V
I_{FB}	Feedback Current	(Note 5)	●		1	10	nA
I_{SUPPLY}	No-Load Supply Current	V_{IN} = 10V, I_{LOAD} = 0 (Note 6)			10		µA
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation	V_{IN} = 5V to 15V (Note 5)	●		0.003	0.03	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	I_{TH} = 0.5V to 2V, Burst Disabled (Note 5)	●		0.25	1	%
I_Q	Input DC Supply Current Active Mode (PGATE = 0V) Sleep Mode (Note 6) Shutdown Short Circuit	(Note 4) V_{IN} = 2.8V to 18V V_{IN} = 2.8V to 18V, V_{FB} = 1.5V V_{IN} = 2.8V to 18V, V_{RUN} = 0V V_{IN} = 2.8V to 18V, V_{FB} = 0V			 150 9 2 175	 235 15 6 275	 µA µA µA µA
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = V_{REF} – 20mV	●	110	140	180	mV
$\Delta V_{SENSE(MIN)}$	Minimum Current Sense Threshold	V_{FB} = V_{REF} + 10mV, Burst Disabled			–25		mV
$\Delta V_{SENSE(SLEEP)}$	Sleep Current Sense Threshold	I_{TH} = 1V			50		mV
t_{OFF}	Switch Off Time	V_{FB} at Regulated Value V_{FB} = 0V			3.5 70		µs µs
V_{MODE}	Mode Pin Threshold	V_{MODE} Rising	●	0.5	1.3	2	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 10V, V_{RUN} = open unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{RUN/SS}$	RUN/SS Pin Threshold	$V_{RUN/SS}$ Rising	●	0.5	1.0	2	V
I_{RUN}	Source Current	V_{RUN} = 0V, V_{IN} = 2.8V to 18V		0.3	1	3	µA
PGATE t_r, t_f	PGATE Transition Time (Note 7)						
	Rise Time	C_{LOAD} = 2000pF			80		ns
	Fall Time	C_{LOAD} = 2000pF			90		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1771S8: $T_J = T_A + (P_D)(110°C/W)$

LTC1771MS8: $T_J = T_A + (P_D)(150°C/W)$

Note 3: The LTC1771E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC1771I is guaranteed and tested over the –40°C to 85°C operating temperature range.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: The LTC1771 is tested in a feedback loop that servos V_{FB} to the balance point for the error amplifier (V_{ITH} = 1.23V).

Note 6: No-load supply current consists of sleep mode current (9µA typical) plus a small switching component necessary to overcome Schottky diode leakage and feedback resistor current.

Note 7: t_r and t_f measured at 10% to 90% levels.

PIN FUNCTIONS

RUN/SS (Pin 1): The voltage level on this pin controls shutdown/run mode (ground = shutdown, open/high = run). Connecting an external capacitor to this pin provides soft-start.

I_{TH} (Pin 2): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 3V.

V_{FB} (Pin 3): Feedback of Output Voltage for Comparison to Internal 1.23V Reference. An external resistive divider across the output is returned to this pin.

GND (Pin 4): Ground Pin.

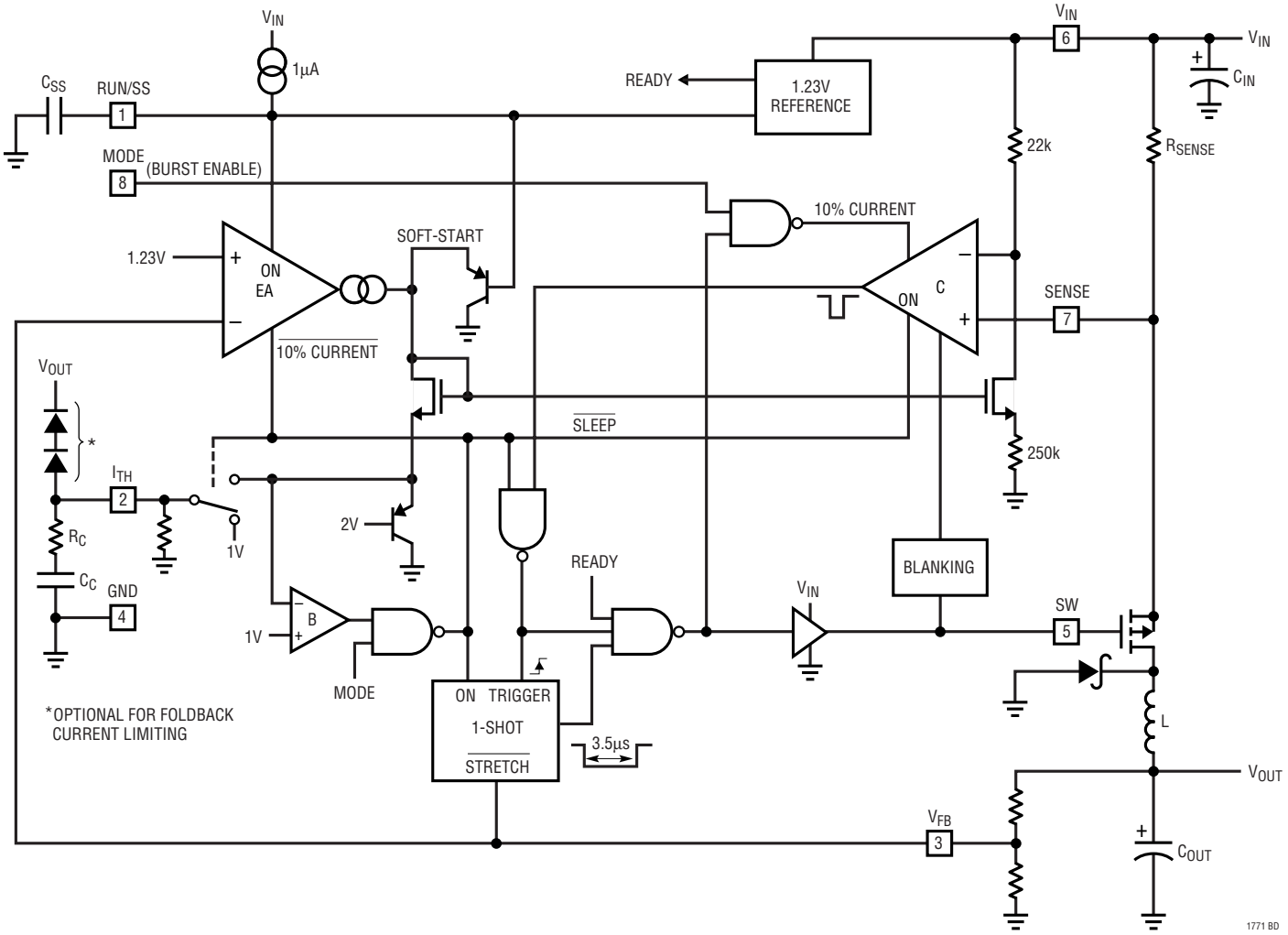
PGATE (Pin 5): High Current Gate Driver for External P-Channel MOSFET Switch. Voltage swing is from ground to V_{IN}.

V_{IN} (Pin 6): Main Input Voltage Supply Pin.

SENSE (Pin 7): Current Sense Input for Monitoring Switch Current. Maximum switch current and Burst Mode threshold is programmed with an external resistor between SENSE and V_{IN}.

MODE (Pin 8): Burst Mode Enable/Disable Pin. Connecting this pin to V_{IN} (or above 2V) enables Burst Mode operation, while connecting this pin to ground disables Burst Mode operation. Do not leave floating.

FUNCTIONAL BLOCK DIAGRAM



OPERATION (Refer to Functional Block Diagram)

Main Control Loop

The LTC1771 uses a constant off-time, current mode step-down architecture. During normal operation, the P-channel MOSFET is turned on at the beginning of each cycle and turned off when the current comparator C triggers the 1-shot timer. The external MOSFET switch stays off for the 3.5µs 1-shot duration and then turns back on again to begin a new cycle. The peak inductor current at which C triggers the 1-shot is controlled by the voltage on Pin 3 (I_{TH}), the output of the error amplifier EA. An external resistive divider connected between V_{OUT} and ground allows EA to receive an output feedback voltage V_{FB}. When the load current increases, it causes a slight decrease in V_{FB} relative to the 1.23V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current.

The main control loop is shut down by pulling Pin 1 (RUN/SS) low. Releasing RUN/SS allows an internal 1µA current source to charge soft-start capacitor C_{SS}. When C_{SS} reaches 1V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 40% of its maximum value. As C_{SS} continues to charge, I_{TH} is gradually released allowing normal operation to resume.

Burst Mode Operation

The LTC1771 provides outstanding low current efficiency and ultralow no-load supply current by using Burst Mode operation when the MODE pin is pulled above 2V. During Burst Mode operation, short burst cycles of normal switching are followed by a longer idle period with the switch off and the load current is supplied by the output capacitor. During this idle period, only the minimum required circuitry—1.23V reference and error amp—are left on, and the supply current is reduced to 9µA. At no load, the output capacitor is still discharged very slowly by leakage current in the Schottky diode and feedback resistor current resulting in very low frequency burst cycles that add a few more microamps to the supply current.

Burst Mode operation is provided by clamping the minimum I_{TH} voltage at 1V which represents about 25% of maximum load current. If the load falls below this level, i.e. the I_{TH} voltage tries to fall below 1V, the burst comparator B switches state signaling the LTC1771 to enter sleep mode. During this time, EA is reduced to 10% of its normal operating current and the external compensation capacitor is disconnected and clamped to 1V so that the EA can drive its output with the lower available current. As the load discharges the output capacitor, the internal I_{TH} voltage increases. When it exceeds 1V the burst comparator exits sleep mode, reconnects the external compensation components to the error amplifier output, and returns EA to full power along with the other necessary circuitry. This scheme (patent pending) allows the EA to be reduced to such a low operating current during sleep mode without adding unacceptable delay to wake up the LTC1771 due to the compensation capacitor on I_{TH} required for stability in normal operation.

Burst Mode operation can be disabled by pulling the MODE pin to ground. In this mode of operation, the burst comparator B is disabled and the I_{TH} voltage allowed to go all the way to 0V. The load can now be reduced to about 1% of maximum load before the loop skips cycles to maintain regulation. This mode provides a low noise output spectrum, useful for reducing both audio and RF interference, at the expense of reduced efficiency at light loads.

Off-Time

The off-time duration is 3.5µs when the feedback voltage is close to the reference voltage; however, as the feedback voltage drops, the off-time lengthens and reaches a maximum value of about 70µs when V_{FB} is zero. This ensures that the inductor current has enough time to decay when the reverse voltage across the inductor is low such as during short circuit, thus protecting the MOSFET and inductor.

APPLICATIONS INFORMATION

The basic LTC1771 application circuit is shown in Figure 1 on the first page. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, L can be chosen. Next, the MOSFET and D1 are selected. The inductor is chosen based largely on the desired amount of ripple current and for Burst Mode operation. Finally C_{IN} is selected for its ability to handle the required RMS input current and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specifications.

R_{SENSE} Selection

R_{SENSE} is chosen based on the required output current. The LTC1771 current comparator has a maximum threshold of 140mV/R_{SENSE}. The current comparator threshold sets the peak inductor current, yielding a maximum average output current I_{MAX} equal to the peak less half the peak-to-peak ripple current ΔI_L. For best performance when Burst Mode operation is enabled, choose ΔI_L equal to 35% of peak current. Allowing a margin for variations in the LTC1771 and external components gives the following equation for choosing R_{SENSE}:

$$R_{SENSE} = 100mV/I_{MAX}$$

At higher supply voltages, the peak currents may be slightly higher due to overshoot from current comparator delay and can be predicted from the second term in the following equation:

$$I_{PEAK} \cong \frac{0.14}{R_{SENSE}} + 0.5\left(\frac{V_{IN} - V_{OUT}}{L(\mu H)}\right)^{1/2}$$

Inductor Value Selection

Once R_{SENSE} is known, the inductor value can be determined. The inductance value has a direct effect on ripple current. The ripple current decreases with higher inductance and increases with higher V_{OUT}. The ripple current during continuous mode operation is set by the off-time and inductance to be:

$$\Delta I_{L(CONT)} = t_{OFF}\left(\frac{V_{OUT} + V_D}{L}\right)$$

where t_{OFF} = 3.5µs. However, the ripple current at low loads during Burst Mode operation is:

$$\Delta I_{L(BURST)} \approx 35\% \text{ of } I_{PEAK} \approx 0.05/R_{SENSE}$$

For best efficiency when Burst Mode operation is enabled, choose:

$$\Delta I_{L(CONT)} \leq \Delta I_{L(BURST)}$$

so that the inductor current is continuous during the burst periods. This sets a minimum inductor value of:

$$L_{MIN} = (70\mu H)(V_{OUT} + V_D)(R_{SENSE})$$

When burst is disabled, ripple currents less than $\Delta I_{L(BURST)}$ can be achieved by choosing $L > L_{MIN}$. Lower ripple current reduces output voltage ripple and core losses, but too low of ripple current will adversely effect efficiency.

Inductor Core Selection

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mµ® cores. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent increase in voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mµ. Toroids are space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available that do not increase the height significantly.

Kool Mµ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

Power MOSFET Selection

An external P-channel power MOSFET must be selected for use with the LTC1771. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$ and the "on" resistance $R_{DS(ON)}$, reverse transfer capacitance and total gate charge.

Since the LTC1771 can operate down to input voltages as low as 2.8V, a sublogic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC1771 is less than the absolute maximum V_{GS} rating (typically 12V), as the MOSFET gate will see the full supply voltage.

The required $R_{DS(ON)}$ of the MOSFET is governed by its allowable power dissipation. For applications that may operate the LTC1771 in dropout, i.e. 100% duty cycle, at its worst case the required $R_{DS(ON)}$ is given by:

$$R_{DS(ON)} = \frac{P_P}{\left(I_{OUT(MAX)}\right)^2\left(1+\delta_P\right)}$$

where P_P is the allowable power dissipation and δ_P is the temperature dependency of $R_{DS(ON)}$. $(1 + \delta_P)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but = 0.005/°C can be used as an approximation for low voltage MOSFETs.

In applications where the maximum duty cycle is less than 100% and the LTC1771 is in continuous mode, the $R_{DS(ON)}$ is governed by:

$$R_{DS(ON)} = \frac{P_P}{\left(DC\right)I_{OUT}{}^2\left(1+\delta_P\right)}$$

$$DC = \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

where DC is the maximum operating duty cycle of the LTC1771.

Catch Diode Selection

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Under this condition, the diode must safely handle I_{PEAK} at close to 100% duty cycle.

To maximize both low and high current efficiencies, a fast switching diode with low forward drop and low reverse leakage should be used. Low reverse leakage current is critical to maximize low current efficiency since the leakage can potentially exceed the magnitude of the LTC1771 supply current. Low forward drop is critical for high current efficiency since loss is proportional to forward drop. The effect of reverse leakage and forward drop on no- load supply current and efficiency for various Schottky diodes is shown in Table 1. As can be seen, these are conflicting parameters and the user must weigh the importance of each spec in choosing the best diode for the application.

Table 1. Effect of Catch Diode on Performance

DIODE	LEAKAGE (V_R = 3.3V)	V_F @ 1A	NO-LOAD SUPPLY CURRENT	EFFICIENCY AT 10V/1A
MBR0540	0.25µA	0.50V	10.4µA	86.3%
UPS5817	2.8µA	0.41V	11.8µA	88.2%
MBR0520	3.7µA	0.36V	12.2µA	88.4%
MBRS120T3	4.4µA	0.43V	12.2µA	87.9%
MBRM120LT3	8.3µA	0.32V	14.0µA	89.4%
MBRS320	19.7µA	0.29V	20.0µA	89.8%

C_{IN} and C_{OUT} Selection

At higher load currents, when the inductor current is continuous, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} = \frac{I_{MAX}\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's

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ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Do not underspecify this component. An additional 0.1μF ceramic capacitor is also helpful on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) in continuous mode is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. For output ripple less than 100mV, assure C_{OUT} required ESR is $<2R_{SENSE}$.

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The I_{TH} pin OPTI-LOOP™ compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size of any aluminum electrolytic at a somewhat higher price. Typically once the ESR requirement is satisfied, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytics and dry tantalum capacitors are both available in surface mount configurations. In case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS, AVX TPSV and KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Sanyo POSCAP, Nichicon PL series and Panasonic SP.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 +L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in the LTC1771 circuits: the LTC1771 DC bias current, MOSFET gate charge current, I^2R losses and catch diode losses.

1. The DC bias current is 9μA at no load and increases proportionally with load up to a constant 150μA during continuous mode. This bias current is so small that this loss is negligible at loads above a milliamp but at no load accounts for nearly all of the loss.
2. The MOSFET gate charge current results from switching the gate capacitance of the power MOSFET switch. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} which is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = fQ_P$ where Q_P is the gate charge of the internal switch. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
3. I^2R losses are predicted from the internal switch, inductor and current sense resistor. In continuous mode the average output current flows through L but is "chopped"

OPTI-LOOP is a trademark of Linear Technology Corporation.

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between the P-channel MOSFET in series with R_{SENSE} and the output diode. The MOSFET $R_{DS(ON)}$ plus R_{SENSE} multiplied by the duty cycle can be summed with the resistance of L to obtain I^2R losses.

4. The catch diode loss is proportional to the forward drop as the diode conducts current during the off-time and is more pronounced at high supply voltages where the off-time is long. However, as discussed in the Catch Diode section, diodes with lower forward drops often have higher leakage currents, so although efficiency is improved, the no-load supply current will increase. The diode loss is calculated by multiplying the forward voltage drop times the diode duty cycle multiplied by the load current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, and inductor core losses, generally account for less than 2% total additional loss.

Output Voltage Programming

The output voltage is programmed with an external divider from V_{OUT} to V_{FB} (Pin 1) as shown in Figure 2. The regulated voltage is determined by:

$$V_{OUT} = 1.23\left(1+\frac{R2}{R1}\right)$$

To minimize no-load supply current, resistor values in the megohm range should be used. The increase in supply current due to the feedback resistors can be calculated from:

$$\Delta I_{VIN} = \frac{V_{OUT}}{R1+R2}\left(\frac{V_{OUT}}{V_{IN}}\right)$$

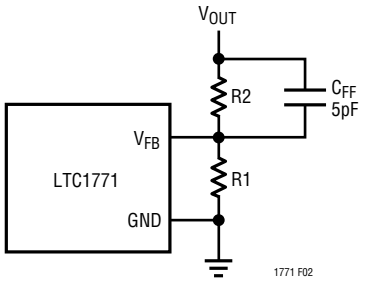


Figure 2. LTC1771 Adjustable Configuaration

A 5pF feedforward capacitor across R2 is recommended to minimize output voltage ripple in Burst Mode operation.

Run/Soft-Start Function

The RUN/SS pin is a dual purpose pin that provides the soft- start function and a means to shut down the LTC1771. Soft-start reduces the input surge current from V_{IN} by gradually increasing the internal current limit. Power supply sequencing can also be accomplished using this pin.

An internal 1μA current source charges up an external capacitor C_{SS}. When the voltage on the RUN/SS reaches 1V, the LTC1771 begins operating. As the voltage on the RUN/SS continues to ramp from 1V to 2.2V, the internal current limit is also ramped at a proportional linear rate. The current limits begins near 40% maximum load at $V_{RUN/SS}$ = 1V and ends at maximum load at $V_{RUN/SS}$ = 2.2V. The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If the RUN/SS has been pulled all the way to ground, there will be a delay before the current limit starts increasing and is given by:

$$t_{DELAY} \approx C_{SS}/I_{CHG}$$

where $I_{CHG} \cong 1\mu A$. Pulling the RUN/SS pin below 0.5V puts the LTC1771 into a low quiescent current shutdown ($I_Q < 2\mu A$).

Foldback Current Limiting

As described in the Catch Diode Selection, the worst-case dissipation for diode occurs with a short-circuit output, when the diode conducts the current limit value almost continuously. In most applications this will not cause excessive heating, even for extended fault intervals. However, when heat sinking is at a premium or higher forward voltage drop diodes are being used, foldback current limiting should be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding two diodes in series between the output and the I_{TH} pin as shown in the Functional Diagram. In a hard short (V_{OUT} = 0V) the current will be reduced to approximately 25% of the maximum output current.

APPLICATIONS INFORMATION

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest amount of time that the LTC1771 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and the amount of gate charge required to turn on the P-channel MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON} = t_{OFF}\left(\frac{V_{OUT} + V_D}{V_{IN} - V_{OUT}}\right) > t_{ON(MIN)}$$

where t_{OFF} = 3.5µs and $t_{ON(MIN)}$ is generally about 0.5µs for the LTC1771.

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC1771 will remain in Burst Mode operation even at high load currents. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

Mode Pin

Burst Mode operation is disabled by pulling MODE (Pin 8) below 0.5V. Disabling Burst Mode operation provides a low noise output spectrum, useful for reducing both audio and RF interference. It does this by keeping the frequency constant (for fixed V_{IN}) down to much lower load current (1% to 2% of I_{MAX}) and reducing the amount of output voltage and current ripple at light loads. When Burst Mode operation is disabled, efficiency is reduced at light loads and no load supply current increases to 175µA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1771. These items are also illustrated graphically in the layout diagram of Figure 3. Check the following in your layout:

1. Is the Schottky diode *closely* connected to the drain of the external MOSFET and the input cap ground?
2. Is the 0.1µF input decoupling capacitor *closely* connected between V_{IN} (Pin 6) and ground (Pin 4)? This capacitor carries the high frequency peak currents.
3. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground. Locate the feedback resistors right next to the LTC1771. The V_{FB} line should not be routed close to any nodes with high slew rates.
4. Is the 1000pF decoupling capacitor for the current sense resistor connected as close as possible to Pins 6 and 7? Ensure accurate current sensing with Kelvin connections to the sense resistor.
5. Is the (+) plate of C_{IN} *closely* connected to the sense resistor ? This capacitor provides the AC current to the MOSFET.
6. Are the signal and power grounds segregated? The signal ground consists of the (–) plate of C_{OUT}, Pin 4 of the LTC1771 and the resistive divider. The power ground consists of the Schottky diode anode and the (–) plate of C_{IN} which should have as short lead lengths as possible.
7. Keep the switching node (SW) and the gate node (PGATE) away from sensitive small signal nodes, especially the voltage sensing feedback pin (V_{FB}), and minimize their PC trace area.
8. High impedance nodes such as I_{TH} and V_{FB} are very sensitive to leakage paths on the PC board due to stray flux, solder, epoxy, etc. **Make sure PC board is clean**. Water-soluble solder flux can be especially leaky if not cleaned properly. Leakage on I_{TH} will manifest itself as excessive output ripple during Burst Mode operation. If the problem persists, adding a 10M resistor from Pin 2 to ground should eliminate the problem.

APPLICATIONS INFORMATION

Design Example

As a design example, assume V_{IN} = 10V (nominal), V_{IN} = $15V_{(MAX)}$, V_{OUT} = 3.3V, and I_{MAX} = 2A. With this information, we can easily calculate all the important components.

R_{SENSE} = 100mV/2A = 0.05Ω

To optimize low current efficiency, MODE pin is tied to V_{IN} to enable Burst Mode operation, thus the minimum inductance necessary is:

L_{MIN} = 70µH(3.3V + 0.5)(0.05Ω) = 13.3µH

15µH is chosen for the application.

$$\Delta I_L = 3.5\mu s\left(\frac{3.3V + 0.5V}{15\mu H}\right) = 0.89A$$

For the feedback resistors, choose R1 = 1M to minimize supply current. R2 can then be calculated to be:

R2 = (V_{OUT}/1.23 – 1) • R1 = 1.68M

Assume that the MOSFET dissipation is to be limited to P_P = 0.25W.

If T_A = 70°C and the thermal resistance of the MOSFET is 83°C/W, then the junction temperatures will be 91°C and δ_P = 0.33. The required $R_{DS(ON)}$ for the MOSFET can now be calculated:

$$\text{P-Channel } R_{DS(ON)} = \frac{0.25W}{\left(\frac{3.3V + 0.5V}{10V + 0.5V}\right)(2A)^2(1.33)} = 0.130\Omega$$

Since the gate of the MOSFET will see the full input voltage, a MOSFET must be selected whose $V_{GS(MAX)}$ > 15V. A P-channel MOSFET that meets both the $V_{GS(MAX)}$ and $R_{DS(ON)}$ requirement is the Si6447DQ.

The most stringent requirement for the Schottky diode occurs when V_{OUT} = 0V (i.e., short circuit) at maximum V_{IN}. In this case the worst-case dissipation rises to:

$$P_D = I_{SC(AVG)}(V_D)\left(\frac{V_{IN}}{V_{IN} + V_D}\right)$$

With a 0.05Ω sense resistor $I_{SC(AVG)}$ = 2A will result, increasing the 0.5V Schottky diode dissipation to 1W.

C_{IN} is chosen for a RMS current rating of at least 1A at temperature. C_{OUT} is chosen with an ESR of 0.05Ω for low output ripple. The output voltage ripple due to ESR is approximately:

$V_{ORIPPLE} \approx (R_{ESR})(\Delta I_L)$ = 0.05Ω (0.89A_{P-P}) = 45mV_{P-P}

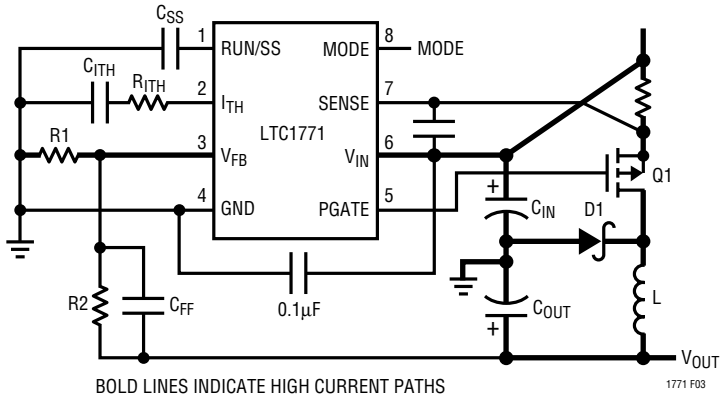
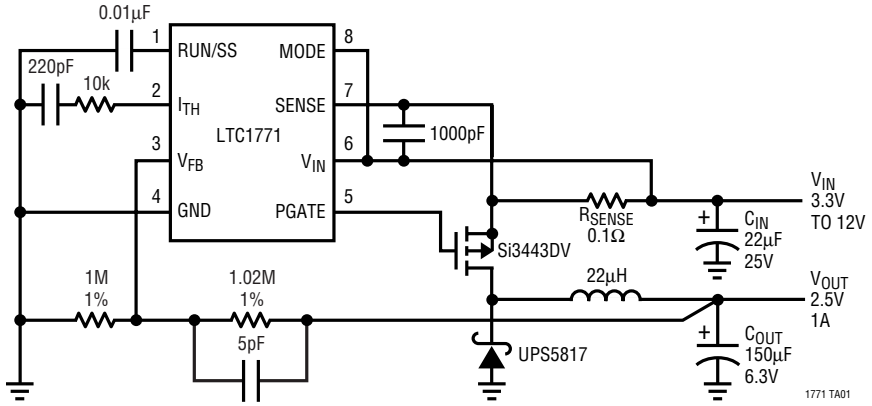


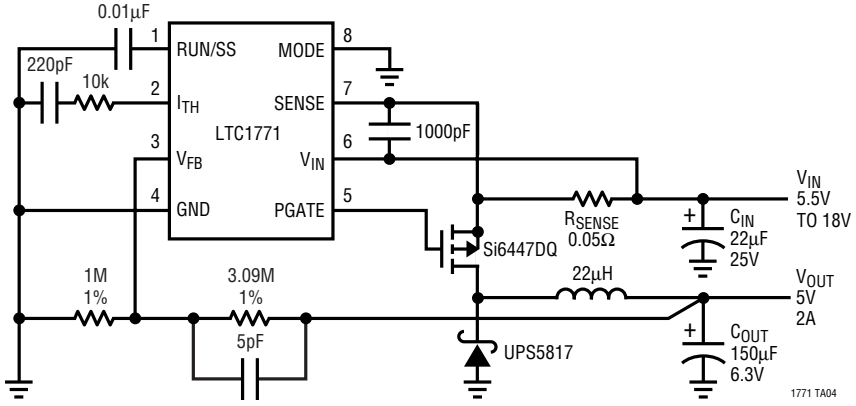
Figure 3. LTC1771 Layout Diagram

TYPICAL APPLICATIONS

3.3V to 2.5V/1A Regulator with Burst Mode Operation Enabled

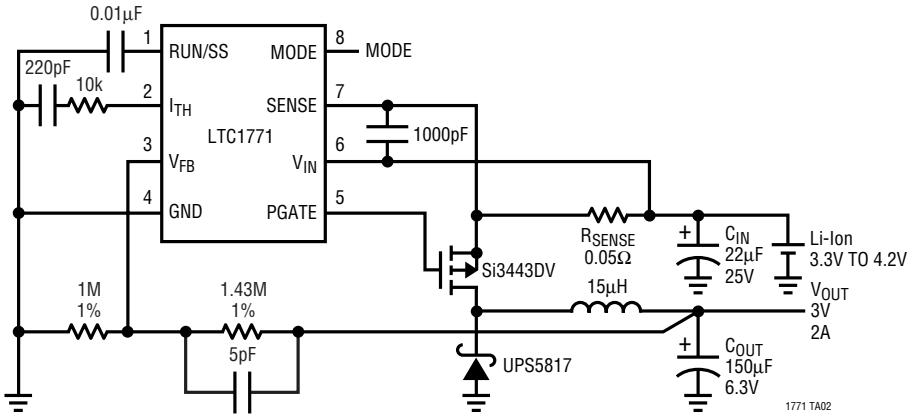


5V/2A Regulator with Burst Mode Operation Disabled

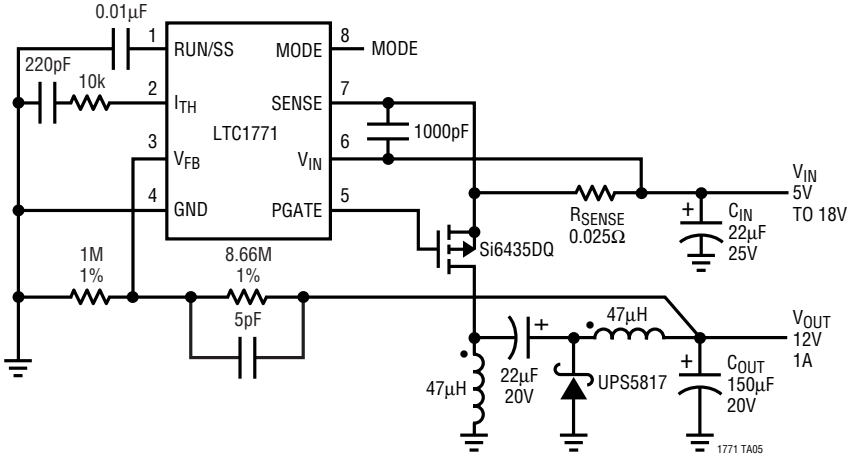


TYPICAL APPLICATIONS

Low Dropout Single Cell Lithium-Ion to 3V

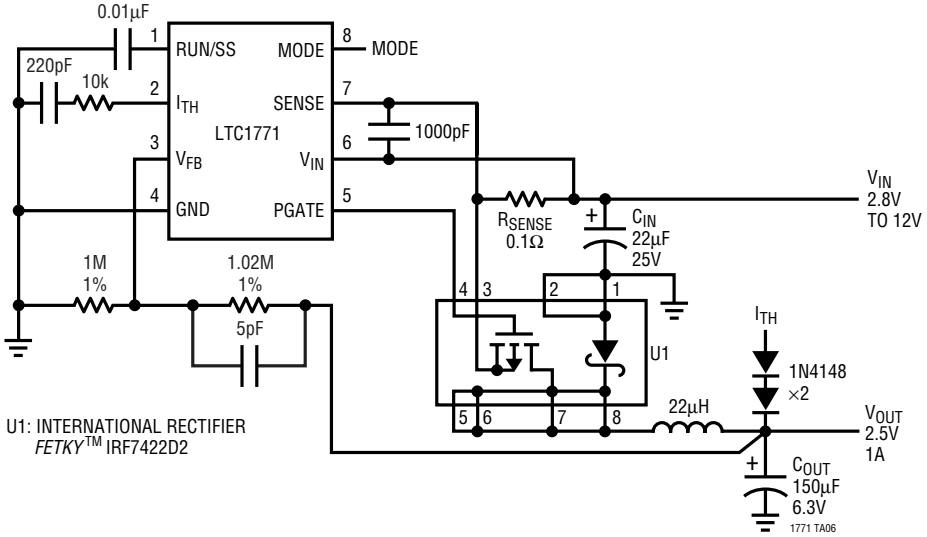


12V/1A Zeta Converter

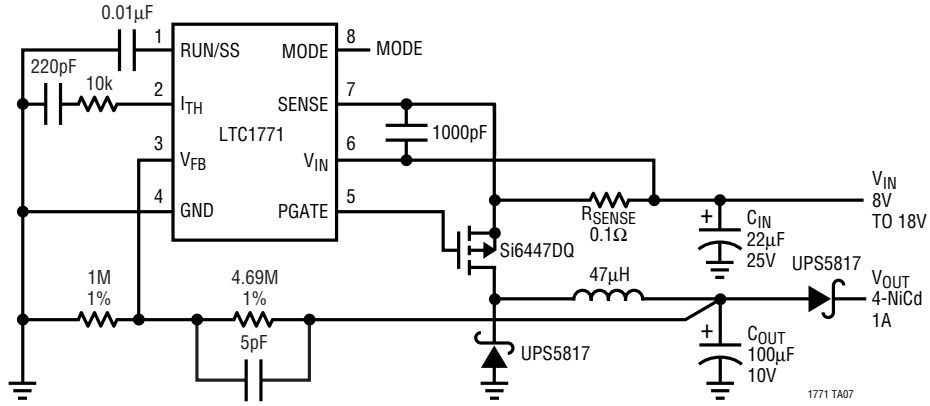


TYPICAL APPLICATIONS

2.5V/1A Regulator with Foldback Current Limit



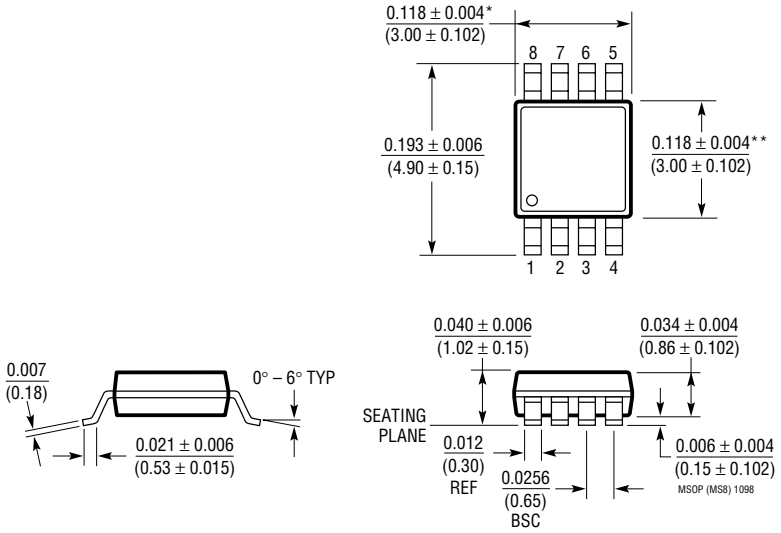
4-NiCd Battery Charger



PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

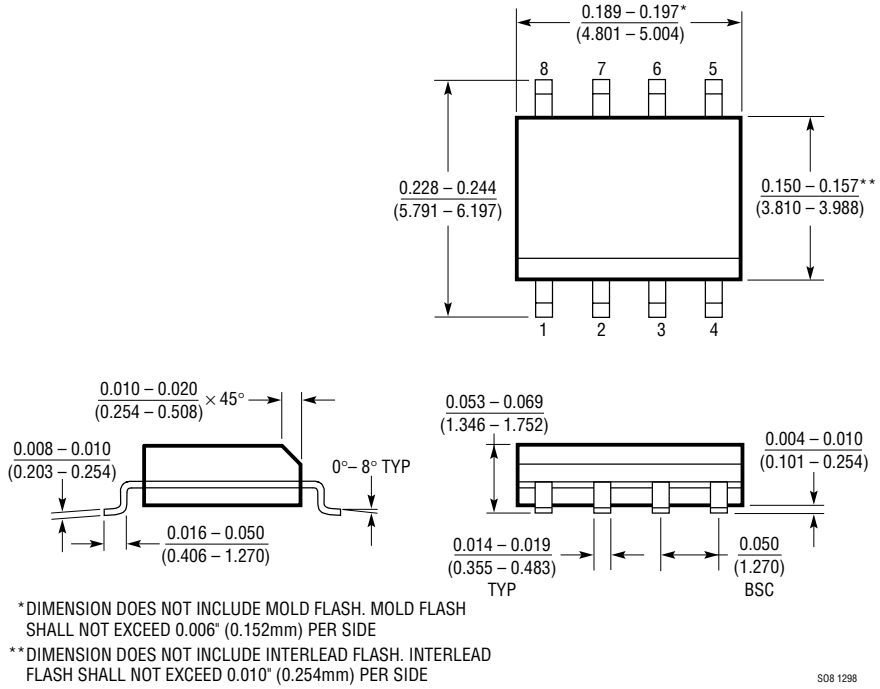
MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

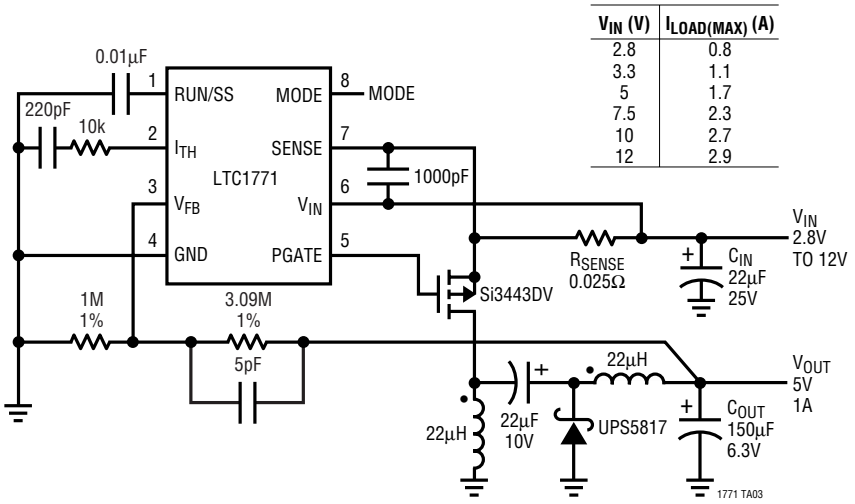


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

5V/1A Zeta Converter



V_{IN} (V)	$I_{LOAD(MAX)}$ (A)
2.8	0.8
3.3	1.1
5	1.7
7.5	2.3
10	2.7
12	2.9

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1147 Series	High Efficiency Step-Down Switching Regulator Controllers	100% DC, 3.5V ≤ V_{IN} ≤ 16V
LTC1174/LTC1174-3.3/LTC1174-5	High Efficiency Step-Down and Inverting DC/DC Converters	Selectable I_{PEAK} = 300mA or 600mA
LTC1265	1.2A High Efficiency Step-Down DC/DC Converter	Burst Mode Operation, Internal MOSFET
LTC1474/LTC1475	Low Quiscent Current Step-Down Regulators	Monolithic, I_Q = 10µA, 400mA, MS8
LTC1574/LTC1574-3.3/LTC1574-5	High Efficiency Step-Down DC/DC Converters with Internal Schottky Diode	LTC1174 with Internal Schottky Diode
LTC1622	Low Input Voltage Step-Down DC/DC Controller	Constant Frequency, 2V to 10V V_{IN}, MS8
LTC1624	High Efficiency SO-8 N-Channel Switching Regulator Controller	95% DC, 3.5V to 36V V_{IN}
LT®1761 Series	100mA, Low Noise, LDO Micropower Regulators in SOT-23	20µA Quiescent Current, 20µV_{RMS} Noise
LT1763 Series	500mA, Low Noise, LDO Micropower Regulators	30µA Quiescent Current, 20µV_{RMS} Noise
LTC1772	Constant Frequency Step-Down DC/DC Controller	SOT-23, 2.2V to 9.8V V_{IN}

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