

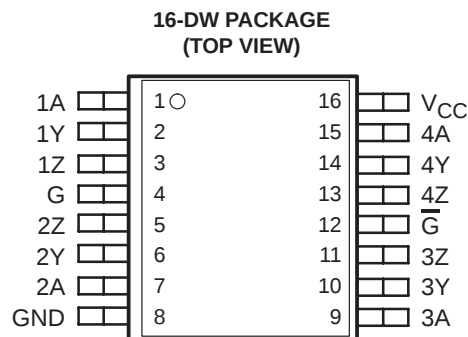
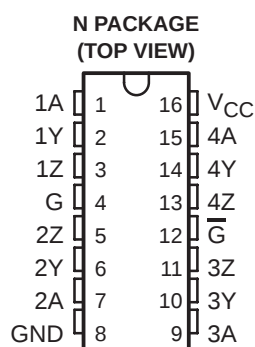
# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

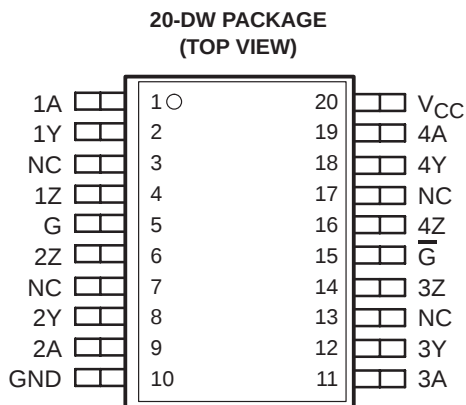
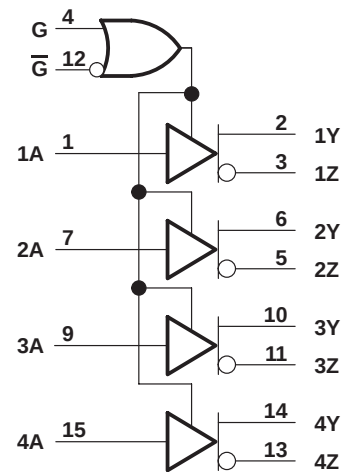
- Designed for TIA/EIA-485, TIA/EIA-422, and ISO 8482 Applications
- Signaling Rates<sup>†</sup> up to 30 Mbps
- Propagation Delay Times <11 ns
- Low Standby Power Consumption  
1.5 mA Max
- Output ESD Protection 12 kV
- Driver Positive- and Negative-Current Limiting
- Power-Up and Power-Down Glitch-Free for Live Insertion Applications
- Thermal Shutdown Protection
- Industry Standard Pin-Out, Compatible With SN75172, AM26LS31, DS96172, LTC486, and MAX3045

## description

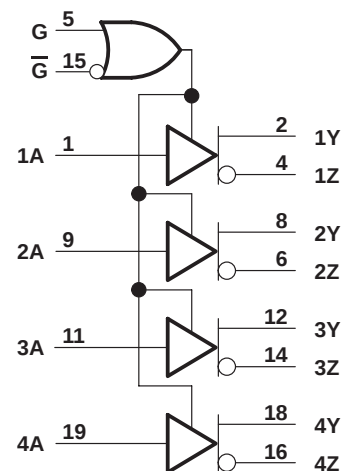
The SN65LBC172A and SN75LBC172A are quadruple differential line drivers with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications.



## logic diagram (positive logic)



## logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments.

<sup>†</sup>The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2008 – 2003, Texas Instruments Incorporated

# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

## description (continued)

These devices are optimized for balanced multipoint bus transmission at signalling rates up to 30 million bits per second. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

Each driver features current limiting and thermal-shutdown circuitry making it suitable for high-speed multipoint data transmission applications in noisy environments. These devices are designed using LinBiCMOS™, facilitating low power consumption and robustness.

The G and  $\overline{G}$  inputs provide driver enable control using either positive or negative logic. When disabled or powered off, the driver outputs present a high-impedance to the bus for reduced system loading.

The SN75LBC172A is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC172A is characterized over the temperature range from –40°C to 85°C.

### AVAILABLE OPTIONS

| T <sub>A</sub> | PACKAGE                                            |                                                    |                                                  |
|----------------|----------------------------------------------------|----------------------------------------------------|--------------------------------------------------|
|                | 16-PIN PLASTIC<br>SMALL OUTLINE†<br>(JEDEC MS-013) | 20-PIN PLASTIC<br>SMALL OUTLINE†<br>(JEDEC MS-013) | 16-PIN PLASTIC<br>THROUGH-HOLE<br>(JEDEC MS-001) |
| 0°C to 70°C    | SN75LBC172A16DW                                    | SN75LBC172ADW                                      | SN75LBC172AN                                     |
|                | Marked as 75LBC172A                                |                                                    |                                                  |
| –40°C to 85°C  | SN65LBC172A16DW                                    | SN65LBC172ADW                                      | SN65LBC172AN                                     |
|                | Marked as 65LBC172A                                |                                                    |                                                  |

† Add R suffix for taped and reeled version.

### FUNCTION TABLE (EACH DRIVER)

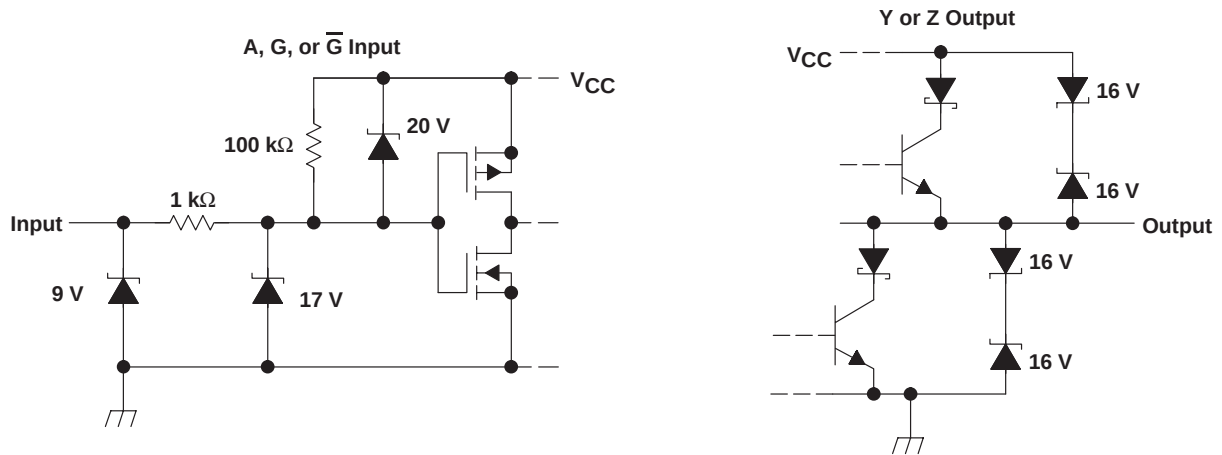
| INPUT | ENABLES |                | OUTPUTS |   |
|-------|---------|----------------|---------|---|
| A     | G       | $\overline{G}$ | Y       | Z |
| L     | H       | X              | L       | H |
| L     | X       | L              | L       | H |
| H     | H       | X              | H       | L |
| H     | X       | L              | H       | L |
| OPEN  | H       | X              | H       | L |
| OPEN  | X       | L              | H       | L |
| H     | OPEN    | X              | H       | L |
| L     | OPEN    | X              | L       | H |
| X     | L       | H              | Z       | Z |
| X     | L       | OPEN           | Z       | Z |

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off)

# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

## equivalent input and output schematic diagrams



## absolute maximum ratings<sup>†</sup>

|                                                                                                |                              |
|------------------------------------------------------------------------------------------------|------------------------------|
| Supply voltage range, $V_{CC}$ (see Note 1)                                                    | –0.3 V to 6 V                |
| Output voltage range, $V_O$ , at any bus (steady state)                                        | –10 V to 15 V                |
| Output voltage range, $V_O$ , at any bus (transient pulse through 100 $\Omega$ , see Figure 8) | –30 V to 30 V                |
| Input voltage range, $V_I$ , at any A, G, or $\bar{G}$ terminal                                | –0.5 V to $V_{CC} + 0.5$ V   |
| Electrostatic discharge: Human body model (see Note 2)                                         | Y, Z, and GND 12 kV          |
|                                                                                                | All pins 5 kV                |
| Charged-device model (see Note 3)                                                              | All pins 1 kV                |
| Storage temperature range, $T_{stg}$                                                           | –65°C to 150°C               |
| Continuous power dissipation                                                                   | See Dissipation Rating Table |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds                                   | 260°C                        |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential I/O bus voltages, are with respect to GND.
  2. Tested in accordance with JEDEC standard 22, Test Method A114–A.
  3. Tested in accordance with JEDEC standard 22, Test Method C101.

DISSIPATION RATING TABLE

| PACKAGE   | JEDEC BOARD MODEL | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR <sup>‡</sup><br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 85^\circ\text{C}$<br>POWER RATING |
|-----------|-------------------|---------------------------------------------|----------------------------------------------------------------|------------------------------------------|------------------------------------------|
| 16-PIN DW | Low K             | 1200 mW                                     | 9.6 mW/°C                                                      | 769 mW                                   | 625 mW                                   |
|           | High K            | 2240 mW                                     | 17.9 mW/°C                                                     | 1434 mW                                  | 1165 mW                                  |
| 20-PIN DW | Low K             | 1483 mW                                     | 11.86 mW/°C                                                    | 949 mW                                   | 771 mW                                   |
|           | High K            | 2753 mW                                     | 22 mW/°C                                                       | 1762 mW                                  | 1432 mW                                  |
| 16-PIN N  | Low K             | 1150 mW                                     | 9.2 mW/°C                                                      | 736 mW                                   | 598 mW                                   |

<sup>‡</sup> This is the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.

# SN65LBC172A, SN75LBC172A

## QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

### recommended operating conditions

|                                                |                      | MIN  | NOM | MAX             | UNIT |
|------------------------------------------------|----------------------|------|-----|-----------------|------|
| Supply voltage, V <sub>CC</sub>                |                      | 4.75 | 5   | 5.25            | V    |
| Voltage at any bus terminal                    | Y, Z                 | −7   |     | 12              | V    |
| High-level input voltage, V <sub>IH</sub>      | A, G, $\overline{G}$ | 2    |     | V <sub>CC</sub> | V    |
| Low-level input voltage, V <sub>IL</sub>       |                      | 0    |     | 0.8             |      |
| Output current                                 |                      | −60  |     | 60              | mA   |
| Operating free-air temperature, T <sub>A</sub> | SN75LBC172A          | 0    |     | 70              | °C   |
|                                                | SN65LBC172A          | −40  |     | 85              |      |

### electrical characteristics over recommended operating conditions

| PARAMETER           |                                                                         | TEST CONDITIONS                            |                                      | MIN   | TYP <sup>†</sup> | MAX      | UNIT    |
|---------------------|-------------------------------------------------------------------------|--------------------------------------------|--------------------------------------|-------|------------------|----------|---------|
| $V_{IK}$            | Input clamp voltage                                                     | $I_I = -18$ mA                             |                                      | -1.5  | -0.77            |          | V       |
| $V_O$               | Open-circuit output voltage                                             | Y or Z, No load                            |                                      | 0     |                  | $V_{CC}$ | V       |
| $ V_{OD(SS)} $      | Steady-state differential output voltage magnitude <sup>‡</sup>         | No load (open circuit)                     |                                      | 3     |                  | $V_{CC}$ | V       |
|                     |                                                                         | $R_L = 54 \Omega$ , see Figure 1           |                                      | 1     | 1.6              | 2.5      |         |
|                     |                                                                         | With common-mode loading, see Figure 2     |                                      | 1     | 1.6              | 2.5      |         |
| $\Delta V_{OD(SS)}$ | Change in steady-state differential output voltage between logic states | See Figure 1                               |                                      | -0.1  |                  | 0.1      | V       |
| $V_{OC(SS)}$        | Steady-state common-mode output voltage                                 | See Figure 3                               |                                      | 2     | 2.4              | 2.8      | V       |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic states  | See Figure 3                               |                                      | -0.02 |                  | 0.02     | V       |
| $I_I$               | Input current                                                           | A, G, $\overline{G}$                       |                                      | -50   |                  | 50       | $\mu$ A |
| $I_{OS}$            | Short-circuit output current                                            | $V_{TEST} = -7$ V to 12 V,<br>See Figure 7 | $V_I = 0$ V                          | -200  |                  | 200      | mA      |
|                     |                                                                         |                                            | $V_I = V_{CC}$                       |       |                  |          |         |
| $I_{OZ}$            | High-impedance-state output current                                     |                                            | G at 0 V, $\overline{G}$ at $V_{CC}$ | -50   |                  | 50       | $\mu$ A |
| $I_{O(OFF)}$        | Output current with power off                                           |                                            | $V_{CC} = 0$ V                       | -10   |                  | 10       |         |
| $I_{CC}$            | Supply current                                                          | $V_I = 0$ V or $V_{CC}$ ,<br>No load       | All drivers enabled                  |       |                  | 23       | mA      |
|                     |                                                                         |                                            | All drivers disabled                 |       |                  | 1.5      |         |

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V and 25°C.

<sup>‡</sup> The minimum  $V_{OD}$  may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly of lower output signal into account in determining the maximum signal transmission distance.

# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

## switching characteristics over recommended operating conditions

| PARAMETER                                                             | TEST CONDITIONS                                                  | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------------------|------------------------------------------------------------------|-----|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low-to-high level output            | $R_L = 54 \, \Omega$ , $C_L = 50 \, \text{pF}$ ,<br>see Figure 4 | 5.5 | 8   | 11  | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low level output            |                                                                  | 5.5 | 8   | 11  | ns   |
| $t_r$ Differential output voltage rise time                           |                                                                  | 3   | 7.5 | 11  | ns   |
| $t_f$ Differential output voltage fall time                           |                                                                  | 3   | 7.5 | 11  | ns   |
| $t_{sk(p)}$ Pulse skew $ t_{PLH} - t_{PHL} $                          |                                                                  |     | 0.6 | 2   | ns   |
| $t_{sk(o)}$ Output skew <sup>†</sup>                                  |                                                                  |     |     | 2   | ns   |
| $t_{sk(pp)}$ Part-to-part skew <sup>‡</sup>                           |                                                                  |     |     | 3   | ns   |
| $t_{PZH}$ Propagation delay time, high-impedance-to-high-level output | See Figure 5                                                     |     |     | 25  | ns   |
| $t_{PHZ}$ Propagation delay time, high-level-output-to-high impedance |                                                                  |     |     | 25  | ns   |
| $t_{PZL}$ Propagation delay time, high-impedance-to-low-level output  | See Figure 6                                                     |     |     | 30  | ns   |
| $t_{PLZ}$ Propagation delay time, low-level-output-to-high impedance  |                                                                  |     |     | 20  | ns   |

<sup>†</sup> Output skew ( $t_{sk(o)}$ ) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

<sup>‡</sup> Part-to-part skew ( $t_{sk(pp)}$ ) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

## PARAMETER MEASUREMENT INFORMATION

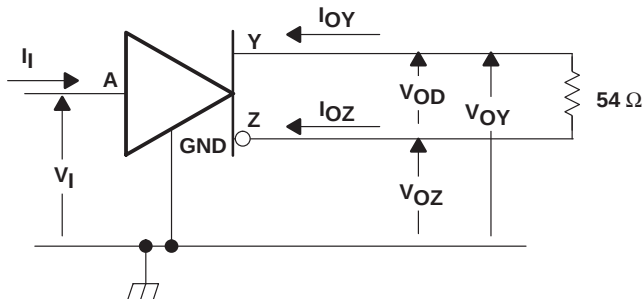


Figure 1. Test Circuit,  $V_{OD}$  Without Common-Mode Loading

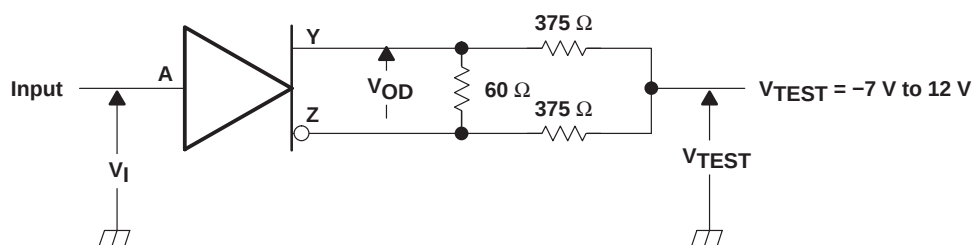
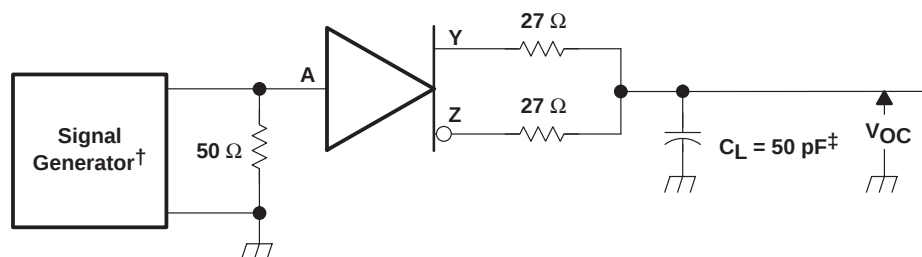


Figure 2. Test Circuit,  $V_{OD}$  With Common-Mode Loading



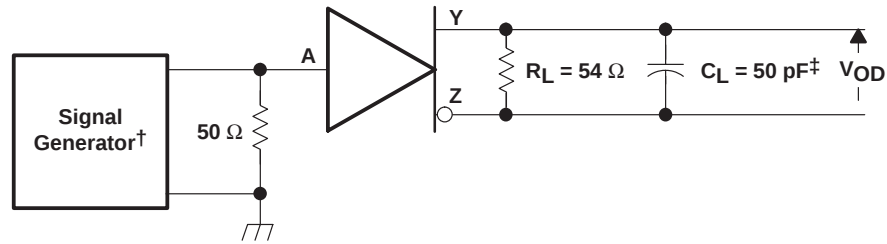
† PRR = 1 MHz, 50% duty cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

‡ Includes probe and jig capacitance

Figure 3.  $V_{OC}$  Test Circuit

# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008



† PRR = 1 MHz, 50% duty cycle,  $t_r < 6\ \text{ns}$ ,  $t_f < 6\ \text{ns}$ ,  $Z_O = 50\ \Omega$

‡ Includes probe and jig capacitance

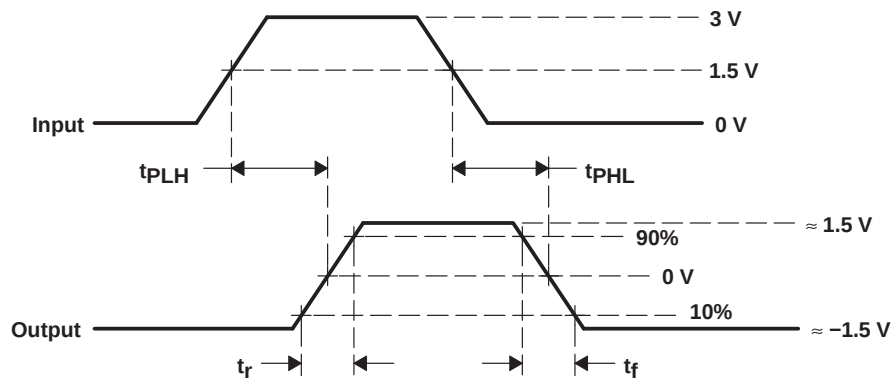
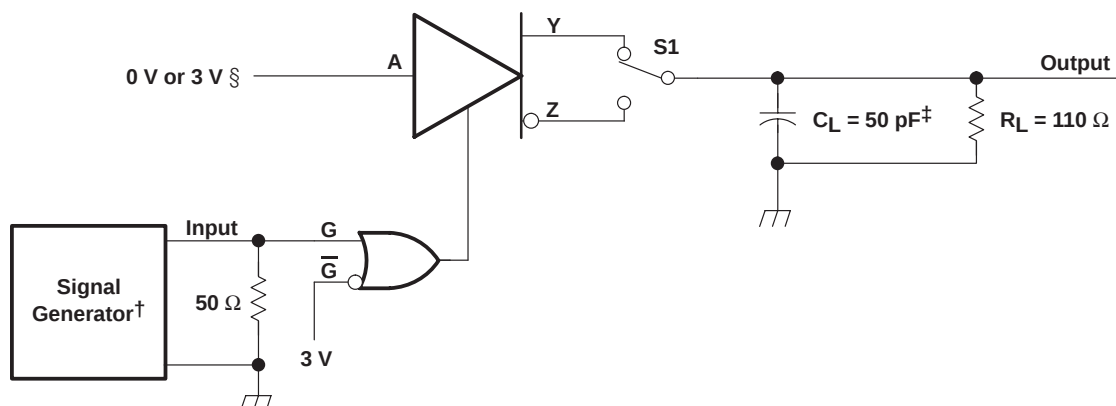


Figure 4. Output Switching Test Circuit and Waveforms

# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

## PARAMETER MEASUREMENT INFORMATION



† PRR = 1 MHz, 50% duty cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

‡ Includes probe and jig capacitance

§ 3-V if testing Y output, 0 V if testing Z output

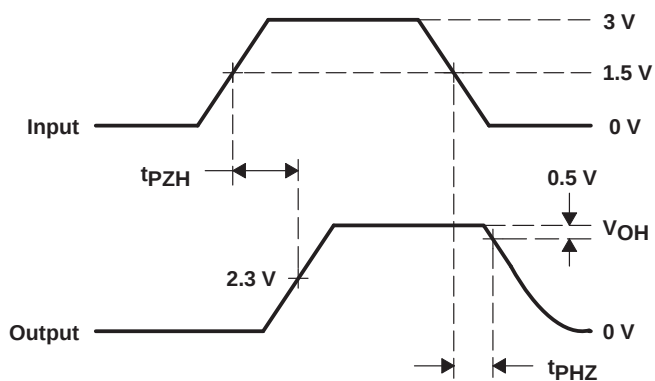
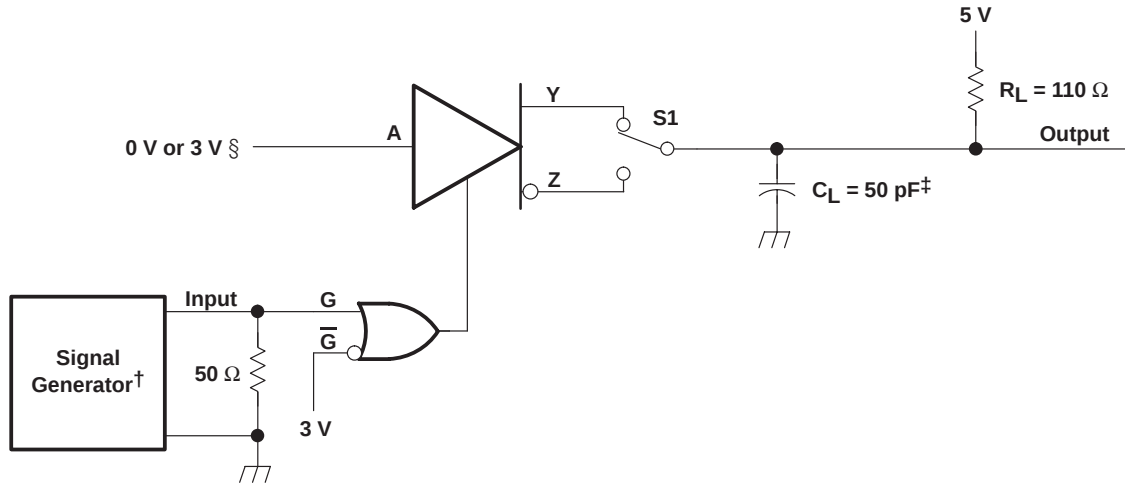


Figure 5. Enable Timing Test Circuit and Waveforms,  $t_{pZH}$  and  $t_{pHZ}$

PARAMETER MEASUREMENT INFORMATION



† PRR = 1 MHz, 50% duty cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

‡ Includes probe and jig capacitance

§ 3-V if testing Y output, 0 V if testing Z output

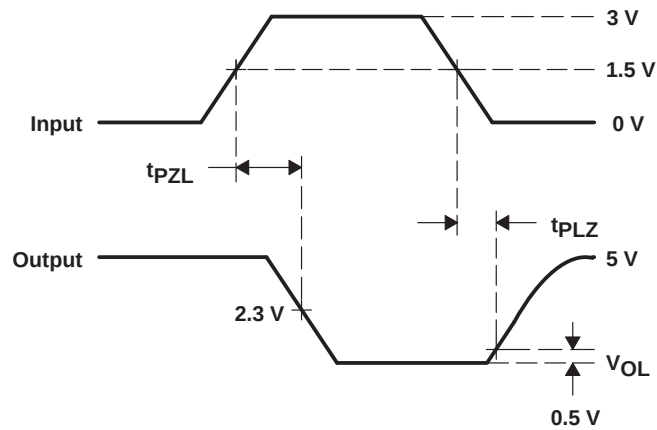


Figure 6. Enable Timing Test Circuit and Waveforms,  $t_{PZL}$  and  $t_{PLZ}$

# SN65LBC172A, SN75LBC172A QUADRUPLER RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

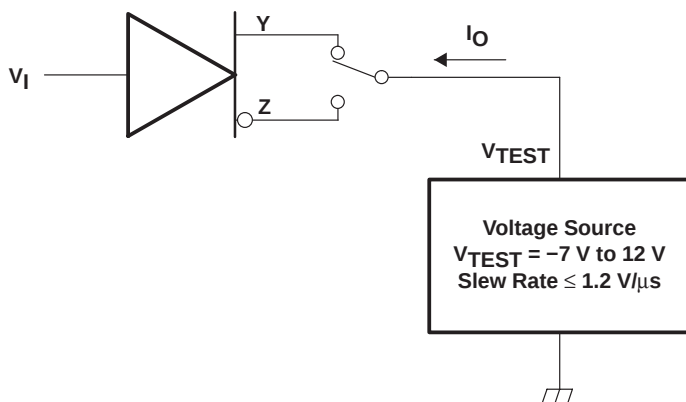


Figure 7. Test Circuit, Short-Circuit Output Current

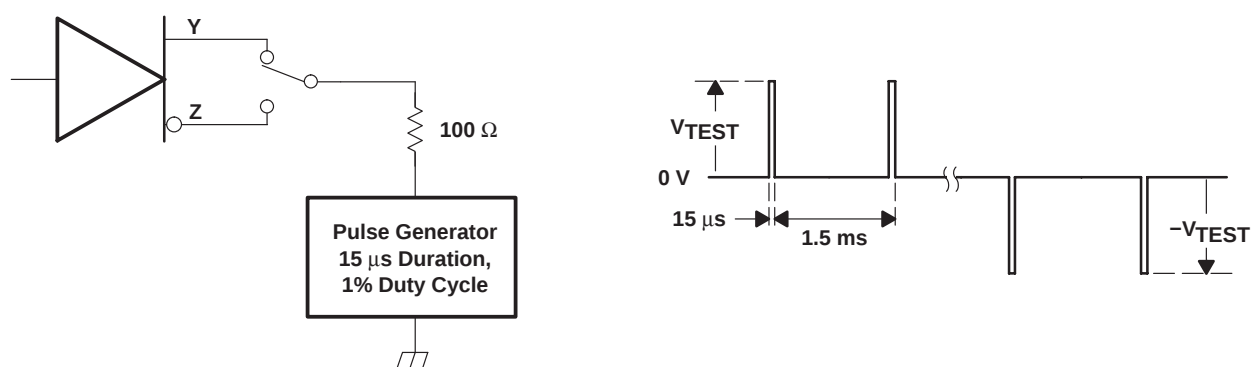


Figure 8. Test Circuit and Waveform, Transient Over-Voltage

# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

## TYPICAL CHARACTERISTICS

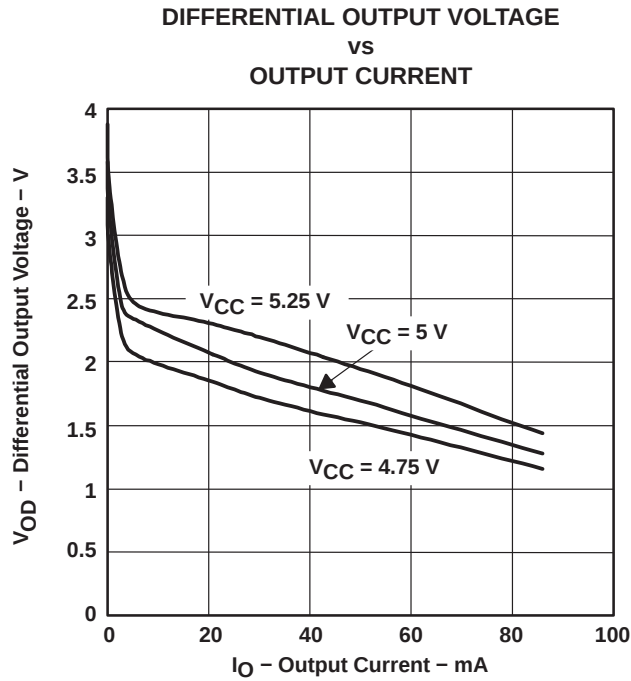


Figure 9

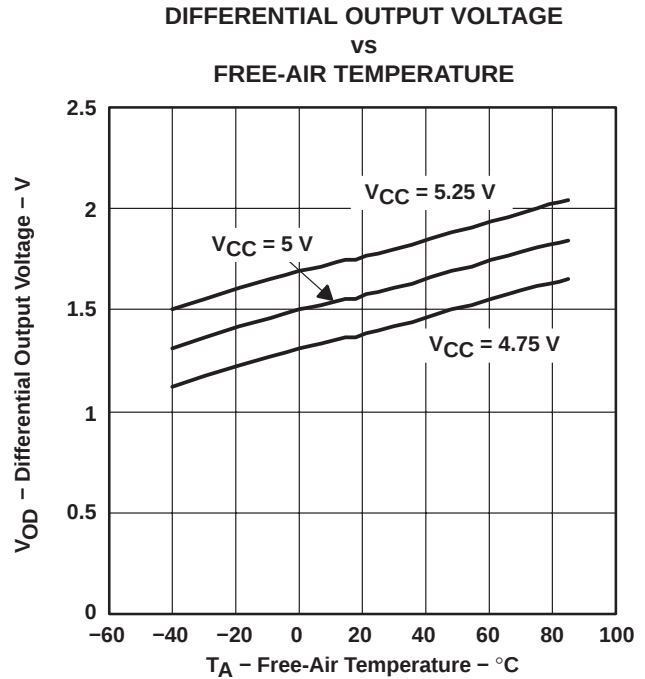


Figure 10

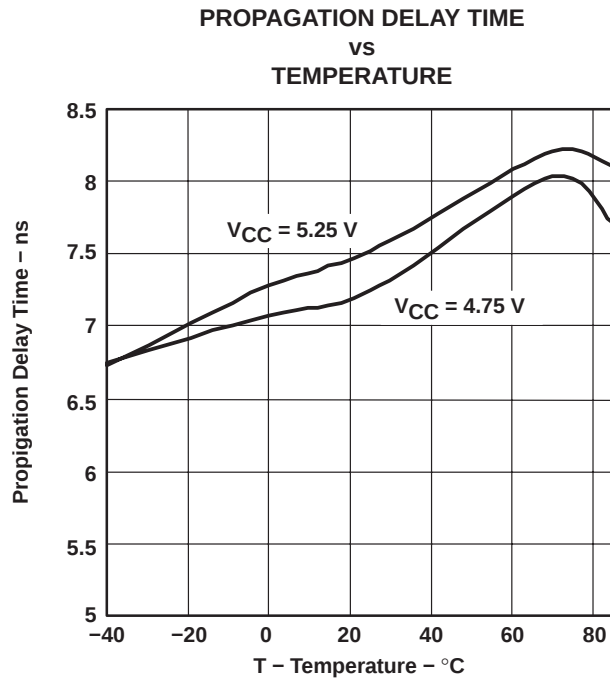


Figure 11

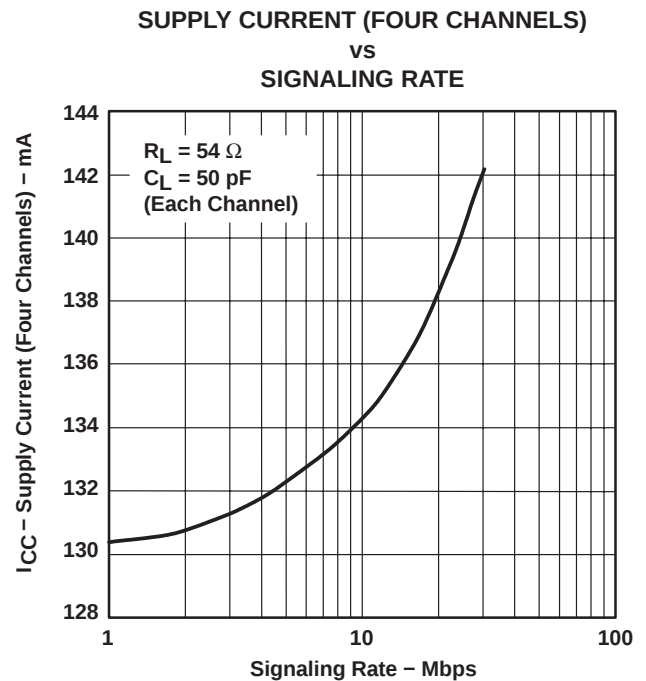


Figure 12

# SN65LBC172A, SN75LBC172A QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

SLLS447C – OCTOBER 2000 – REVISED AUGUST 2008

## TYPICAL CHARACTERISTICS

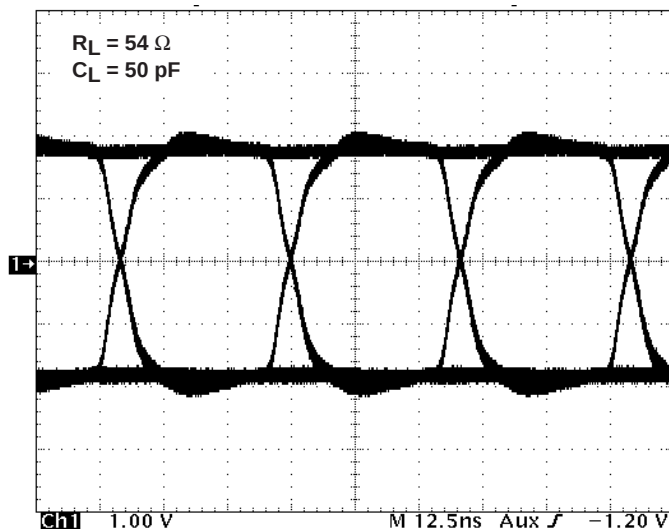


Figure 13. Eye Pattern, Pseudorandom Data at 30 Mbps

## APPLICATION INFORMATION

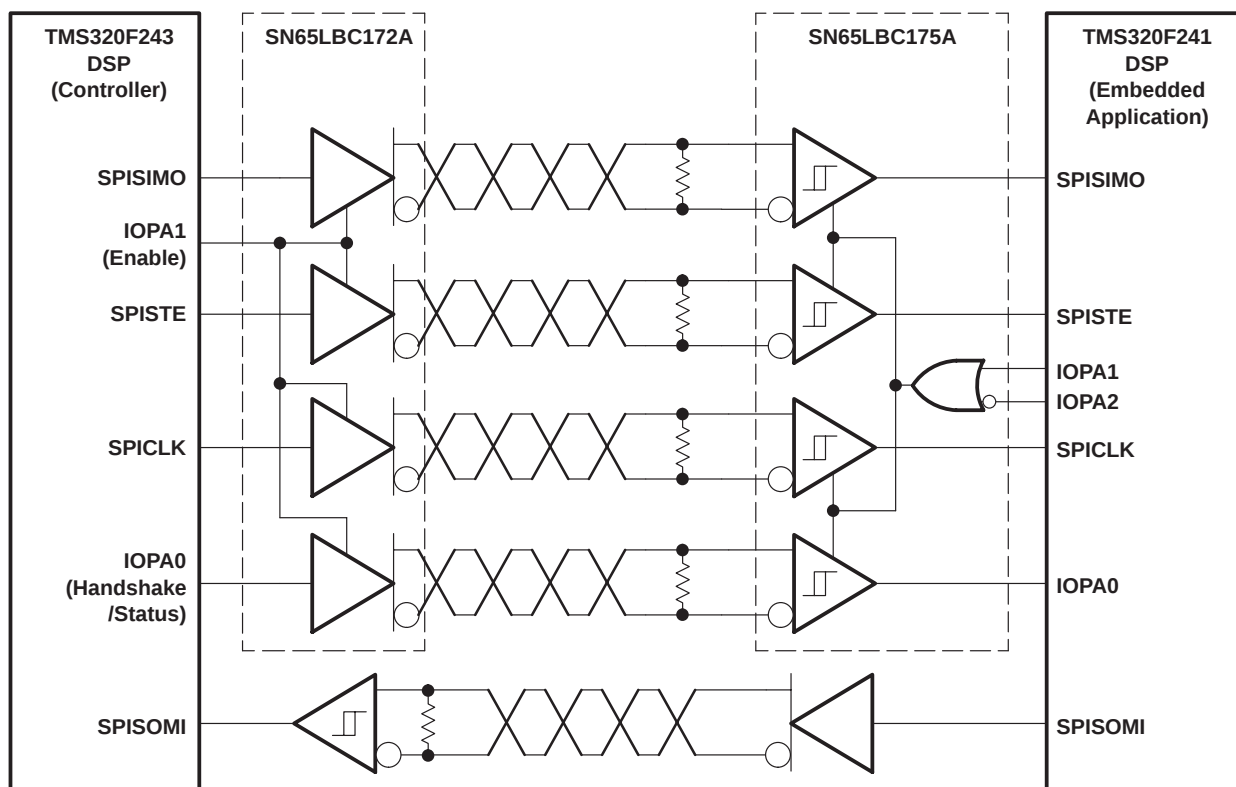


Figure 14. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65LBC172A16DW  | ACTIVE        | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 65LBC172A               | <a href="#">Samples</a> |
| SN65LBC172A16DWR | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 65LBC172A               | <a href="#">Samples</a> |
| SN65LBC172ADW    | ACTIVE        | SOIC         | DW                 | 20   | 25             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 65LBC172A               | <a href="#">Samples</a> |
| SN65LBC172ADWR   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 65LBC172A               | <a href="#">Samples</a> |
| SN65LBC172AN     | ACTIVE        | PDIP         | N                  | 16   | 25             | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | 65LBC172A               | <a href="#">Samples</a> |
| SN65LBC172ANE4   | ACTIVE        | PDIP         | N                  | 16   | 25             | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | 65LBC172A               | <a href="#">Samples</a> |
| SN75LBC172A16DW  | ACTIVE        | SOIC         | DW                 | 16   | 40             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75LBC172A               | <a href="#">Samples</a> |
| SN75LBC172A16DWR | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75LBC172A               | <a href="#">Samples</a> |
| SN75LBC172ADW    | ACTIVE        | SOIC         | DW                 | 20   | 25             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75LBC172A               | <a href="#">Samples</a> |
| SN75LBC172ADWR   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75LBC172A               | <a href="#">Samples</a> |
| SN75LBC172AN     | ACTIVE        | PDIP         | N                  | 16   | 25             | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | 75LBC172A               | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LBC172A16DWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| SN65LBC172ADWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN75LBC172A16DWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| SN75LBC172ADWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LBC172A16DWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| SN65LBC172ADWR   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN75LBC172A16DWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| SN75LBC172ADWR   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

## TUBE



\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65LBC172A16DW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| SN65LBC172ADW   | DW           | SOIC         | 20   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN65LBC172ADW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN65LBC172AN    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN65LBC172ANE4  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN75LBC172A16DW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| SN75LBC172ADW   | DW           | SOIC         | 20   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN75LBC172ADW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN75LBC172AN    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

## GENERIC PACKAGE VIEW

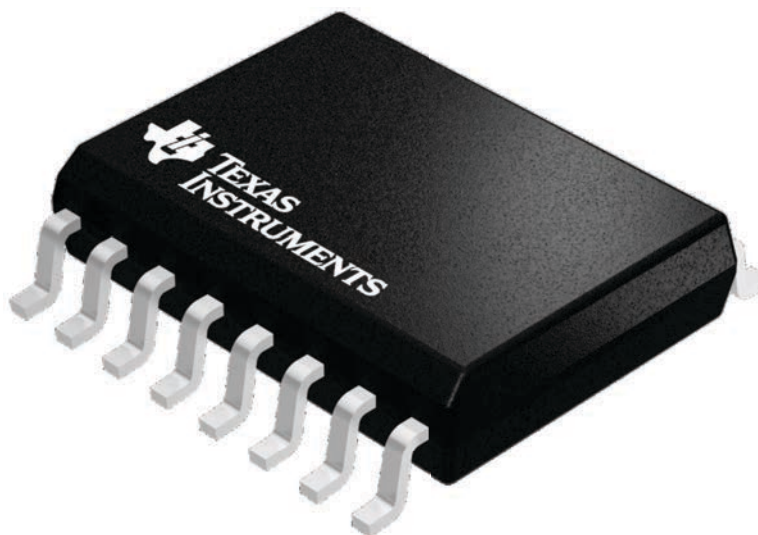
**DW 16**

**SOIC - 2.65 mm max height**

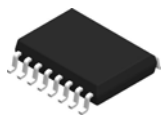
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

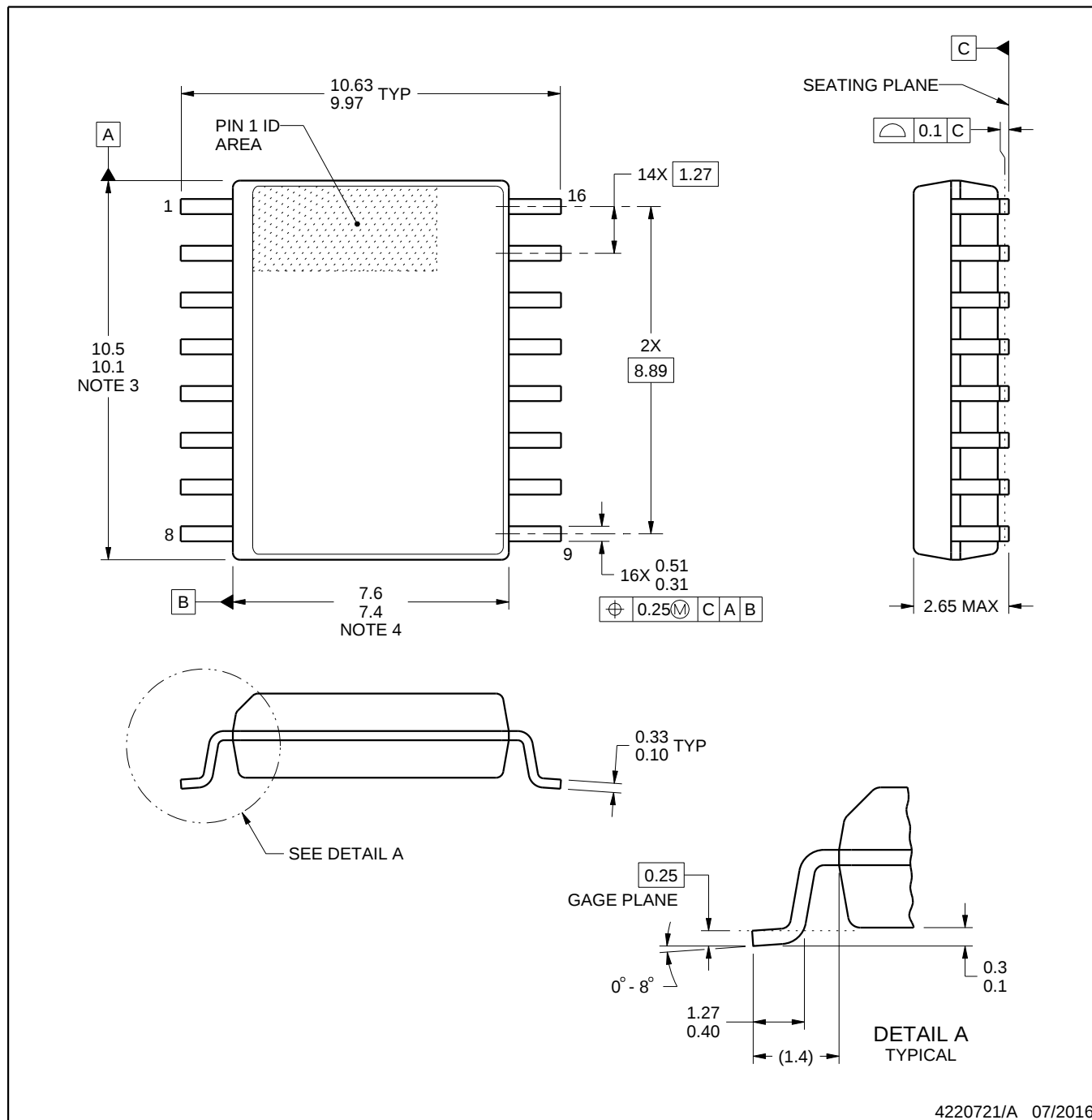


DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

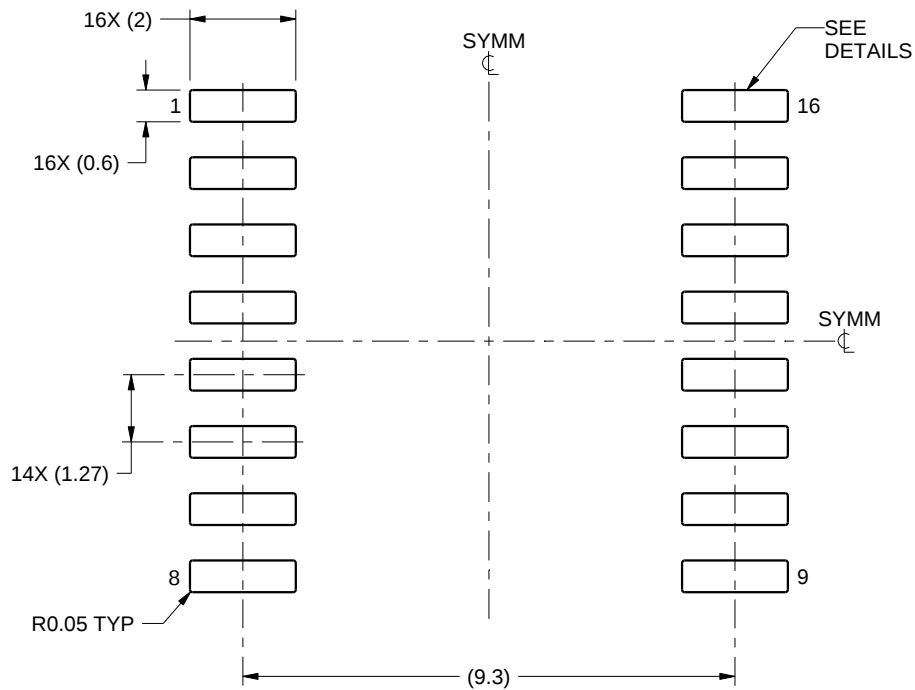
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

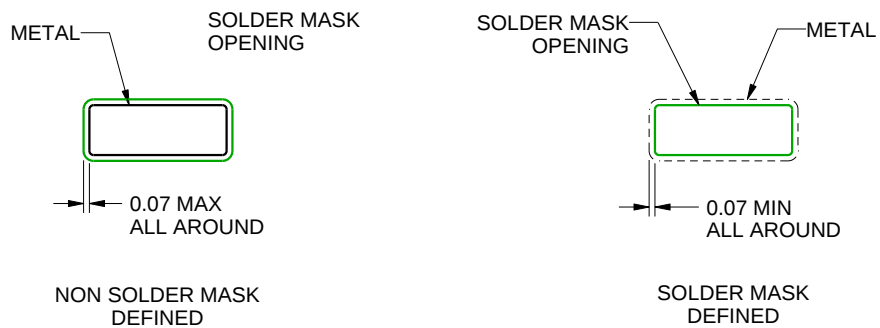
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

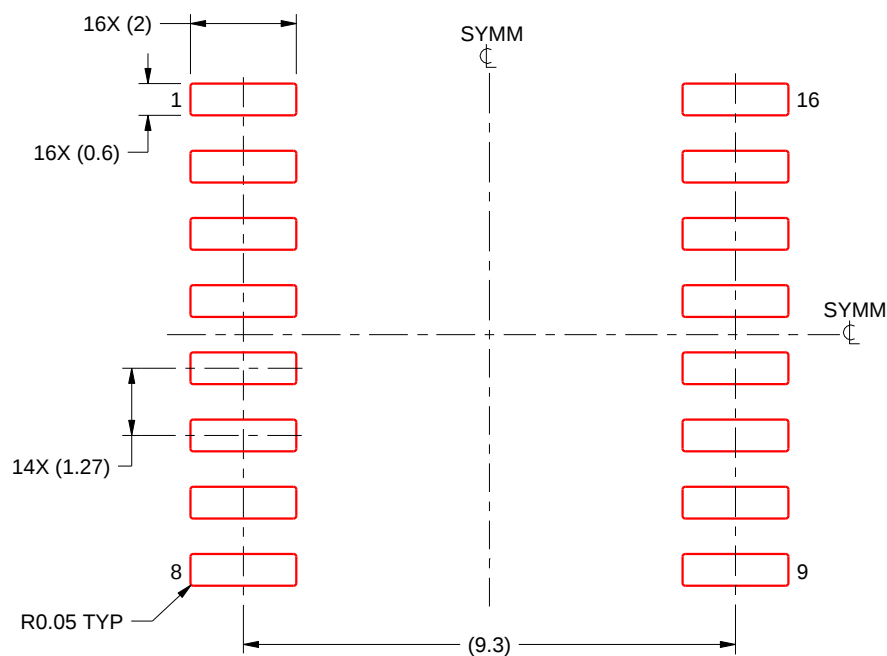
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



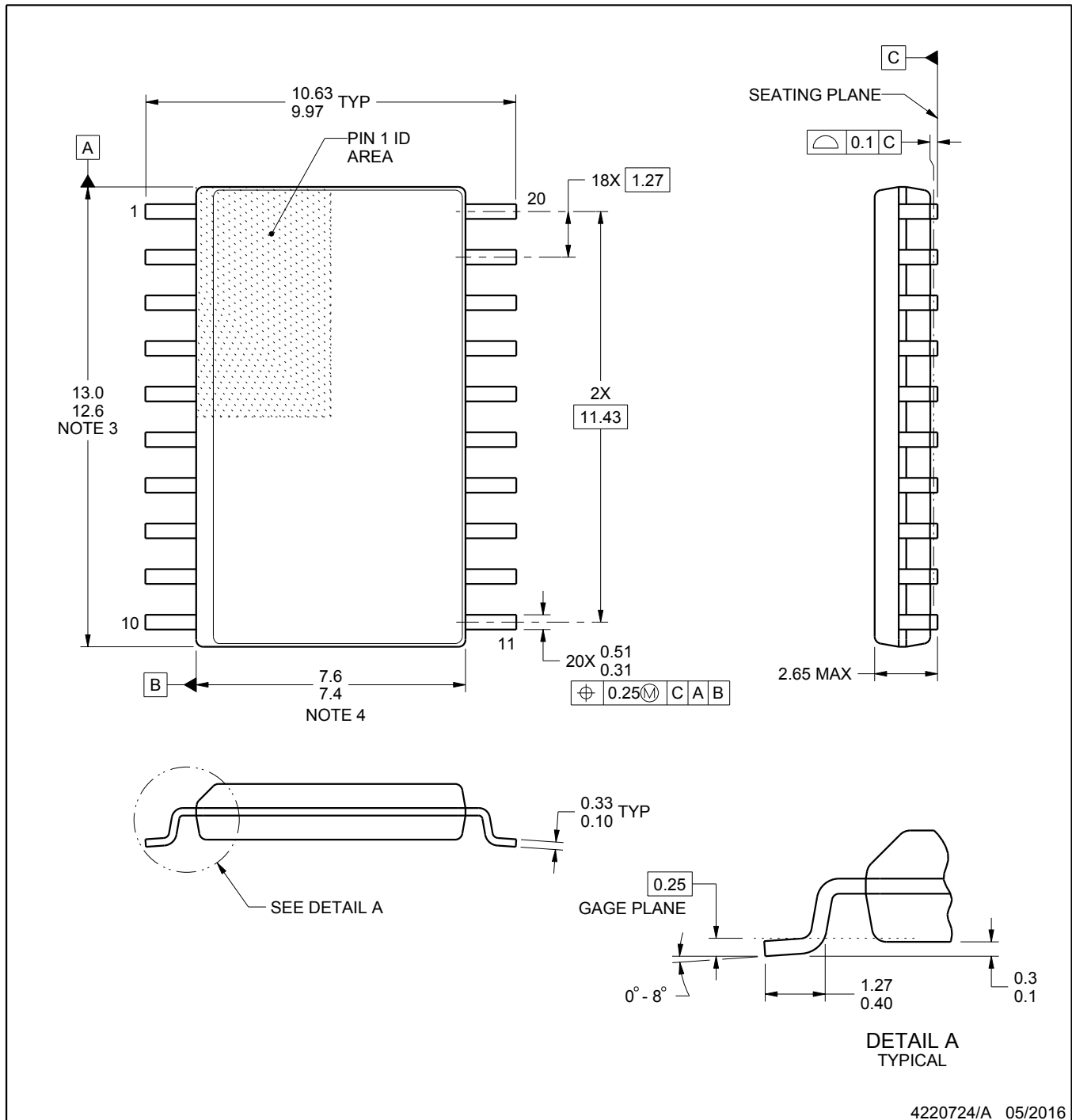
| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

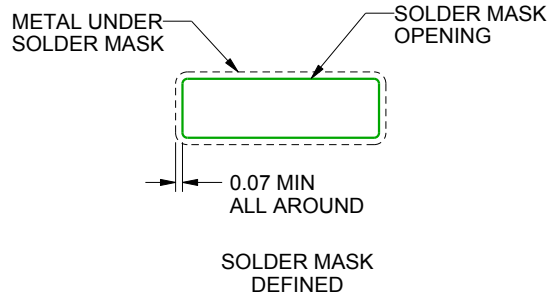
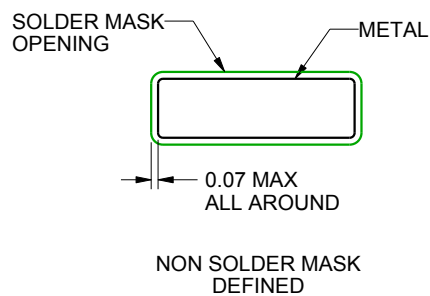
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated