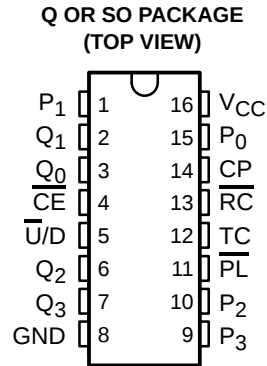


- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- 64-mA Output Sink Current
32-mA Output Source Current



description

The CY74FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the CY74FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple-clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
$\overline{CE}$	Count enable input (active low)
CP	Clock pulse input (active rising edge)
P	Parallel data inputs
$\overline{PL}$	Asynchronous parallel load input (active low)
$\overline{U/D}$	Up/down count control input
Q	Flip-flop outputs
$\overline{RC}$	Ripple clock output (active low)
TC	Terminal count output



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

CY74FCT191T

4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

ORDERING INFORMATION

T _A	PACKAGE [†]		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	6.2	CY74FCT191CTQCT	FT191-3
	SOIC – SO	Tube	6.2	CY74FCT191CTSOC	FCT191C
		Tape and reel	6.2	CY74FCT191CTSOCT	
	SOIC – SO	Tube	7.8	CY74FCT191ATSOC	FCT191A
		Tape and reel	7.8	CY74FCT191ATSOCT	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

$\overline{RC}$ FUNCTION

INPUTS		OUTPUTS	
$\overline{CE}$	CP	TC [†]	$\overline{RC}$
L		H	
H	X	X	H
X	X	L	H

H = High logic level, L = Low logic level,

X = Don't care,  = Low pulse

[†] TC is generated internally.

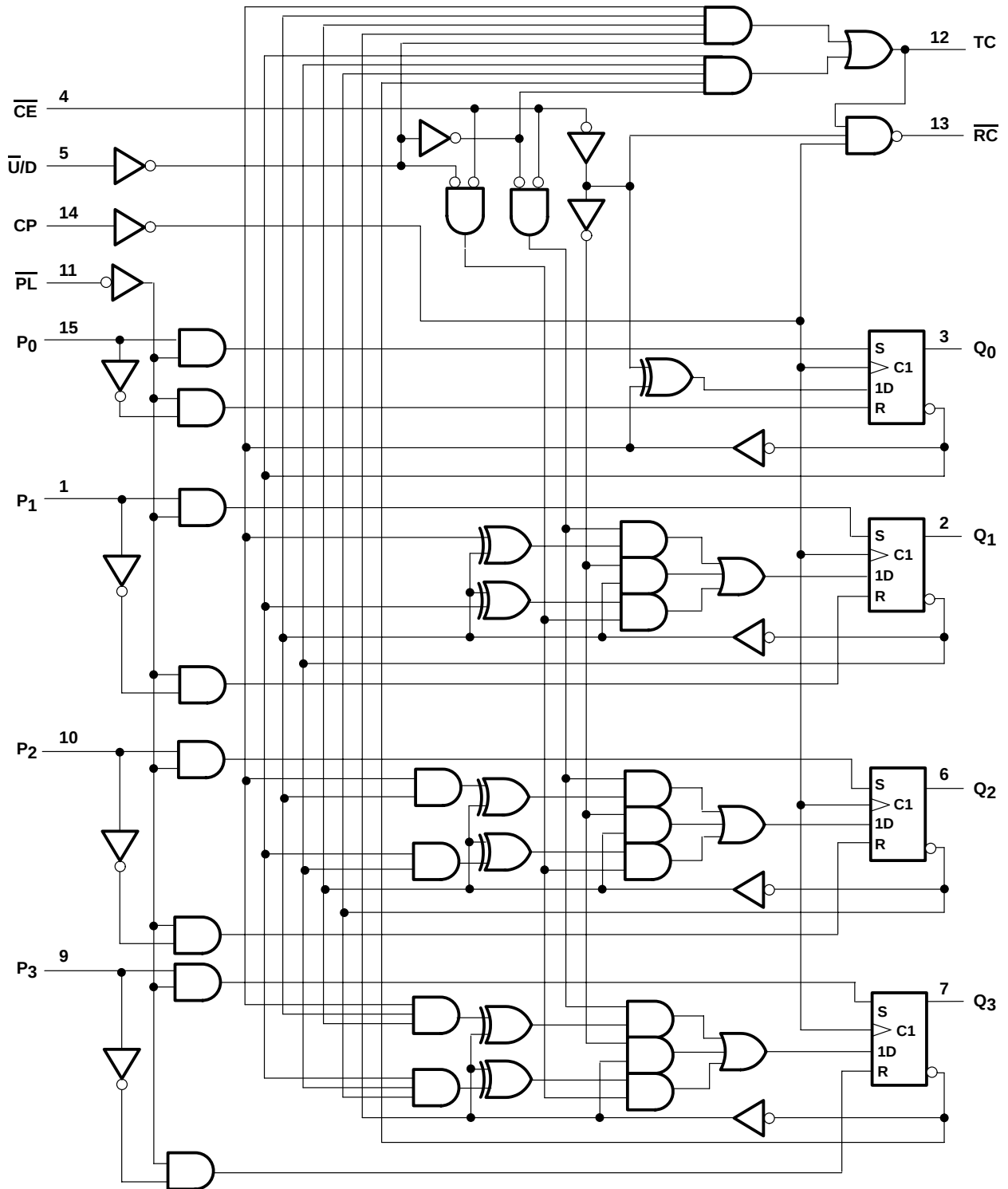
MODE SELECT

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L	↑	Count up
H	L	H	↑	Count down
L	X	X	X	Preset (asynchronous)
H	H	X	X	No change (hold)

H = High logic level, L = Low logic level, X = Don't care,

↑ = Low-to-high clock transition

logic diagram (positive logic)



CY74FCT191T
4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	−0.5 V to 7 V
DC input voltage range	−0.5 V to 7 V
DC output voltage range	−0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	90°C/W
SO package	57°C/W
Ambient temperature range with power applied, T_A	−65°C to 135°C
Storage temperature range, T_{Stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			−32	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	−40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.75\text{ V}$,	$I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
V_{OH}	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -32\text{ mA}$	2			V
	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -15\text{ mA}$	2.4	3.3		
V_{OL}	$V_{CC} = 4.75\text{ V}$,	$I_{OL} = 64\text{ mA}$		0.3	0.55	V
V_H	All inputs			0.2		V
I_I	$V_{CC} = 5.25\text{ V}$,	$V_{IN} = V_{CC}$			5	μA
I_{IH}	$V_{CC} = 5.25\text{ V}$,	$V_{IN} = 2.7\text{ V}$			± 1	μA
I_{IL}	$V_{CC} = 5.25\text{ V}$,	$V_{IN} = 0.5\text{ V}$			± 1	μA
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$,	$V_{OUT} = 0\text{ V}$	-60	-120	-225	mA
I_{off}	$V_{CC} = 0\text{ V}$,	$V_{OUT} = 4.5\text{ V}$			± 1	μA
I_{CC}	$V_{CC} = 5.25\text{ V}$, $V_{IN} \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.1	0.2	mA
ΔI_{CC}	$V_{CC} = 5.25\text{ V}$, $V_{IN} = 3.4\text{ V}^\S$, $f_1 = 0$, Outputs open			0.5	2	mA
$I_{CCD}^\P$	$V_{CC} = 5.25\text{ V}$, One bit switching at 50% duty cycle, Preset mode, Outputs open, $\overline{MR} = V_{CC} = \overline{SR}$, $\overline{PL} = \overline{CE} = \overline{U/D} = \overline{CP} = \text{GND}$, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.06	0.12	mA/MHz
$I_C^\#$	$V_{CC} = 5.25\text{ V}$, Preset mode, Outputs open, $\overline{PL} = \overline{CE} = \overline{U/D} = \overline{CP} = \text{GND}$	One bit switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} = V_{CC}$ or GND	0.4	0.8	mA
			$V_{IN} = 3.4\text{ V}$ or GND	0.7	1.8	mA
		Four bits switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} = V_{CC}$ or GND	1.3	2.6	mA
			$V_{IN} = 3.4\text{ V}$ or GND	2.3	6.6	mA
C_i				5	10	pF
C_0				9	12	pF

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4\text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

CY74FCT191T

4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			CY74FCT191AT		CY74FCT191CT		UNIT
			MIN	MAX	MIN	MAX	
t_w Pulse duration	CP	High or Low	4		4		ns
	$\overline{PL}$ low		5.5		5		
t_{su} Setup time	Data before $\overline{PL}\downarrow$	High or Low	4		3.5		ns
	$\overline{CE}$ before $CP\uparrow$	Low	9		7.2		
	$\overline{U/D}$ before $CP\uparrow$	High or Low	10		8		
t_h Hold time	Data after $\overline{PL}\downarrow$	High or Low	1.5		1		ns
	$\overline{CE}$ after $CP\uparrow$	Low	0		0		
	$\overline{U/D}$ after $CP\uparrow$	High or Low	0		0		
t_{rec} Recovery time	$\overline{PL}$ after $CP\uparrow$		5		4.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT191AT		CY74FCT191CT		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	CP	Q_n	1.5	7.8	1.5	6.2	ns
t_{PHL}			1.5	7.8	1.5	6.2	
t_{PLH}	CP	TC	1.5	11.8	1.5	9.4	ns
t_{PHL}			1.5	11.8	1.5	9.4	
t_{PLH}	CP	$\overline{RC}$	1.5	8.5	1.5	6.8	ns
t_{PHL}			1.5	8.5	1.5	6.8	
t_{PLH}	CE	$\overline{RC}$	1.5	7.2	1.5	6	ns
t_{PHL}			1.5	7.2	1.5	6	
t_{PLH}	$\overline{U/D}$	$\overline{RC}$	1.5	13	1.5	11	ns
t_{PHL}			1.5	13	1.5	11	
t_{PLH}	$\overline{U/D}$	TC	1.5	7.2	1.5	6.1	ns
t_{PHL}			1.5	7.2	1.5	6.1	
t_{PLH}	P_n	Q_n	1.5	9.1	1.5	7.7	ns
t_{PHL}			1.5	9.1	1.5	7.7	
t_{PLH}	$\overline{PL}$	Q_n	2	8.5	2	7.2	ns
t_{PHL}			2	8.5	2	7.2	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT191ATSOC	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191A	Samples
CY74FCT191CTQCT	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT191-3	Samples
CY74FCT191CTSOC	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT191C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



www.ti.com

PACKAGE OPTION ADDENDUM

10-Dec-2020

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

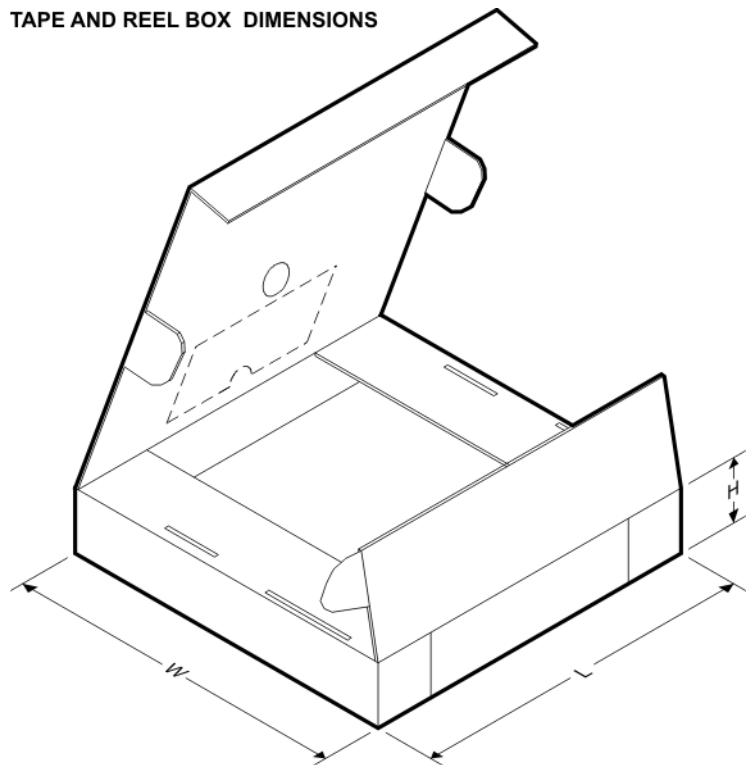
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT191CTQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT191CTQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY74FCT191ATSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6
CY74FCT191CTSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

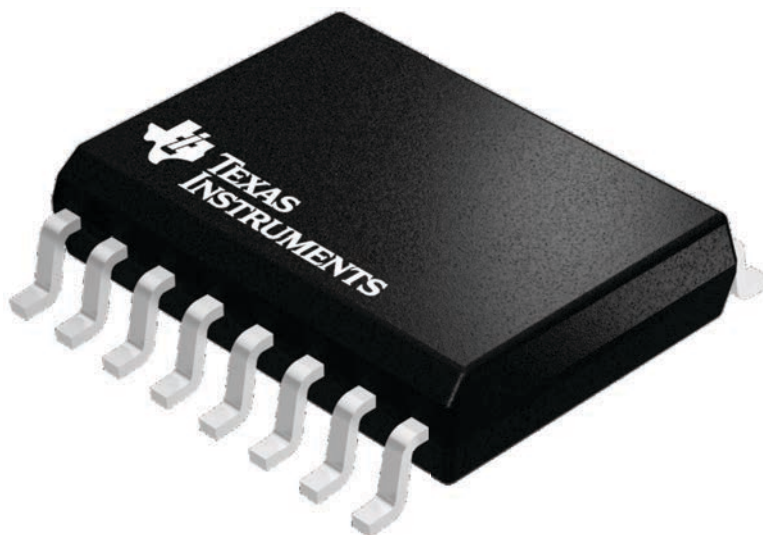
DW 16

SOIC - 2.65 mm max height

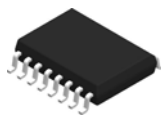
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

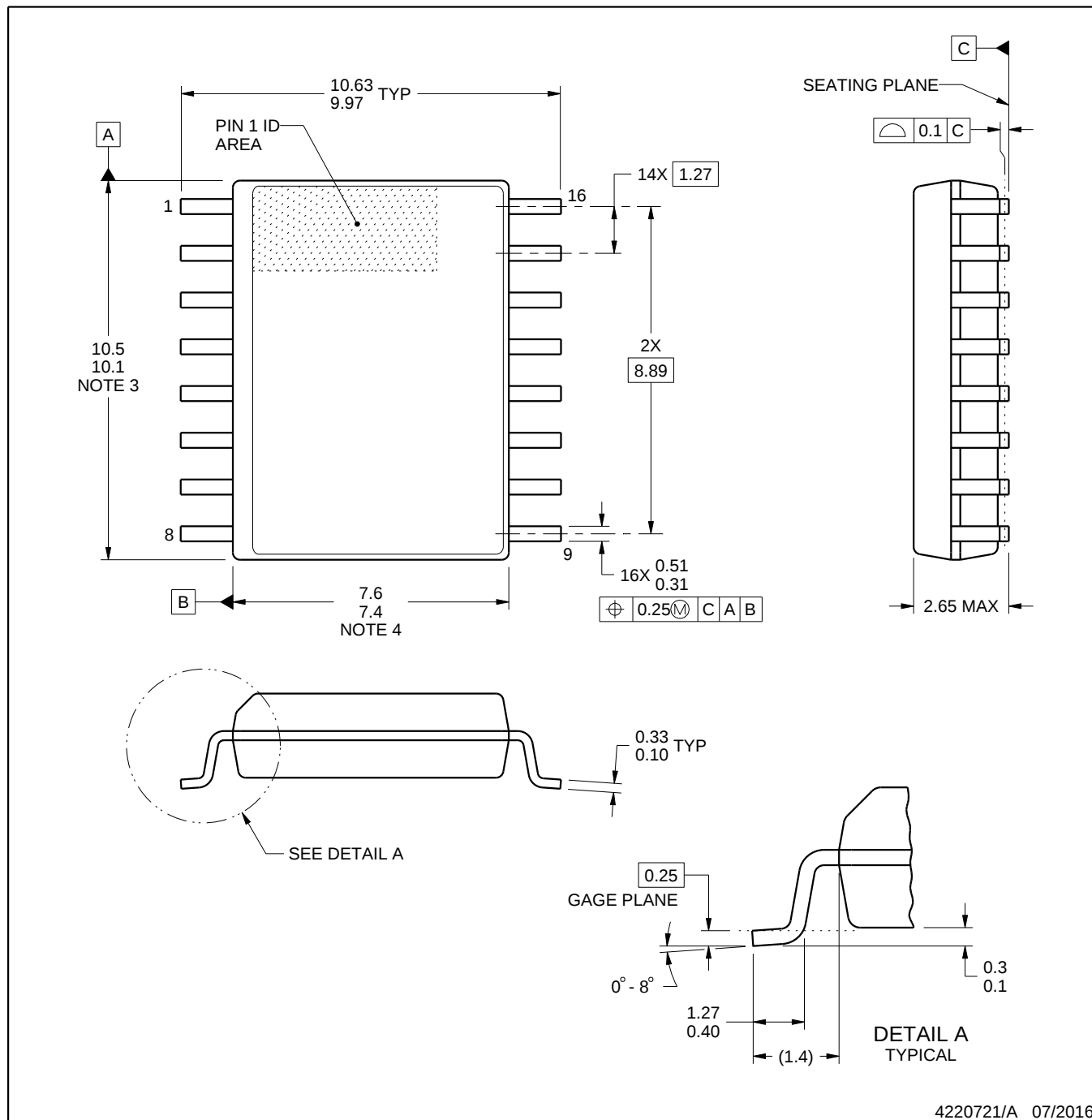


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

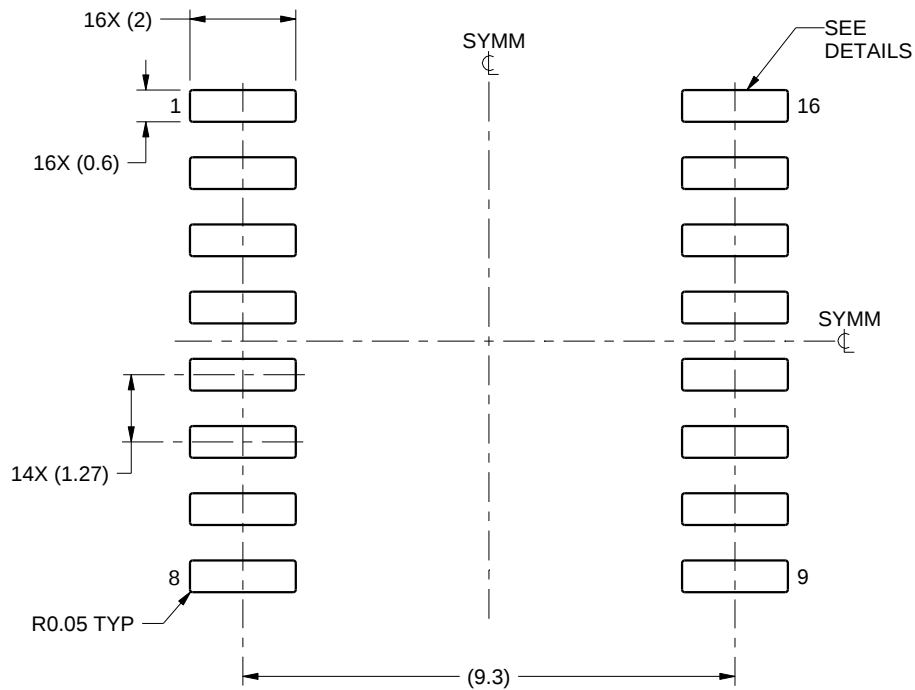
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

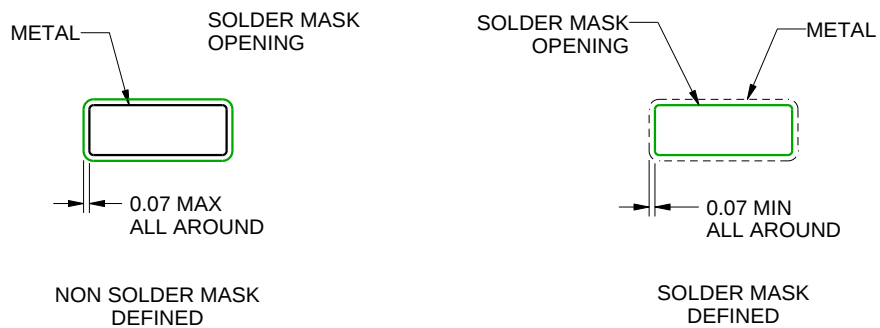
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

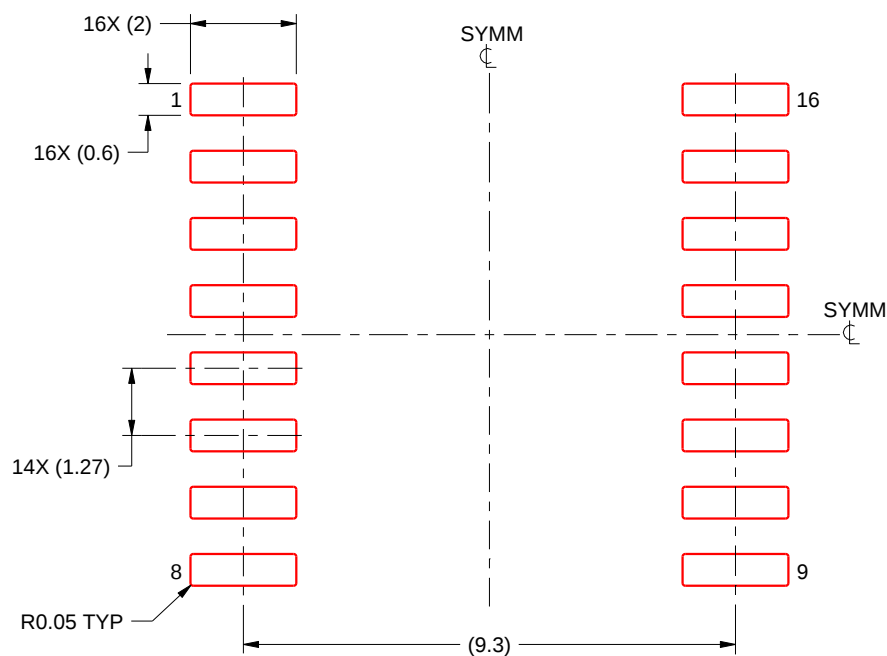
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC

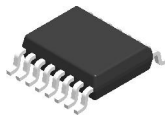


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

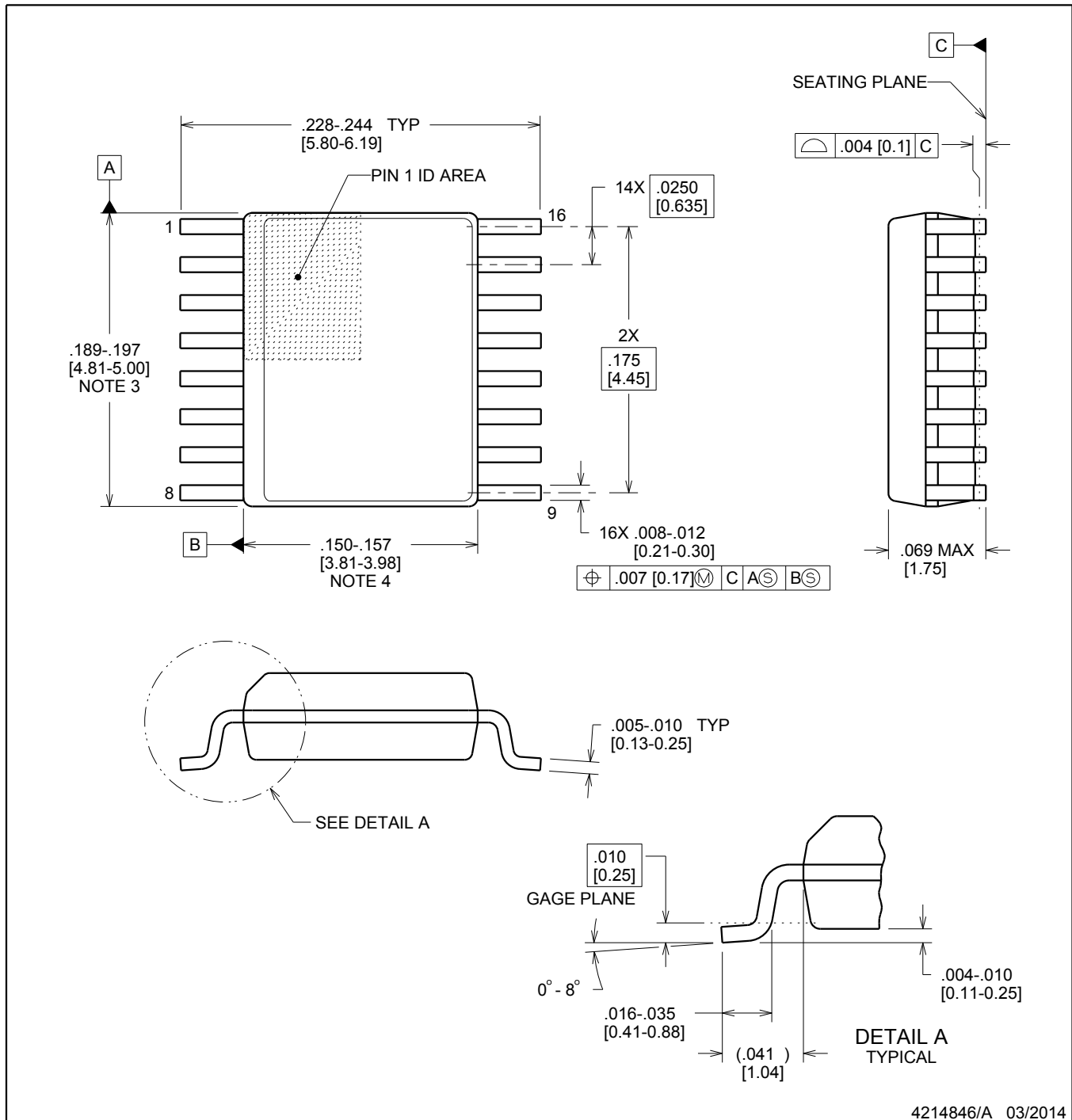


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

NOTES:

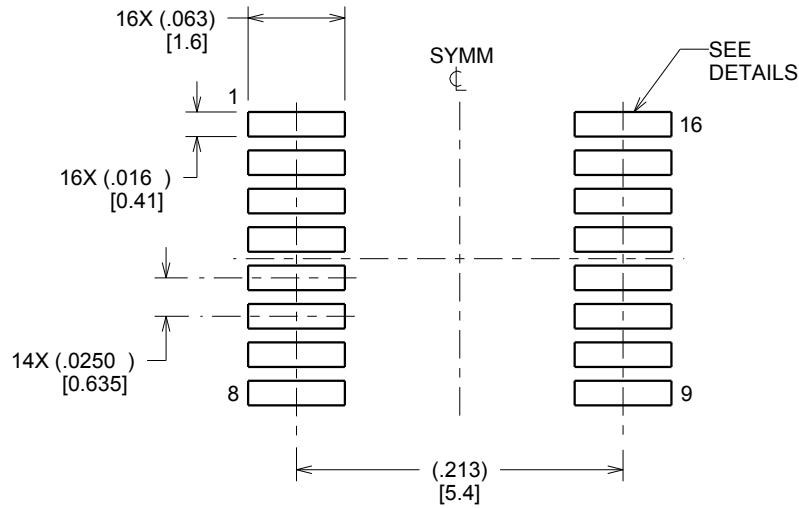
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

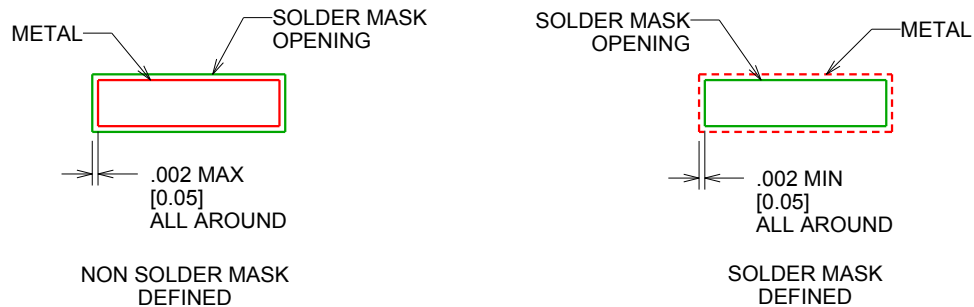
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

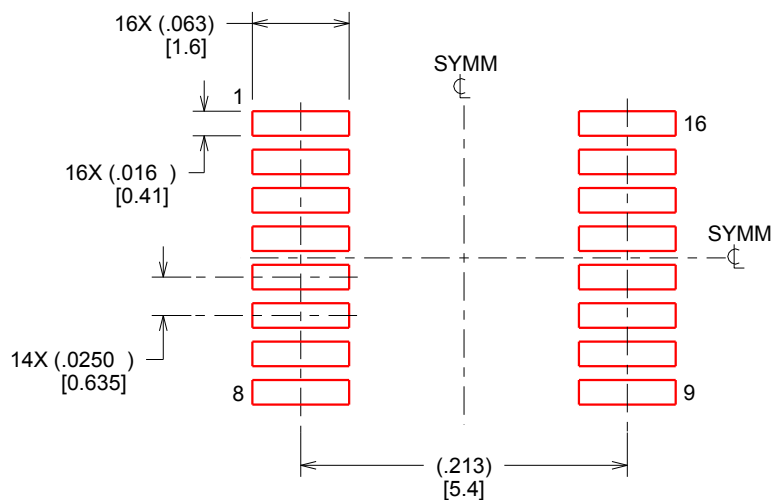
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated