WS4639

Configurable Reset Timer with Integrated Load Switch

Http//:www.sh-willsemi.com

Descriptions

The WS4639 is both a timer for resetting a mobile device and an advanced load management switches for applications requiring a highly integrated solution. Output auto-discharge while the device shutdown made output voltage off quickly. Thermal shutdown function can protect the device and load.

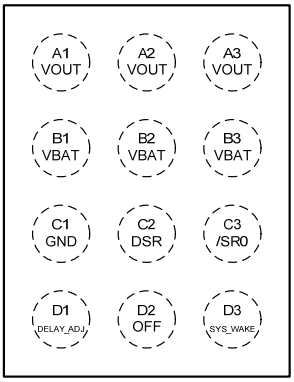
The WS4639 is available in CSP-12L package. Standard product is Pb-free and Halogen-free.

Features

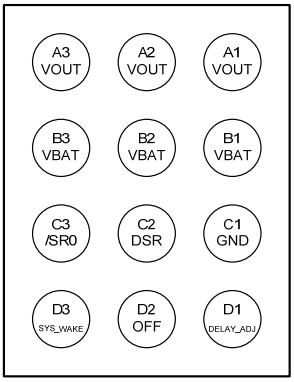
- Input voltage range : 1.8~5.5V
- Main switch R_{ON} : 23mΩ @ V_{BAT}=3.8V, Typ.
- Continue output current :
  3.8A (JEDEC 2S2P, No VIA)
  4.5A (JEDEC 2S2P, Thermal VIA)
- Slew Rate / Inrush Control with t_R: 2.7ms (Typ.)
- Factory Programmed Reset Delay: 7.5s
- Factory Programmed Reset Pulse: 400ms
- Factory Customized Turn-on Time: 2.3s
- Factory Customized Turn-off Delay: 7.3s
- Adjustable Reset Delay Option with External Resistor
- Zero-Second Test-Mode Enable
- Over-Voltage Protection: Allow Input Pins > VBAT

Applications

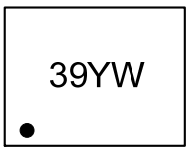
- Smart Phones
- Tablet PCs



(Top View)



(Bottom View)
Pin configuration



39 = Device code
Y = Year code
W = Week code
Marking

Order information

Device	Package	Shipping
WS4639FC-12/TR	CSP-12L (1.16*1.56)	3000/Reel&Tape

Typical Applications

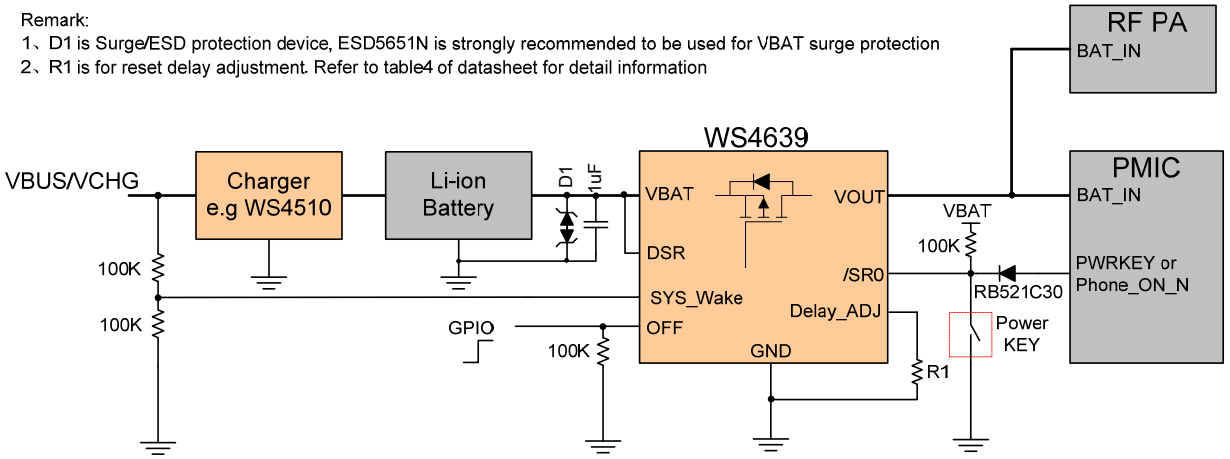
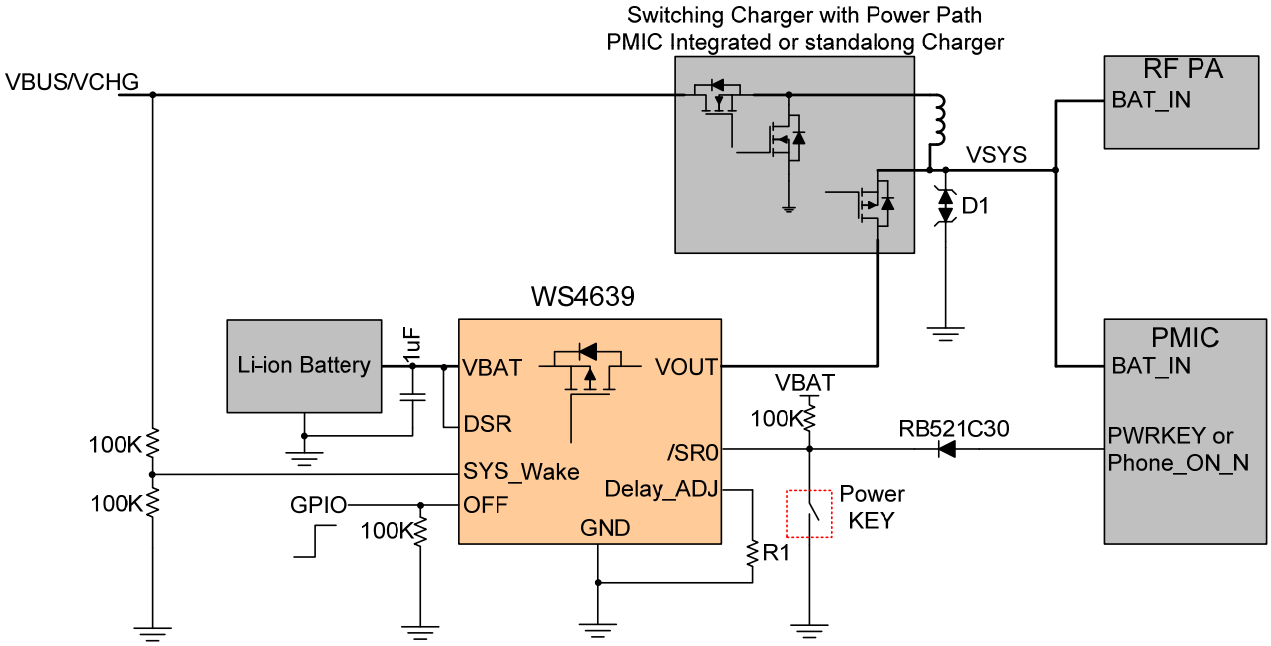


Figure 1. Typical Application without power path system



Remark:
1、D1 is Surge/ESD protection device, ESD5651N is strongly recommended to be used for VBAT surge protection
2、R1 is for reset delay adjustment. Refer to table4 of datasheet for detail information

Figure 2. Typical Application with power path system

Pin Descriptions

Pin Number	Symbol	Descriptions	Zero-Second Factory Test-Mode(1)
A1, A2, A3	VOUT	Switch Output	Switch Output
B1, B2, B3	VBAT	Supply Input	Supply Input
C1	GND	Ground	Ground
C2	DSR	Delay selection input, connected to GPIO with 100KΩ pull-up or to VBAT directly without pull-up resistor	Logic Low Level
C3	/SR0	Power-on or reset input, active LOW	Logic Low Level
D1	DELAY_ADJ	Reset delay adjustment, Must tie to VBAT directly if not used. To adjust the reset delay, a resistor (R_{ADJ}) is connected between this pin and ground	Connect to VBAT or GND
D2	OFF	Load switch disable, Rising Edge Triggered, changes load switch from ON state to OFF state	NA
D3	SYS_WAKE	System wake-up input, changes load switch from OFF state to ON state	NA

Note: (1) Zero-Second Factory Test-Mode applies only to t_{VON} and t_{PHL1}.

Block Diagram

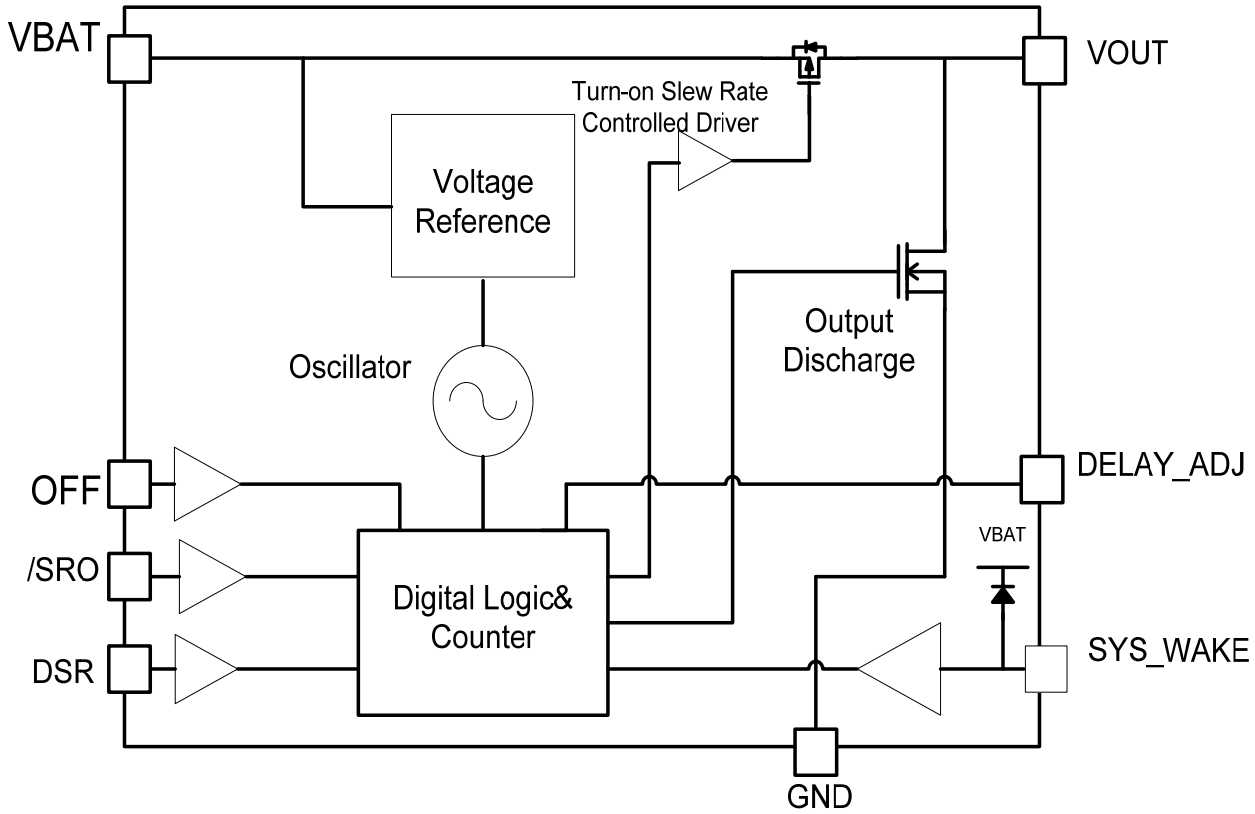


Figure 3. Block Diagram

Absolute maximum ratings

Parameter	Symbol	Value	Unit
VBAT VOUT pin voltage range	V_{BAT} , V_{OUT}	-0.3～6.5	V
Other pin voltage range	V	-0.3~5.5	V
Power Dissipation @25 °C, (I_{OUT} = 4.5A)	P_D	0.34	W
Junction-to-Ambient Thermal Resistance	θ_{JA}	85	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	48	°C/W
Junction temperature	T_J	150	°C
Lead temperature(Soldering, 10s)	T_L	260	°C
Storage temperature	Tstg	-65 ~ 150	°C
VBAT VOUT Pin ESD Ratings	HBM	10000	V
	CDM	2000	V
All other Pins ESD Ratings	HBM	8000	V
	CDM	2000	V

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Recommend Operating Conditions

Parameter	Symbol	Value	Unit
VBAT pin voltage range(1)	V_{BAT}	1.8 ~ 5.5	V
/SR0, DSR, OFF, VOUT pin voltage range	V	0 ~ 5.5	V
SYS_WAKE pin voltage range		0 ~ VBAT	V
Operating ambient temperature	T_A	-40 ~ 85	°C

Note: (1) When input pin have a voltage, ban VBAT float

DC Electronics Characteristics (Ta=25°C, V_{BAT}=4.5V, unless otherwise noted)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
Off Supply Current	I_{OFF}	V_{BAT}=4.5V, V_{OUT}=Open, Load Switch = OFF	Ta=25°C		0.2	1	uA
			Ta=-40~85°C			3	uA
		V_{BAT}=4.5V, V_{OUT}=GND, Load Switch = OFF	Ta=25°C		0.2	1	uA
			Ta=-40~85°C			3	uA
		V_{BAT}=3.8V, V_{OUT}=GND, Load Switch = OFF	Ta=25°C		0.1	1	uA
			Ta=-40~85°C			3	uA
On Resistance	R_{ON}	V_{BAT}=5.5V, I_{OUT}=1A(1)			20	24	mΩ
		V_{BAT}=4.5V, I_{OUT}=1A (1)			21	25	
		V_{BAT}=3.8V, I_{OUT}=500mA(1)			23	28	
		V_{BAT}=3.3V, I_{OUT}=500mA(1)			24	29	
		V_{BAT}=2.5V, I_{OUT}=500mA(1)			28	35	
		V_{BAT}=1.8V, I_{OUT}=250mA(1)			37	45	
Output Discharge $R_{PULL\ DOWN}$	R_{PD}	V_{BAT}=4.5V, V_{OUT}= OFF, I_{FORCE}=20mA			65	85	Ω
Input High Voltage(2)	V_{IH}	1.8V≤V_{BAT}≤5.5V		1.2			V
Input Low Voltage(2)	V_{IL}					0.4	V
Input Leakage Current(2)	I_{IN}	0V≤V_{BAT}≤5.5V				±1	uA
Quiescent Current	I_{CCQ}	/SR0=5.5V, DSR=5.5V, SYS_WAKE=5.5V, OFF =GND, I_{OUT}=0mA, V_{BAT}=5.5V, Load Switch=ON			0.3	3	μA
		/SR0=3.8V, DSR=3.8V, SYS_WAKE=3.8V，OFF=GND，I_{OUT}=0mA, V_{BAT}=3.8V, Load Switch=ON			0.1	3	μA
	I_{CCT}	DSR=OFF=GND, /SR0 = SYS_WAKE=1.2V, V_{BAT}=5.5V, Load Switch=ON			2	6	μA
Dynamic Supply Current	I_{CC}	/SR0=GND, DSR=5.5V, V_{BAT}=5.5V, Load Switch =ON			20	40	μA

AC Electronics Characteristics (Ta=25°C, V_{BAT}=4.5V, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power-On and Reset Timing						
Turn-On Time for V_{OUT}	t_{VON}	C_L=5pF，R_L=5kΩ，DSR= HIGH，Figure 19	1.8	2.3	2.8	s
Timer Delay before Reset	t_{PHL1}	C_L=5pF，R_L=5kΩ，DSR= HIGH，Figure 20	6.0	7.5	9.0	s
Reset Timeout Delay of V_{OUT}	t_{REC1}	C_L=5pF, R_L=5kΩ, Figure 20	320	400	480	ms
Load Switch Turn-On Timing						
Turn-On Delay(3)	t_{DON}	V_{BAT}=4.5V, R_L=5Ω, C_L=100μF, T_A=25°C, Figure 18		1.7		ms
V_{OUT} Rise Time(3)	t_R			2.7		ms
Turn-On Time, SYS_WAKE to V_{OUT}	t_{ON}			4.4		ms
Load Switch Turn-Off with Delay						
Delay to Turn Off Load Switch	t_{SD}	V_{BAT}=4.5V，R_L=150Ω，C_L=100μF, T_A=25°C,DSR= HIGH，Figure 17	5.8	7.3	8.8	s
V_{OUT} Fall Time(3)	t_F			10		ms
Turn-Off(4) (5)	t_{OFF}			7.3		s
Load Switch Zero-Second Turn-Off						
Delay to Turn Off Load Switch	t_{SD}	V_{BAT}=4.5V，R_L=150Ω，C_L=100μF, T_A=25°C,DSR= LOW，Figure 17		0.6		ms
V_{OUT} Fall Time(3)	t_F			10		ms
Turn-Off(4) (5)	t_{OFF}			10.6		ms
Zero-Second Factory Test Mode						
Turn-On Time for V_{OUT}	t_{VON}	C_L=5pF， R_L=5kΩ， V_{OUT}=OFF，DSR=LOW，Figure 19		2		ms
Timer Delay before Reset	t_{PHL1}	C_L=5pF， R_L=5kΩ， V_{OUT}=ON，DSR=LOW，Figure 20		1		ms

Note:

(1) This parameter is guaranteed by design and characterization, RON is tested with different voltage and current conditions in production.

(2) Input pins are /SR0, OFF, DSR, and SYS_WAKE. Input pins should not be floated when VBAT is connected to the power supply.

(3) $t_{ON}=t_R + t_{DON}$.

(4) $t_{OFF}=t_F + t_{SD}$.

(5) Output discharge enabled during off-state.

Typical Characteristics (Ta=25°C, unless otherwise noted)

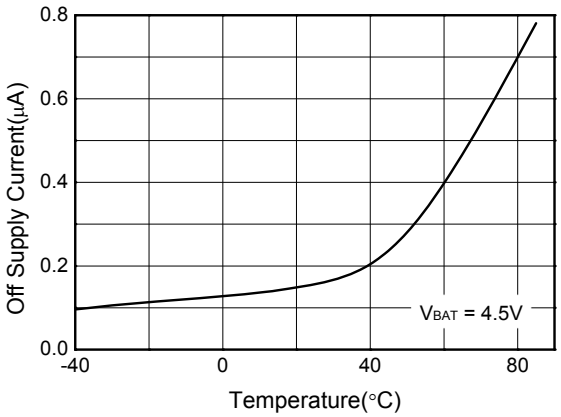


Figure 4. Off Supply Current vs. Temperature

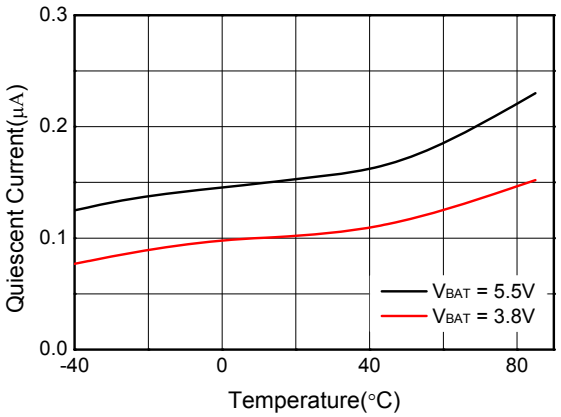


Figure 5. Quiescent Current vs. Temperature

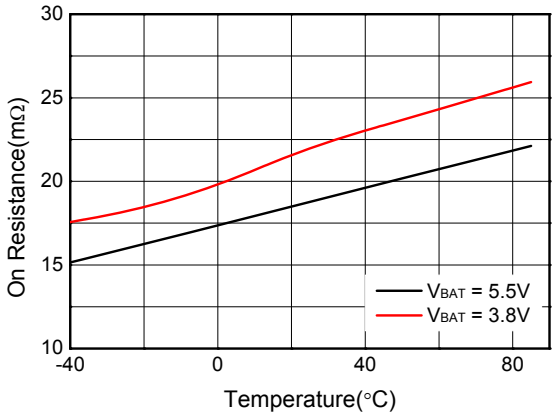


Figure 6. R_{ON} vs. Temperature

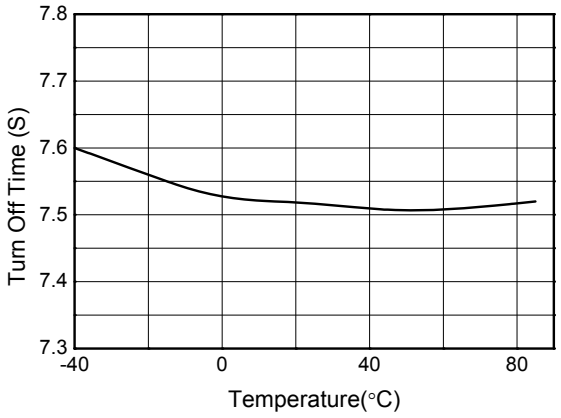


Figure 7. t_{OFF} vs. Temperature

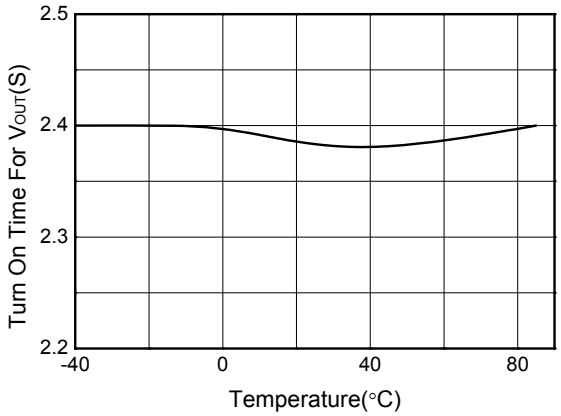


Figure 8. t_{VON} vs. Temperature

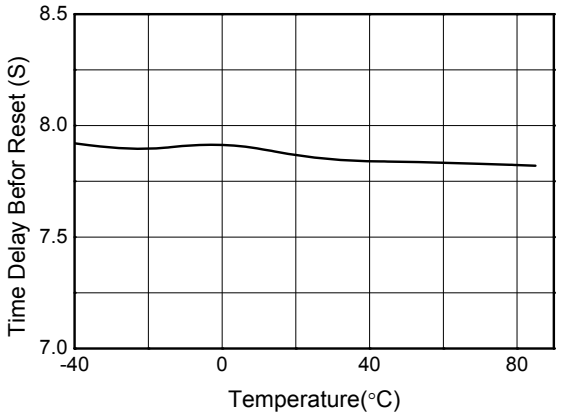


Figure 9. t_{PHL1} vs. Temperature

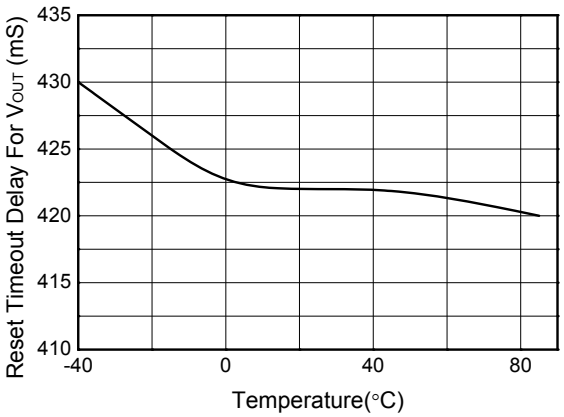


Figure 10. t_{REC1} vs. Temperature

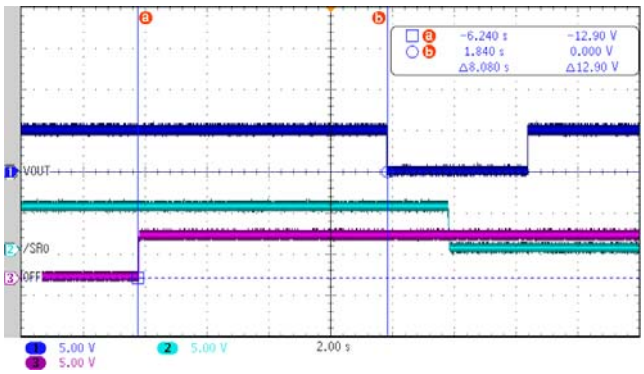


Figure 11. t_{OFF}

(/SR0=5V,Vbat=DSR=5V,OFF=SYS_WAKE=GND)

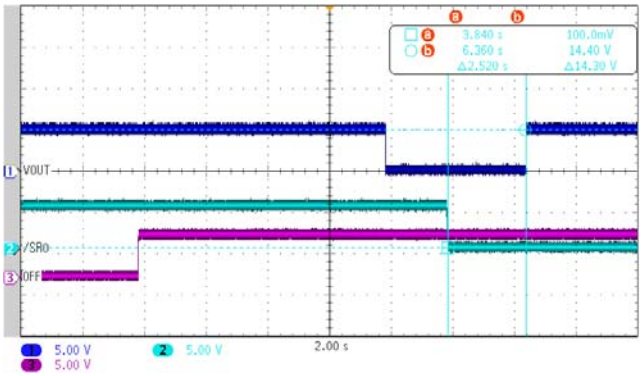


Figure 12. t_{VON}

(/SR0=5V,Vbat=DSR=5V,OFF=SYS_WAKE=GND)

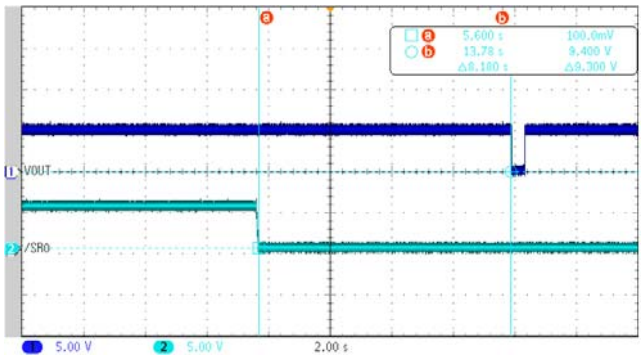


Figure 13. t_{PHL1}

(/SR0=5V,Vbat=DSR=5V,OFF=SYS_WAKE=GND)

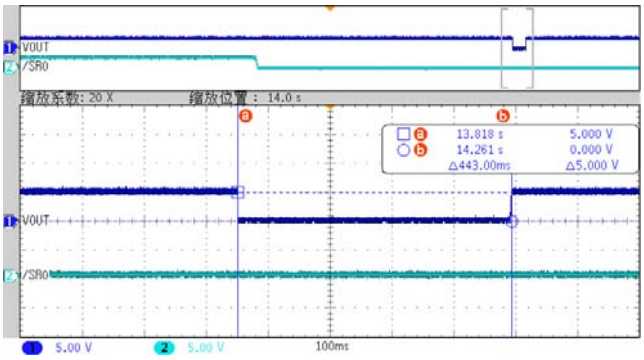


Figure 14. t_{REC1}

(/SR0=5V,Vbat=DSR=5V,OFF=SYS_WAKE=GND)

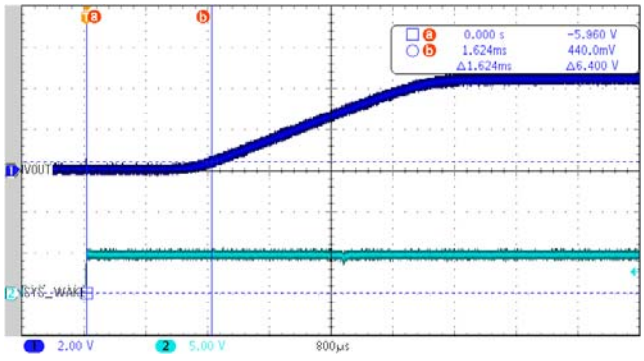


Figure 15. t_{DON}

(Cl=100uF,Rl=5ohm,Vbat=/SR0=DSR=4.5V,OFF=SYS_WAKE=0V)

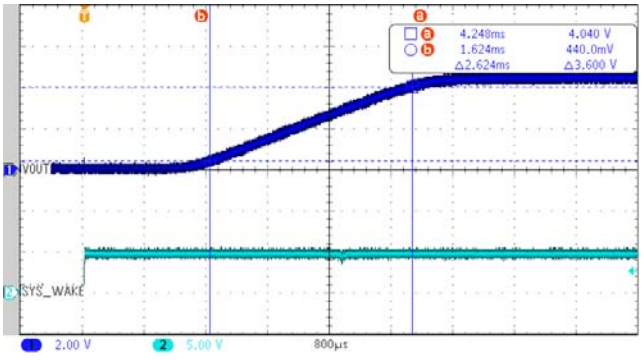


Figure 16. t_{R}

(Cl=100uF,Rl=5ohm,Vbat=/SR0=DSR=4.5V,OFF=SYS_WAKE=0V)

Application Information

Reset Timer and Advanced Load Management

The WS4639 is both a reset IC and an advanced load management device. A typical application is shown in Figure 1.

Disconnect PMIC from Battery (Turn Off)

After holding the DSR pin HIGH, changing the OFF pin from LOW to HIGH (rising edge triggered) and holding it HIGH for at least 1ms, the WS4639 triggers an internal counter to allow a factory- customized 7.3s delay before turning off internal load switch. The delay is intended to allow the PMIC to complete a power-down sequence before safely disconnecting from the power supply. However, the turn-off sequence is terminated if a higher priority input is detected in t_{SD} period (see Resolving Input Conflicts).

Alternatively, after holding the DSR pin LOW, changing the OFF pin from LOW to HIGH (rising edge triggered) and holding it HIGH for at least 1ms, the WS4639 triggers the zero-second turn-off. Delay t_{SD} is significantly reduced to 0.6ms to avoid the default delay to turn-off load switch (t_{SD}).

With its stringent shutdown current flow, the WS4639 significantly reduces the current drain on a battery when the PMIC is turned off. This preserves the battery power for a longer period when a mobile device is in Shutdown Mode.

Power On

There are two methods to turn on the load switch to wake up the PMIC. When a HIGH is inserted to the SYS_WAKE pin or when /SR0 is held LOW for > 2.3s (see Figure 19), the WS4639 turns on its load switch to allow PMIC to connect to the battery. The reset feature is disabled when V_{OUT} is toggled from OFF to ON. Continuously holding /SR0 LOW do not trigger a reset event. To enable the reset feature, /SR0 must return to HIGH such that WS4639 resets its internal counter.

Reset Timer

During normal operation of a mobile device, if a reset operation is needed for mobile equipment holding the power switch, to which /SR0 is connected and is forced LOW, for at least 7.5s, causes the WS4639 to cut off the supply power to PMIC for 400ms by turning off the load switch. The WS4639 then automatically turns on the load switch to reconnect the PMIC to battery. This forces PMIC to enter a power-on sequence. If the power switch is released and /SR0 is returned to HIGH within 7.5s, the WS4639 resets its counter and VOUT remains in ON state, there is no change on VOUT and a reset does not occur.

Power-On Reset

When WS4639 is connected to a battery (VBAT $\geqslant$ 1.8V), the part enters Power-On Reset (POR) Mode. All internal registers are reset and V_{OUT} is ON at the end of POR sequence (see Table 2).

Zero-Second Factory Test Mode

WS4639 includes a Zero-Second Factory Test Mode to shorten the turn-on time for V_{OUT} (t_{VON}) and timer delay before reset (t_{PHL1}) for factory testing. When V_{OUT} is OFF, the default turn-on time (t_{VON}) is 2.3s. If the DSR pin is LOW prior to /SR0 going LOW, the WS4639 bypasses the 2.3s delay and V_{OUT} changes from OFF to ON immediately. Similarly, default reset delay (t_{PHL1}) is 7.5s. If V_{OUT} is ON and the DSR pin is LOW prior to /SR0 going LOW, the IC enters Zero-Second Factory Test Mode and bypasses the default reset delay of 7.5s, V_{OUT} is pulled from ON to OFF immediately. The reset pulse (t_{REC1}) remains at 400ms in Zero-Second Factory Test Mode. DSR should never be left floating during normal operation.

Table 1. V_{OUT} and Input Conditions

Function	Initial Conditions (t=0 Second)				Associated Delay	V_{OUT}	
	/SR0	SYS_WAKE	OFF	DSR		Before	After
Power-On	LOW	X	X	LOW	t_{VON} <4ms	OFF	ON
	LOW	X	X	HIGH	t_{VON} =2.3s	OFF	ON
	HIGH	HIGH	X	X	t_{ON} =4.4ms	OFF	ON
Reset Function	LOW	X	X	LOW	t_{PHL1}<1ms t_{REC1}=400ms	ON	⊓⊓
	LOW	X	X	HIGH	t_{PHL1}=7.5s (2) t_{REC1}=400ms	ON	⊓⊓
Turn Off	HIGH	LOW	⌐ (1)	LOW	t_{SD} <1ms	ON	OFF
	HIGH	LOW	⌐	HIGH	t_{SD}=7.3s	ON	OFF

Note:

(1) X=Don't Care, ⌐ = Rising Edge, ⊓⊓ =HIGH to LOW to HIGH.

(2) Reset delay (t_{PHL1}) is adjustable (see Table 4).

Table 2. Pin Condition after POR

Pin Name	/SR0	DSR	SYS_WAKE	OFF	VOUT
Default State (after POR)	1	1	0	0	ON

Note:

(1) 1=Input Logic HIGH, 0=Input Logic LOW, ON=load switch is ON state.

Timing Diagrams

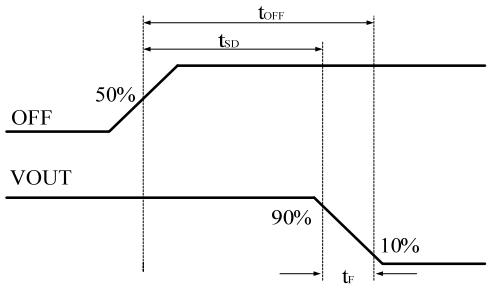


Figure 17. OFF vs. V_{OUT}

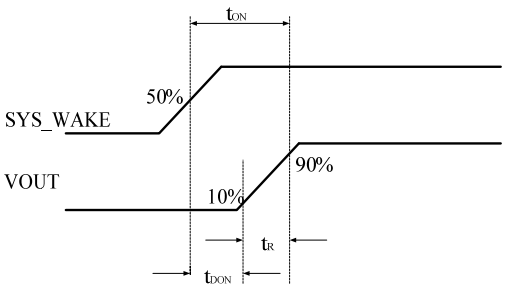


Figure 18. SYS_WAKE vs. V_{OUT}

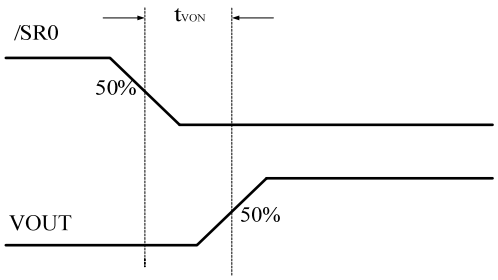


Figure 19. /SR0 Power On

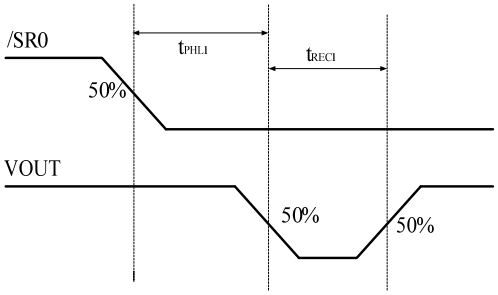


Figure 20. Reset Timing

Resolving Input Conflicts

The WS4639 allows multiple simultaneous inputs and can resolve conflicts based on priority level (see Table 3). When two input pins are triggered at the same time, only the higher priority input is served and the lower priority input is ignored. The lower-priority signal must be repeated to be serviced.

Table 3. Input Priority

Input	Priority (1=Highest)
/SR0	1
SYS_WAKE	2
OFF	3

Special Note on OFF Pin

In the t_{SD} period (DSR=HIGH only, see Figure 17), if /SR0 or SYS_WAKE is triggered when $0 < t < t_{SD}$, the WS4639 exits the turn-off sequence and V_{OUT} remains in ON state. The higher priority input is served regardless of the condition of OFF pin.

To re-initiate the turn-off sequence, the OFF pins must return to LOW, and then toggle from LOW to HIGH again. The same input priority applies (Table 3) if DSR = HIGH.

Special Note on SYS_WAKE Pin

The SYS_WAKE pin is designed and characterized to handle high voltage input at least 20V. Therefore, in application, a current-limiting resistor (i.e 100kΩ) is required between SYS_WAKE and the input signal regardless of input voltage.

Adjustable Reset Delay with an External Resistor and DSR

The reset delay is adjustable by connecting a commonly available, low-power, ±5%, RoHS-compliant resistor between the DELAY_ADJ pin and the GND pin (see Table 4). To disable the adjustable delay feature, DELAY_ADJ should be tied to VBAT directly. The reset delay is factory programmed at 7.5s. The additional power consumption caused by using an external resistor is negligible. The external resistor is normally disconnected and is enabled for milliseconds when /SR0 is pulled LOW.

This external adjustment feature provides a simple alternate method for controlling delay time for engineering and production at customer's location. WILL can also factory program a wide range of turn-on times for V_{OUT} (t_{VON}), timer delay before reset (t_{PHL1}), reset timeout delay for V_{OUT} (t_{REC1}), and load switch turn-off time (t_{OFF}) to match customer applications. In this case, the external resistor (R_{ADJ}) can be eliminated.

Table 4. Delay Adjustment vs. External Resistor

External Resistor R_{ADJ} (kΩ)	Delay Multiplier	Adjusted Reset Delay t_{PHL1_ADJ}, (Seconds) ±20%
Tie to GND (No Resistor)	0.50 x t_{PHL1}	3.8
3.9	0.75 x t_{PHL1}	5.6
10	1.25 x t_{PHL1}	9.4
22	1.50 x t_{PHL1}	11.3
47	1.75 x t_{PHL1}	13.1
120	2.00 x t_{PHL1}	15
Tie to VBAT (No Resistor)	1.00 x t_{PHL1}	7.5

Inside Load Switch Instruction

Input Capacitor

The chip inside the reset timer doesn't require an input capacitor. To reduce device inrush current, a 0.1μF ceramic capacitor, C_{IN}, is recommended close to the V_{BAT} pin. A higher value of C_{IN} can be used to reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

While the load switch works without an output capacitor, if parasitic board inductance forces V_{OUT} below GND when switching off, a 0.1μF capacitor, C_{OUT}, should be placed between V_{OUT} and GND.

Fall Time

Device output fall time can be calculated based on the RC constant of the external components, as:

$$T_F = R_L \times C_L \times 2.2 \quad (1)$$

Where t_F is 90% to 10% fall time, RL is output load, and C_L is output capacitor.

The same equation works for a device with a pull-down output resistor. R_L is replaced by a parallel connected pull-down and an external output resistor combination, calculated as:

$$t_F = \frac{R_L \times R_{PD}}{R_L + R_{PD}} \times C_L \times 2.2 \quad (2)$$

Where t_F is 90% to 10% fall time, RL is output load, R_{PD}=65Ω is output pull-down resistor, and C_L is the output capacitor.

Resistive Output Load

If resistive output load is missing, the chip without a pull-down output resistor does not discharge the output voltage. Output voltage drop depends, in that case, mainly on external device leaks.

Application Specifics

At maximum operational voltage (V_{BAT}=5.5V), device inrush current might be higher than expected. Spike current should be taken into account if V_{BAT}>5V and the output capacitor is much larger than the input capacitor. Input current I_{BAT} can be calculated as:

$$I_{BAT}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + (C_{LOAD} - C_{IN}) \frac{dV_{OUT}(t)}{dt} \quad (3)$$

Where switch and wire resistances are neglected and capacitors are assumed ideal.

Estimating $V_{OUT}(t)=V_{BAT}/10$ and using experimental formula for slew rate ($dV_{OUT}(t)/dt$), spike current can be written as:

$$max(I_{BAT}) = \frac{V_{BAT}}{10R_{LOAD}} + (C_{LOAD} - C_{IN})(0.05V_{BAT} - 0.255) \quad (4)$$

Where supply voltage VBAT is in volts, capacitances are in micro farads, and resistance is in ohms.

Example: If V_{BAT}=5.5V, C_{LOAD}=100μF, C_{IN}=10μF, and R_{LOAD}=50Ω, calculate the spike current by:

$$\max(IBAT) = \frac{5.5}{10 \times 50} + (100 - 10)(0.05 \times 5.5 - 0.2555)A = 1.8A$$

Maximum spike current is 1.8A, while average ramp-up current is:

$$IBAT(t) \approx \frac{VOUT(t)}{RLOAD} + (CLOAD - CIN) \frac{dVBAT(t)}{dt}$$
$$\approx 2.75/50 + 100 \times 0.0022 = 0.275A$$

Output Discharge

The device contains a R_{PD}=65Ω on-chip pull-down resistor for quick output discharge. The resistor is activated when the switch is turned off.

Recommended Layout

For best thermal performance and minimal inductance and parasitic effects, keeping the input and output traces short and capacitors as close to the device as possible is recommended. Additional recommended layout considerations include:

- A1, A2, and A3 are interconnected at PCB, as close to the landing pad as possible.
- B1, B2, and B3 are interconnected at PCB, as close to the landing pad as possible.
- C1 (GND) is connected to GND plane of PCB.
- Reserve a pad for capacitor connection (C1) between V_{BAT} and GND, if no input capacitor is planned.
- Reserve a pad for capacitor connection (C2) between V_{OUT} and GND, if no output capacitor is planned.
- Use a dedicated V_{OUT} or V_{BAT} plane to improve thermal dissipation.

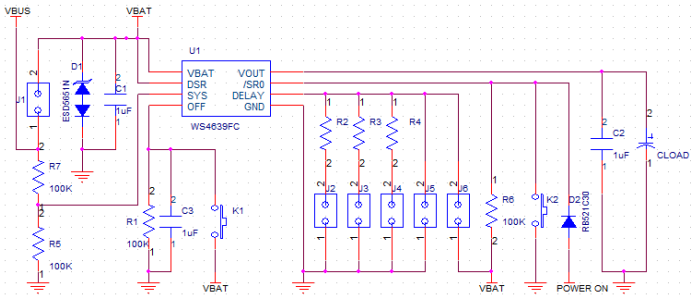


Figure 21. Demo Schematic

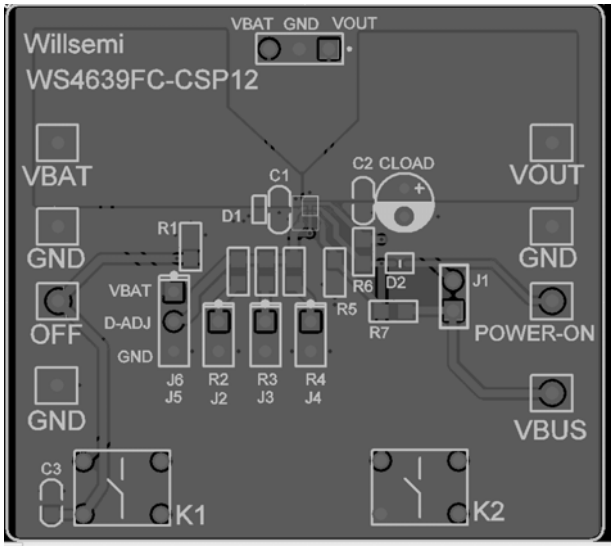


Figure 22. Demo Board Layout (TOP View)

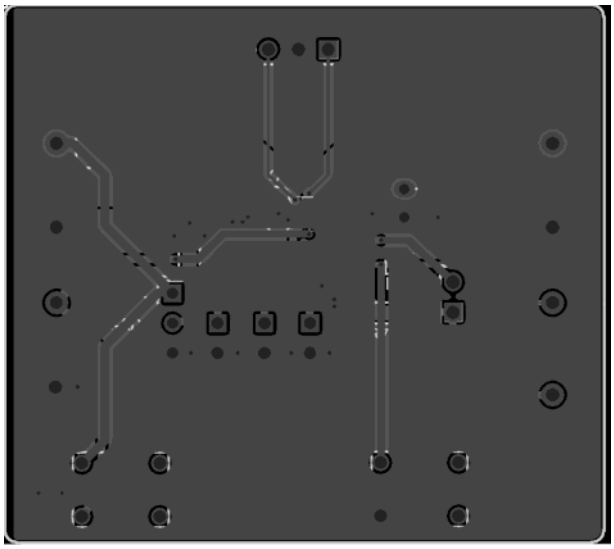
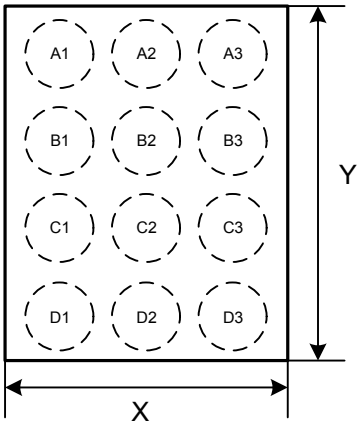


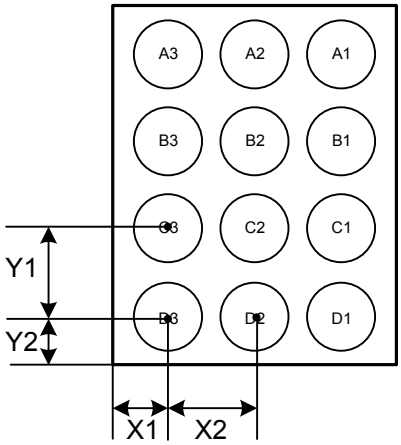
Figure 23. Demo Board Layout (Bottom View)

Package Information

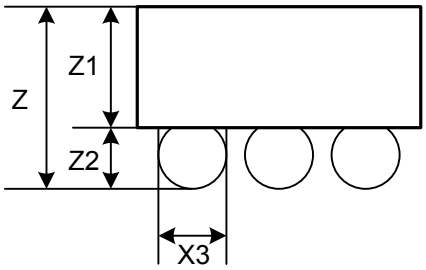
CSP-12L



Top View



Bottom View



Side View

Symbol	Dimensions in millimeter		
	Min.	Typ.	Max.
X	1.150	1.160	1.170
Y	1.550	1.560	1.570
X1		0.180	
X2		0.400	
X3	0.260	0.270	0.280
Y1		0.400	
Y2		0.180	
Z	0.560	0.570	0.580
Z1		0.380	
Z2	0.180	0.190	0.200