

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

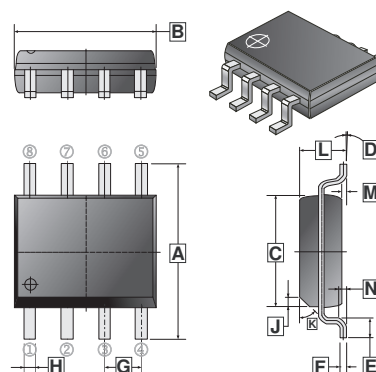
FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8 saves board space.
- Fast Switch Speed.
- High performance trench technology.

APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

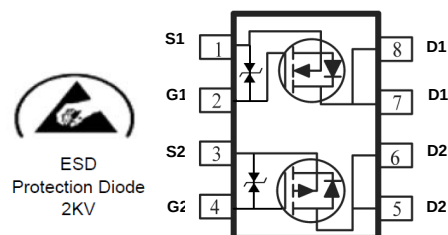
SOP-8



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	H	0.35	0.49
B	4.80	5.00	J	0.375	REF.
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.40	0.90	M	0.10	0.25
F	0.19	0.25	N	0.25	REF.
G	1.27	TYP.			

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	2.5K	13 inch



MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter		Symbol	Ratings		Unit
			N-Ch	P-Ch	
Drain-Source Voltage		V _{DS}	30	-30	V
Gate-Source Voltage		V _{GS}	±20	±20	V
Continuous Drain Current ¹	T _A =25°C	I _D	6.9	-5.2	A
	T _A =70°C		5.4	-6.8	A
Pulsed Drain Current ²		I _{DM}	20	-20	A
Continuous Source Current (Diode Conduction) ¹		I _S	1.3	-1.3	A
Total Power Dissipation ¹	T _A =25°C	P _D	2.1	2.1	W
	T _A =70°C		1.3	1.3	W
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55~150		°C
Thermal Resistance Ratings					
Maximum Junction-ambient ¹	t<=5 sec	R _{θJA}	60		°C / W
Maximum Junction-Case ¹	t<=5 sec	R _{θJC}	40		°C / W

Notes :

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature

N-CHANNEL ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate Threshold Voltage	$V_{GS(th)}$	1	-	-	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=8\text{V}$, $V_{DS}=0$
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	$V_{DS}=24\text{V}$, $V_{GS}=0$
On-State Drain Current ¹	$I_{D(ON)}$	20	-	-	A	$V_{DS}=5\text{V}$, $V_{GS}=10\text{V}$
Static Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	31	m Ω	$V_{GS}=10\text{V}$, $I_D=6.9\text{A}$
		-	-	40		$V_{GS}=4.5\text{V}$, $I_D=6\text{A}$
Forward Transconductance ¹	g_{fs}	-	25	-	S	$V_{DS}=15\text{V}$, $I_D=6.9\text{A}$
Dynamic						
Total Gate Charge	Q_g	-	4.0	-	nC	$I_D=6.9\text{A}$ $V_{DS}=15\text{V}$ $V_{GS}=10\text{V}$
Gate-Source Charge	Q_{gs}	-	1.1	-		
Gate-Drain ("Miller") Charge	Q_{gd}	-	1.4	-		
Turn-on Delay Time	$T_{d(on)}$	-	8	-	nS	$V_{DD}=15\text{V}$ $V_{GS}=10\text{V}$ $I_D=1\text{A}$ $R_{GEN}=6\Omega$
Rise Time	T_r	-	5	-		
Turn-off Delay Time	$T_{d(off)}$	-	23	-		
Fall Time	T_f	-	3	-		

Notes:

1. Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.

P-CHANNEL ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	$V_{DS}=V_{GS}$, $I_D = -250\mu\text{A}$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS} = -8\text{V}$, $V_{DS}=0$
Drain-Source Leakage Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -24\text{V}$, $V_{GS}=0$
On-State Drain Current ¹	$I_{D(ON)}$	-20	-	-	A	$V_{DS} = -5\text{V}$, $V_{GS} = -10\text{V}$
Static Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	52	m Ω	$V_{GS} = -10\text{V}$, $I_D = -5.2\text{A}$
		-	-	80		$V_{GS} = -4.5\text{V}$, $I_D = -4.2\text{A}$
Forward Transconductance ¹	g_{fs}	-	10	-	S	$V_{DS} = -15\text{V}$, $I_D = -5.2\text{A}$
Dynamic						
Total Gate Charge	Q_g	-	10	-	nC	$I_D = -5.2\text{A}$ $V_{DS} = -15\text{V}$ $V_{GS} = -10\text{V}$
Gate-Source Charge	Q_{gs}	-	2.2	-		
Gate-Drain ("Miller") Charge	Q_{gd}	-	1.7	-		
Turn-on Delay Time	$T_{d(on)}$	-	10	-	nS	$V_{DD} = -15\text{V}$ $V_{GS} = -10\text{V}$ $I_D = -1\text{A}$ $R_{GEN}=6\Omega$
Rise Time	T_r	-	2.8	-		
Turn-off Delay Time	$T_{d(off)}$	-	53.6	-		
Fall Time	T_f	-	46	-		

Notes:

1. Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.

CHARACTERISTIC CURVE (N-Ch)

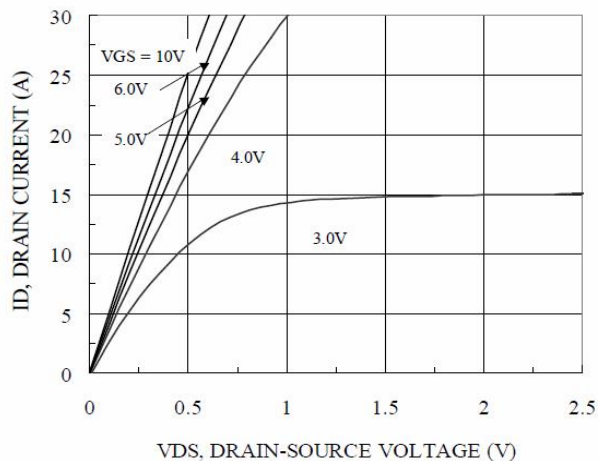


Figure 1. On-Region Characteristics

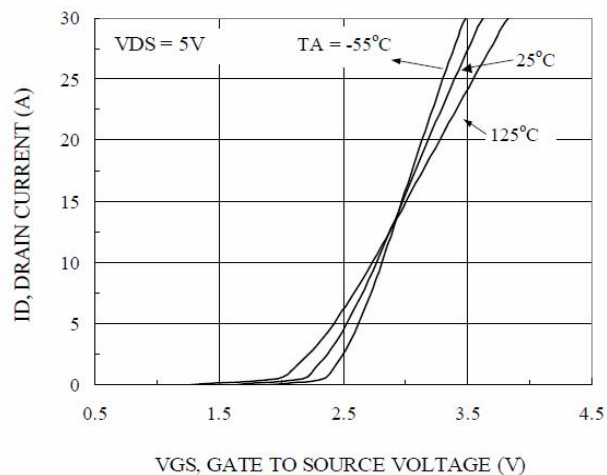


Figure 2. Body Diode Forward Voltage Variation with Source Current and Temperature

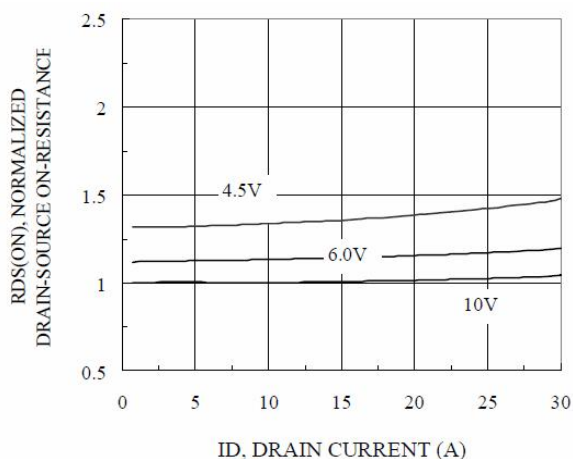


Figure 3. On Resistance Vs Vgs Voltage

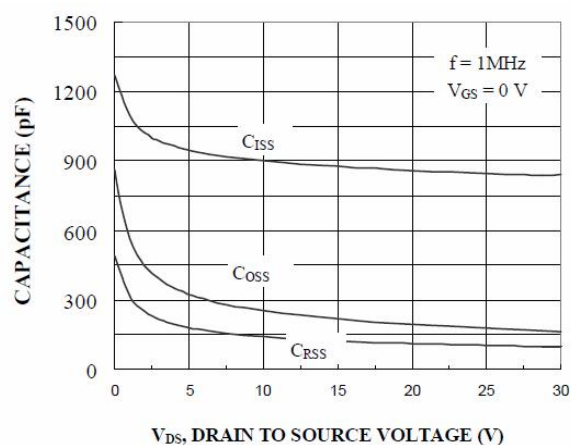


Figure 4. Capacitance Characteristics

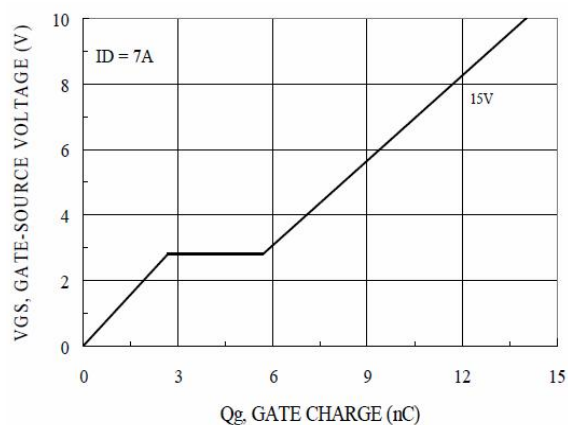


Figure 5. Gate Charge Characteristics

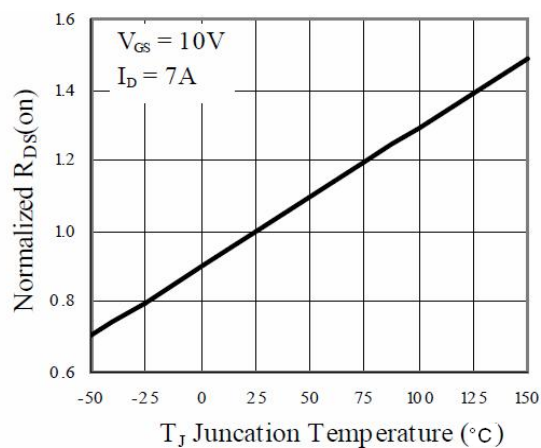


Figure 6. On-Resistance Variation with Temperature

CHARACTERISTIC CURVE (N-Ch)

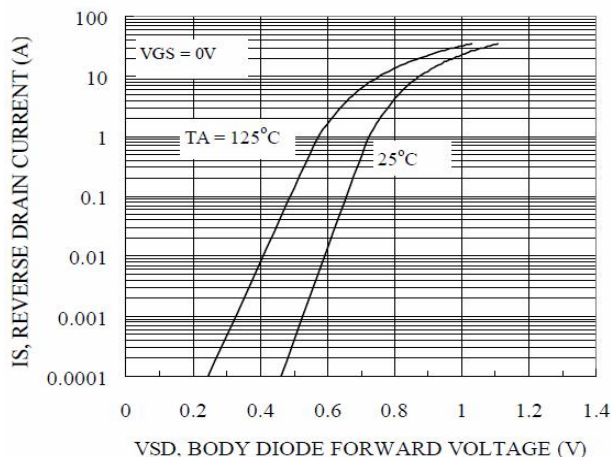


Figure 7. Transfer Characteristics

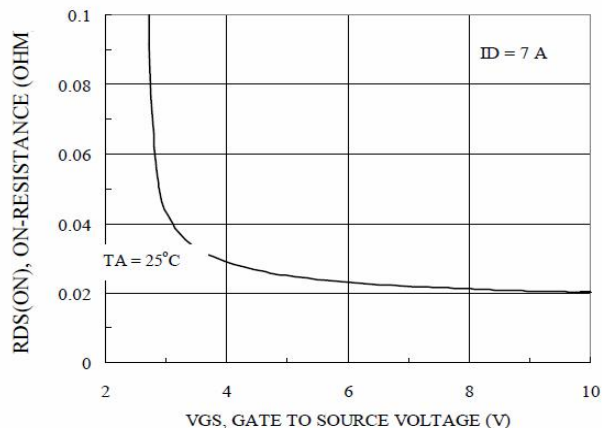


Figure 8. On-Resistance with Gate to Source Voltage

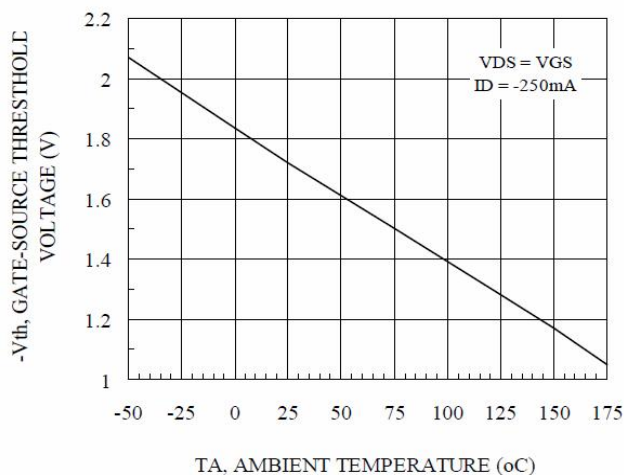


Figure 9. Vth Gate to Source Voltage Vs Temperature

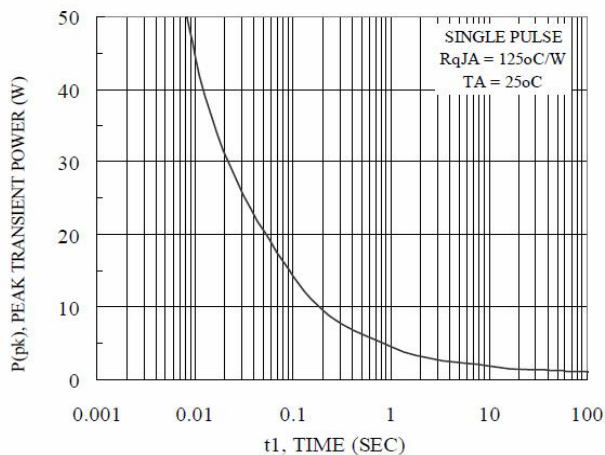


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

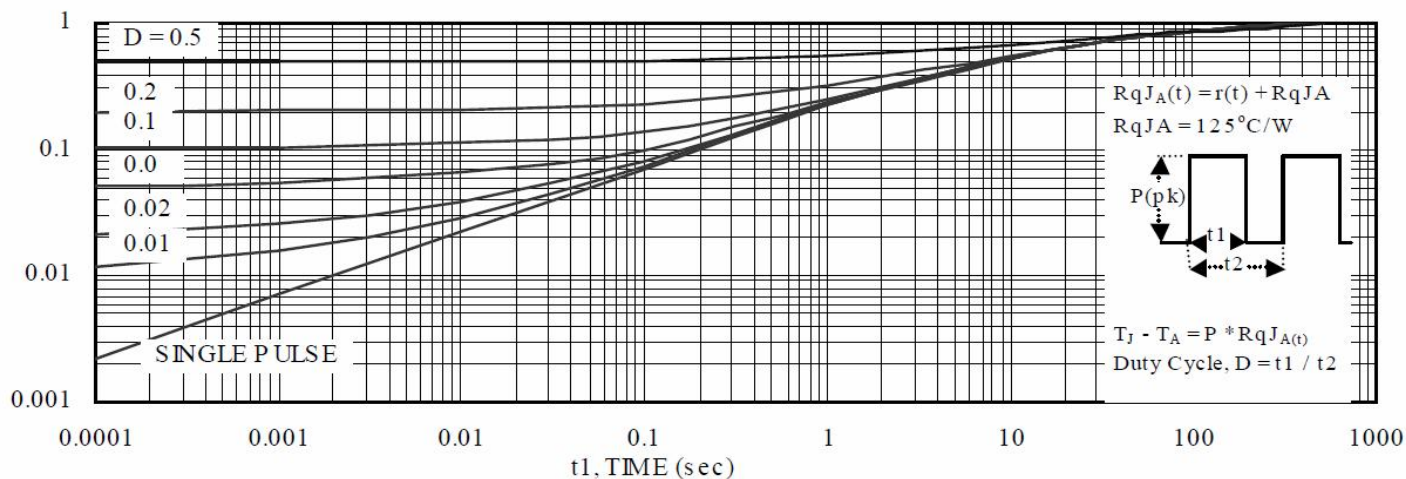


Figure 11. Transient Thermal Response Curve

CHARACTERISTIC CURVE (P-Ch)

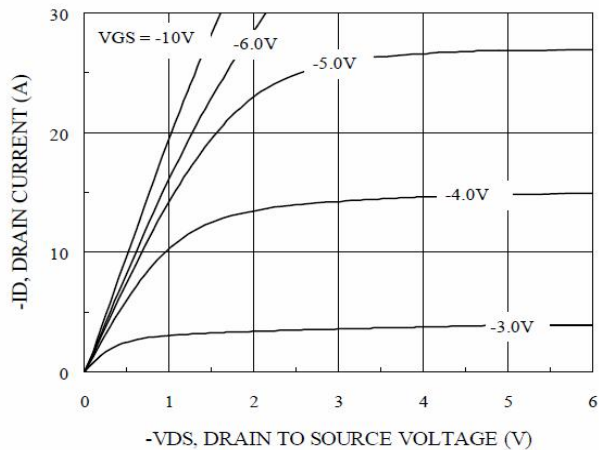


Figure 1. On-Region Characteristics

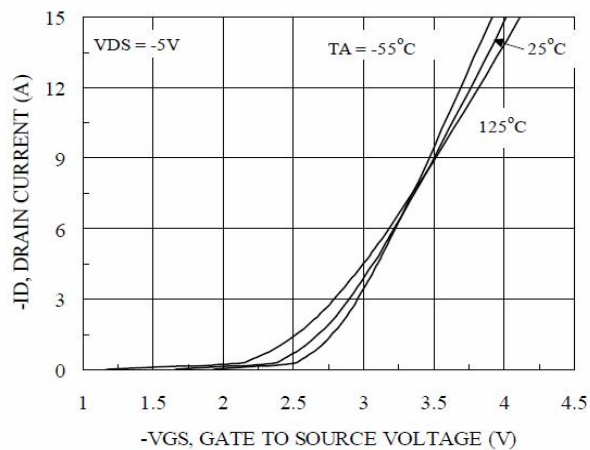


Figure 2. Body Diode Forward Voltage Variation with Source Current and Temperature

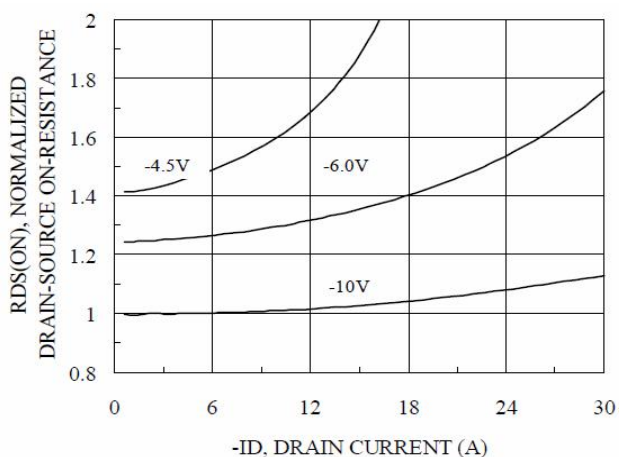


Figure 3. On Resistance Vs Vgs Voltage

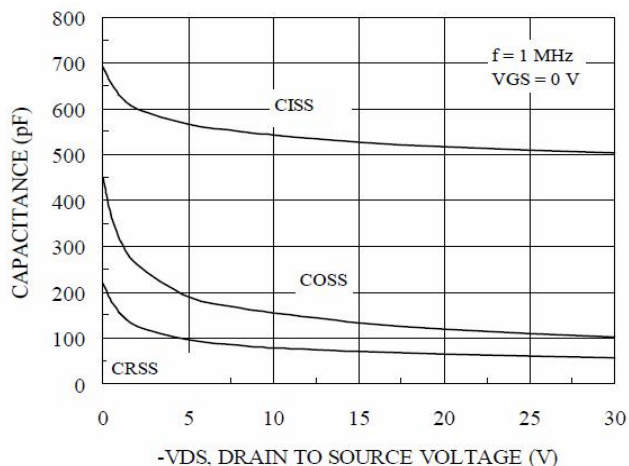


Figure 4. Capacitance Characteristics

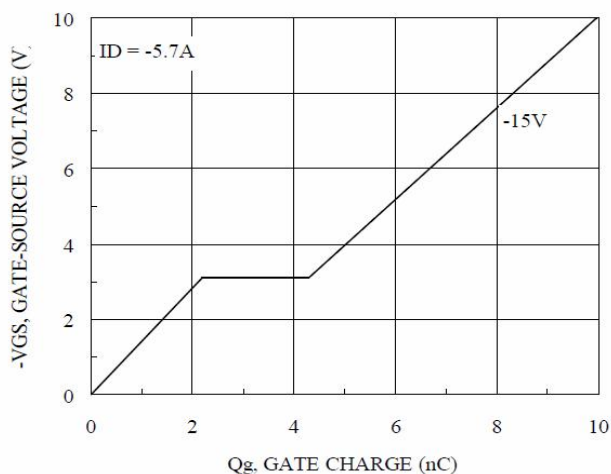


Figure 5. Gate Charge Characteristics

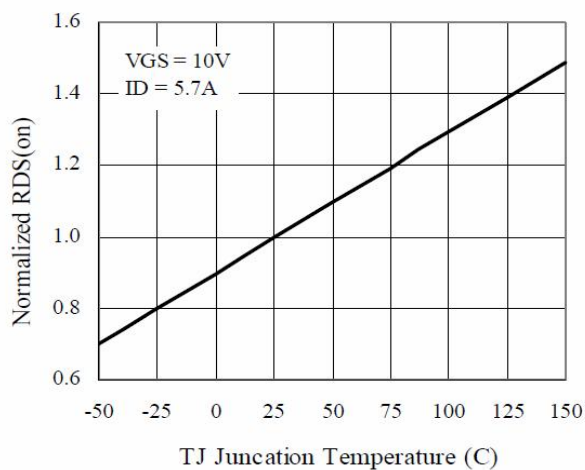


Figure 6. On-Resistance Variation with Temperature

CHARACTERISTIC CURVE (P-Ch)

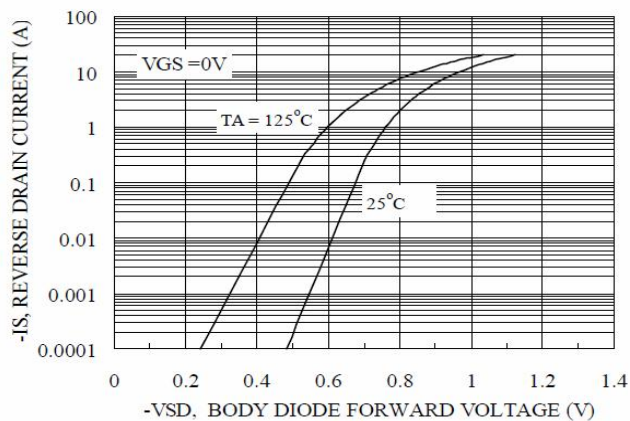


Figure 7. Transfer Characteristics

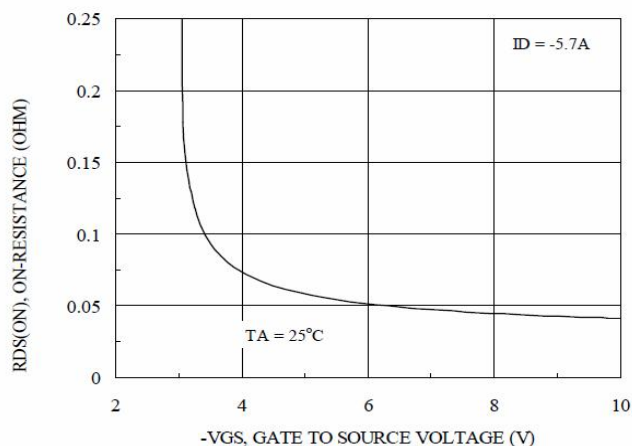


Figure 8. On-Resistance with Gate to Source Voltage

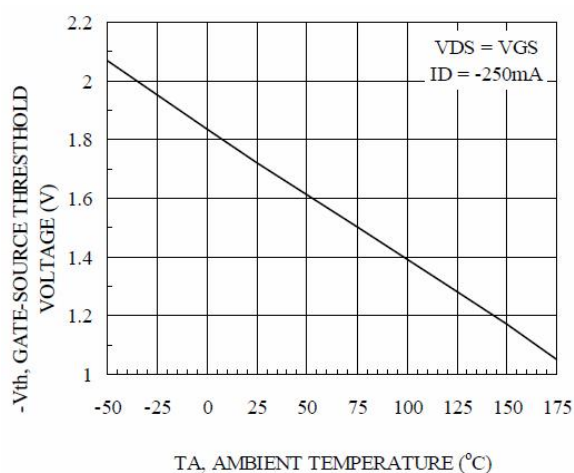


Figure 9. Vth Gate to Source Voltage Vs Temperature

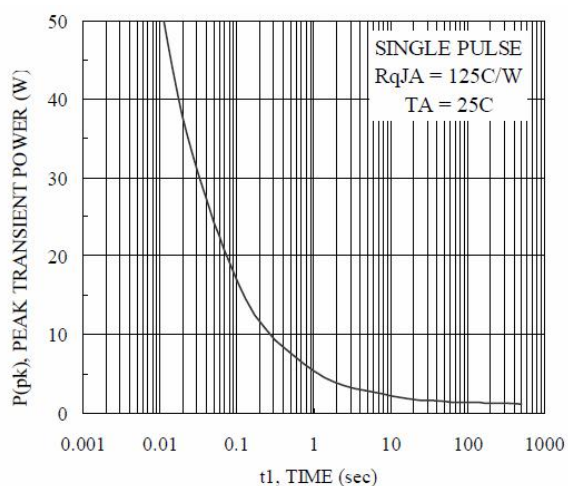


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

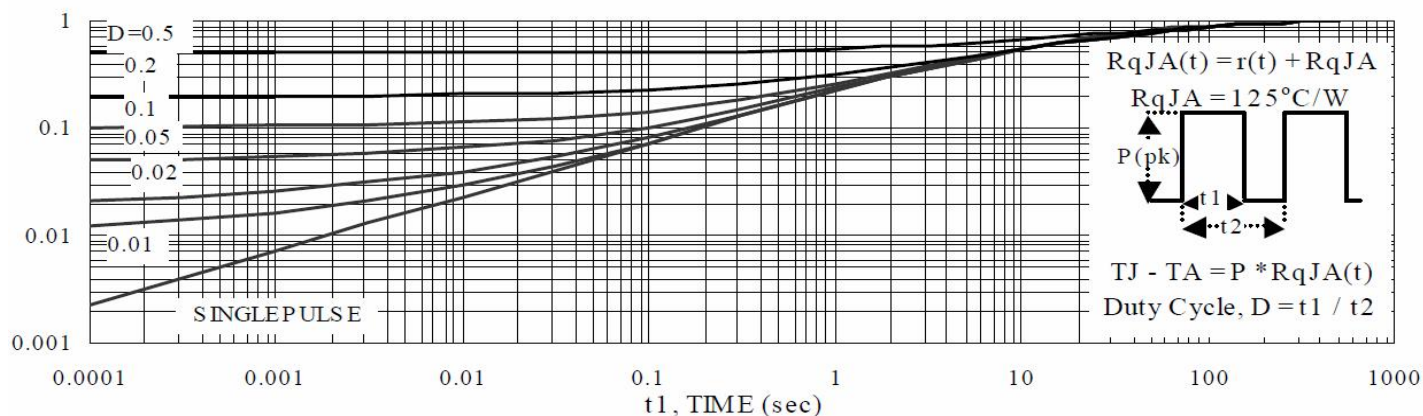


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