

Precision, High Slew Rate, Wideband Operational Amplifier

July 1997

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- High Slew Rate 120V/μs (Typ)
- Low Offset Voltage 300μV (Typ)
900μV (Max)
- High Open Loop Gain 130dB (Typ)
114dB (Min)
- Gain Bandwidth Product 150MHz (Typ)
- Low Voltage Noise at 1kHz 8.3nV/√Hz (Typ)
- Minimum Gain Stability ≥ 5 (Typ)

Applications

- High Speed Instrumentation
- Data Acquisition Systems
- Analog Signal Conditioning
- Precision, Wideband Amplifiers
- Pulse/RF Amplifiers

Description

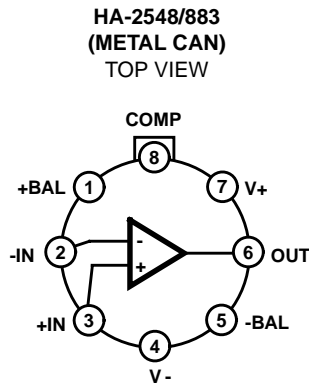
The HA-2548/883 is a monolithic op amp that offers a unique combination of bandwidth, slew rate, and precision specifications. These features can eliminate the need for composite op amp designs and external calibration circuitry.

Optimized for gains ≥5, the HA-2548/883 has a gain bandwidth product of 150MHz (typ) and a slew rate of 120V/μs (typ) while maintaining an extremely high open loop gain of 130dB (typ) and a low offset voltage of 300μV (typ). These specifications are achieved through uniquely designed input circuitry and a single ultra-high gain stage that minimizes the AC signal path. Capable of delivering over 30mA (min) of output current, the HA-2548/883 is ideal for precision, high speed applications such as signal conditioning, instrumentation, video/pulse amplifiers and buffers.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2548/883	-55 to 125	8 Pin Can	T8.C

Pinout



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
 Differential Input Voltage 5V
 Voltage at Either Input Terminal V+ to V-
 Peak Output Current (< 10% Duty Cycle) 60mA
 Continuous Output Current 40mA
 ESD Rating <2000V

Operating Conditions

Temperature Range -55°C to 125°C
 Supply Voltage ±15V
 $V_{INCM} \leq 1/2 (V+ - V-)$
 $R_L \geq 1k\Omega$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} θ_{JC}
 Metal Can Package 142°C/W 66°C/W
 Package Power Dissipation Limit at 75°C
 Metal Can Package 0.70W
 Package Power Dissipation Derating Factor Above 75°C
 Metal Can Package 7.0mW/°C
 Maximum Junction Temperature 175°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_{SUPPLY} = \pm 15V$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP. (°C)	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	25	-900	900	μV
			2, 3	125, -55	-1200	1200	μV
Input Bias Current	$+I_B$	$V_{CM} = 0V$, $+R_S = 100.1k\Omega$, $-R_S = 100\Omega$	1	25	-50	50	nA
			2, 3	125, -55	-100	100	nA
	$-I_B$	$V_{CM} = 0V$, $+R_S = 100\Omega$, $-R_S = 100.1k\Omega$	1	25	-50	50	nA
			2, 3	125, -55	-100	100	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$, $+R_S = 100.1k\Omega$, $-R_S = 100.1k\Omega$	1	25	-50	50	nA
			2, 3	125, -55	-100	100	nA
Common Mode Range	+CMR	$V+ = +8V$, $V- = -22V$	1	25	7	-	V
			2, 3	125, -55	7	-	V
	-CMR	$V+ = +22V$, $V- = -8V$	1	25	-	-7	V
			2, 3	125, -55	-	-7	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and $+10V$, $R_L = 1k\Omega$	4	25	114	-	dB
			5, 6	125, -55	108	-	dB
	$-A_{VOL}$	$V_{OUT} = 0V$ and $-10V$, $R_L = 1k\Omega$	4	25	114	-	dB
			5, 6	125, -55	108	-	dB
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +2V$, $V+ = +13V$, $V- = -17V$, $V_{OUT} = -2V$	1	25	80	-	dB
			2, 3	125, -55	80	-	dB
	-CMRR	$\Delta V_{CM} = -2V$, $V+ = +17V$, $V- = -13V$, $V_{OUT} = 2V$	1	25	80	-	dB
			2, 3	125, -55	80	-	dB

HA-2548/883

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $V_{SUPPLY} = \pm 15V$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP. (°C)	MIN	MAX	UNITS
Output Voltage Swing	+V _{OUT}	R _L = 1kΩ	4	25	11	-	V
			5, 6	125, -55	11	-	V
	-V _{OUT}	R _L = 1kΩ	4	25	-	-11	V
			5, 6	125, -55	-	-11	V
Output Current	+I _{OUT}	V _{OUT} = +10V	4	25	30	-	mA
			5, 6	125, -55	30	-	mA
	-I _{OUT}	V _{OUT} = -10V	4	25	-	-30	mA
			5, 6	125, -55	-	-30	mA
Quiescent Power Supply Current	+I _{CC}	V _{OUT} = 0V, I _{OUT} = 0mA	1	25	-	18	mA
			2, 3	125, -55	-	18	mA
	-I _{CC}	V _{OUT} = 0V, I _{OUT} = 0mA	1	25	-18	-	mA
			2, 3	125, -55	-18	-	mA
Power Supply Rejection Ratio	+PSRR	$\Delta V_{SUP} = 10V$, V ₊ = +10V, V ₋ = -15V, V ₊ = +20V, V ₋ = -15V	1	25	86	-	dB
			2, 3	125, -55	86	-	dB
	-PSRR	$\Delta V_{SUP} = 10V$, V ₊ = +15V, V ₋ = -10V, V ₊ = +15V, V ₋ = -20V	1	25	86	-	dB
			2, 3	125, -55	86	-	dB

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See AC Characteristics in Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_{SUPPLY} = \pm 15V$, $R_{LOAD} = 1k\Omega$, $C_{LOAD} \leq 10pF$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMP. (°C)	MIN	MAX	UNITS
Average Offset Voltage Drift	V _{IO} TC	V _{CM} = 0V	2	-55 to 125	-	7	μV/°C
Offset Voltage Adjust	V _{IO} Adj		2, 6	25	1	-	mV
Input Noise Voltage Density	E _N	R _S = 10Ω, f _O = 1kHz	2	25	-	13.0	nV/√Hz
Input Noise Current Density	I _N	R _S = 500Ω, f _O = 1kHz	2	25	-	1.0	pA/√Hz
Gain Bandwidth Product	GBWP	V _O = 1.0V, f _O = 1MHz	2	25	-	130	MHz
			2	-55 to 125	-	110	MHz
Slew Rate	+SR	V _{OUT} = -5V to +5V	2	25	80	-	V/μs
			2	-55 to 125	70	-	V/μs
	-SR	V _{OUT} = +5V to -5V	2	25	80	-	V/μs
			2	-55 to 125	70	-	V/μs
Full Power Bandwidth	FPBW	V _{PEAK} = 10V	2, 3	25	1.11	-	MHz

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: $V_{SUPPLY} = \pm 15V$, $R_{LOAD} = 1k\Omega$, $C_{LOAD} \leq 10pF$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMP. (°C)	MIN	MAX	UNITS
Minimum Closed Loop Stable Gain	CLSG	$R_L = 1k\Omega$, $C_L = 10pF$	2	-55 to 125	5	-	V/V
Rise and Fall Time	t_r	$V_{OUT} = -100mV$ to $+100mV$	2, 5	25	-	15	ns
			2, 5	-55 to 125	-	20	ns
	t_f	$V_{OUT} = +100mV$ to $-100mV$	2, 5	25	-	15	ns
			2, 5	-55 to 125	-	20	ns
Overshoot	+OS	$V_{OUT} = -100mV$ to $+100mV$	2	25	-	30	%
			2	-55 to 125	-	35	%
	-OS	$V_{OUT} = +100mV$ to $-100mV$	2	25	-	30	%
			2	-55 to 125	-	35	%
Settling Time	t_S	To 0.01% for a 10V Step	2	25	-	260	ns
Power Consumption	PC	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	2, 4	-55 to 125	-	540	mW

NOTES:

- Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
- Full Power Bandwidth guarantee based on Slew Rate measurement using $FPBW = Slew\ Rate / (2\pi V_{PEAK})$.
- Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
- Measured between 10% and 90% points.
- Offset adjustment range is $[V_{IO}(Measured) \pm 1mV]$ minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 7), 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C and D Endpoints	1

NOTE:

- PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:

85 mils x 91 mils x 19 mils
 2160µm x 2320µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
 Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Nitride (Si3N4) over Silox (SiO2, 5% Phos.)
 Silox Thickness: 12kÅ ± 2kÅ
 Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:

$3.6 \times 10^4 \text{ A/cm}^2$

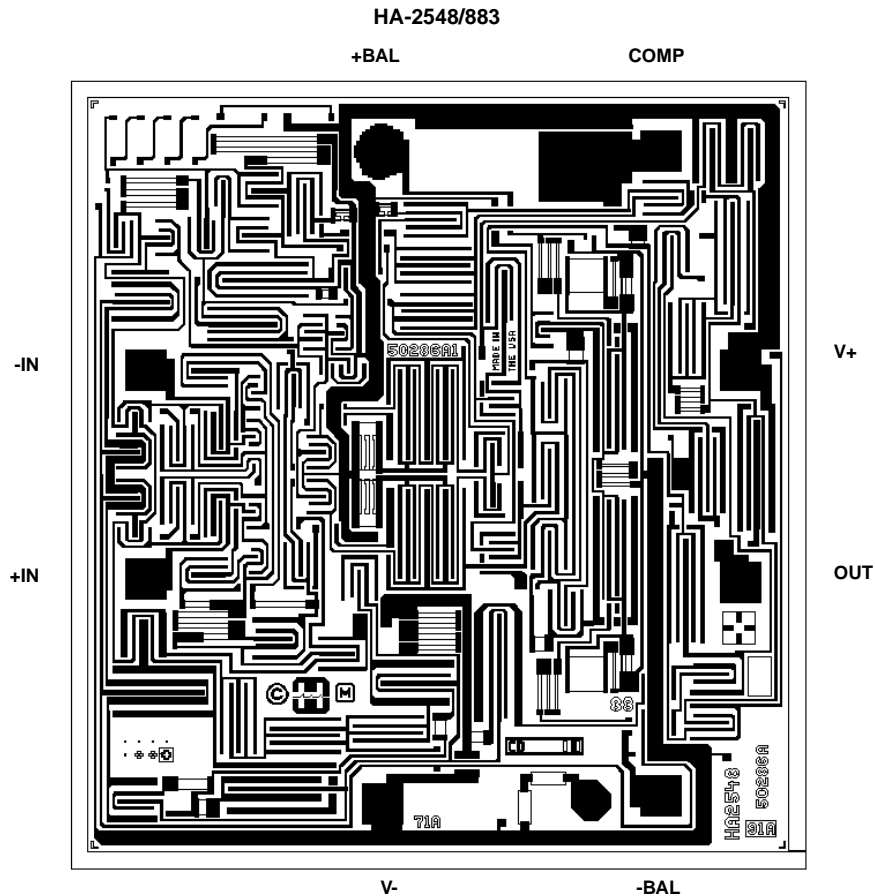
SUBSTRATE POTENTIAL (Powered Up): V- (Note)

TRANSISTOR COUNT: 60

PROCESS: Bipolar, Dielectric Isolation

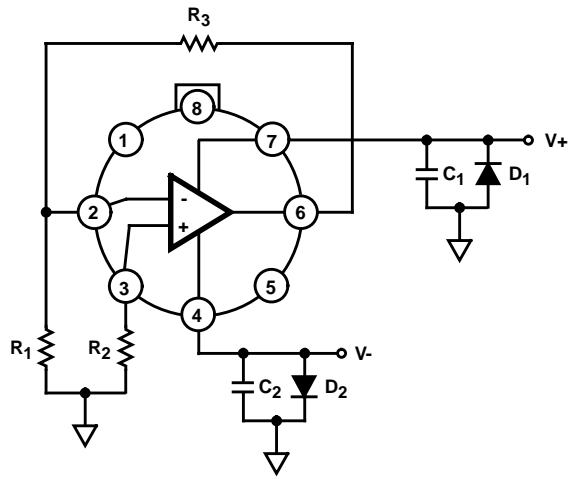
NOTE: The Substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at a V- potential.

Metallization Mask Layout



Burn-In Circuit

HA2-2548/883 METAL CAN



NOTES:

$R_1 = 1k\Omega, \pm 5\%, 1/4W$ (Min)

$R_2 = 1k\Omega, \pm 5\%, 1/4W$ (Min)

$R_3 = 10k\Omega, \pm 5\%, 1/4W$ (Min)

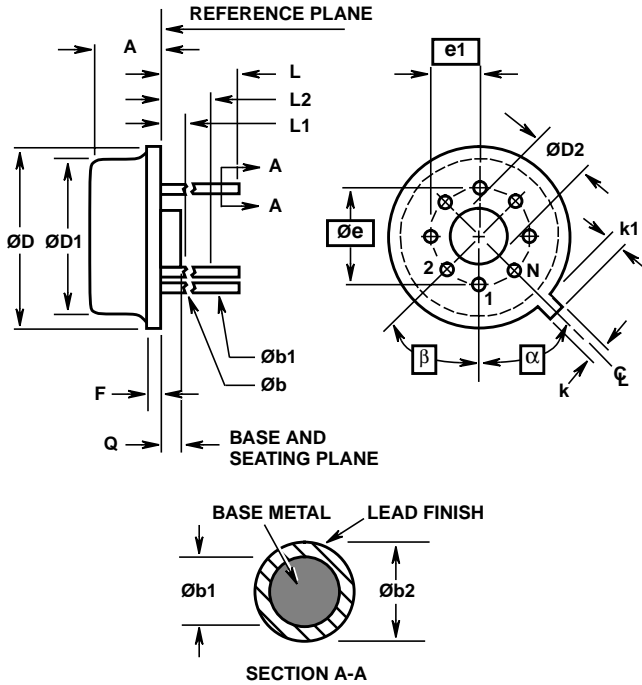
$C_1 = 0.01\mu F$ /Socket or $0.1\mu F$ /Row

$C_2 = 0.01\mu F$ /Socket or $0.1\mu F$ /Row

$D_1 = D_2 = 1N4002$ or Equivalent/Board

$|V_+ - V_-| = 31V \pm 1V$

Metal Can Packages (Can)



**T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

Rev. 0 5/18/94

NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N - 1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029