INTEGRATED CIRCUITS
UNITRODE

UC1823A,B/1825A,B
UC2823A,B/2825A,B
UC3823A,B/3825A,B

High Speed PWM Controller

FEATURES

- Improved versions of the UC3823/UC3825 PWMs
- Compatible with Voltage or Current-Mode Topologies
- Practical Operation at Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (2A Peak)
- Trimmed Oscillator Discharge Current
- Low 100µA Startup Current
- Pulse-by-Pulse Current Limiting Comparator
- Latched Overcurrent Comparator With Full Cycle Restart

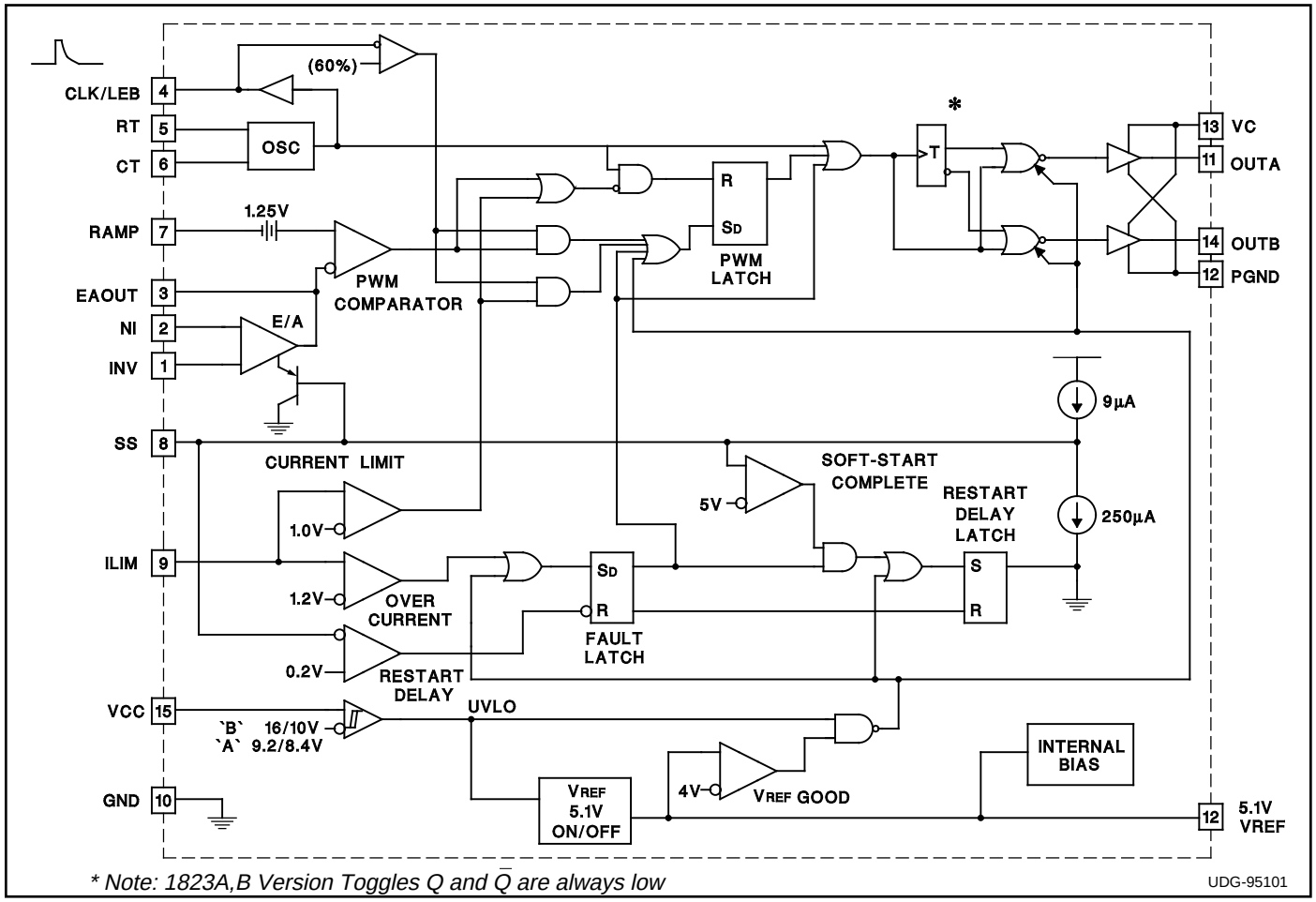
DESCRIPTION

The UC3823A & B and the UC3825A & B family of PWM control ICs are improved versions of the standard UC3823 & UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12MHz while input offset voltage is 2mV. Current limit threshold is guaranteed to a tolerance of 5%. Oscillator discharge current is specified at 10mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100µA, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2A peak currents during transitions.

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2V. The overcurrent comparator sets a latch that ensures full discharge of the soft start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 Clock pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

The UC3825A,B has dual alternating outputs and the same pin configuration of the UC3825. The UC3823A,B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the UC3823A,B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. “A” version parts have UVLO thresholds identical to the original UC3823/25. The “B” versions have UVLO thresholds of 16 and 10V, intended for ease of use in off-line applications.

Consult Application Note U-128 for detailed technical and applications information. Contact the factory for further packaging and availability information.

Device	UVLO	DMAX
UC3823A	9.2V/8.4V	< 100%
UC3823B	16V/10V	< 100%
UC3825A	9.2V/8.4V	< 50%
UC3825B	16V/10V	< 50%

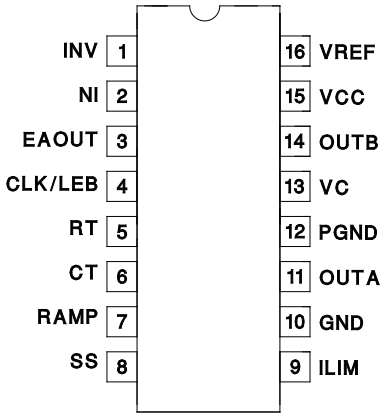
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VC, VCC) 22V
Output Current, Source or Sink (Pins OUTA, OUTB)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground (PGND) ..... ±0.2V
Analog Inputs
(INV, NI, RAMP) ..... –0.3V to 7V
(ILIM, SS) ..... –0.3V to 6V
Clock Output Current (CLK/LEB) ..... –5mA
Error Amplifier Output Current (EAOUT) 5mA
Soft Start Sink Current (SS) 20mA
Oscillator Charging Current (RT) ..... –5mA
Power Dissipation at TA = 60°C 1W
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

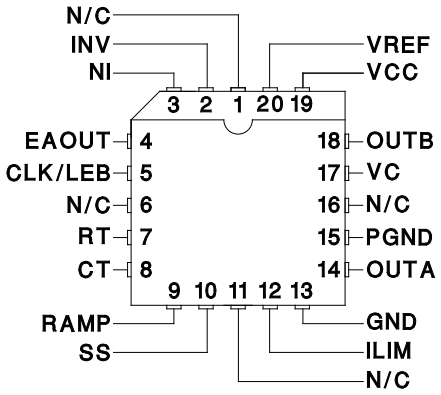
All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16, (Top View)
J or N Package; DW Package



PLCC-20, LCC-20, (Top View)
Q, L Packages



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for TA = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	TJ = 25°C, Io = 1mA	5.05	5.1	5.15	V
Line Regulation	12 < VCC < 20V		2	15	mV
Load Regulation	1mA < Io < 10mA		5	20	mV
Total Output Variation	Line, Load, Temp	5.03		5.17	V
Temperature Stability	TMIN < TA < TMAX (Note 1)		0.2	0.4	mV/°C
Output Noise Voltage	10Hz < f < 10kHz (Note 1)		50		µVRMS
Long Term Stability	TJ = 125°C, 1000 hours (Note 1)		5	25	mV
Short Circuit Current	VREF = 0V	30	60	90	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Initial Accuracy	T_J = 25°C (Note 1)	375	400	425	kHz
Total Variation	Line, Temperature (Note 1)	350		450	kHz
Voltage Stability	12V < VCC < 20V			1	%
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note 1)		5		%
Initial Accuracy	RT = 6.6k, CT = 220pF T_A = 25°C (Note 1)	0.9	1	1.1	MHz
Total Variation	RT = 6.6k, CT = 220pF (Note 1)	0.85		1.15	MHz
Clock Out High		3.7	4		V
Clock Out Low			0	0.2	V
Ramp Peak		2.6	2.8	3	V
Ramp Valley		0.7	1	1.25	V
Ramp Valley to Peak		1.6	1.8	2	V
Oscillator Discharge Current	RT = Open, V_{CT} = 2V	9	10	11	mA
Error Amplifier Section					
Input Offset Voltage			2	10	mV
Input Bias Current			0.6	3	µA
Input Offset Current			0.1	1	µA
Open Loop Gain	1V < Vo < 4V	60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		dB
PSRR	12V < VCC < 20V	85	110		dB
Output Sink Current	V_{EAOUT} = 1V	1	2.5		mA
Output Source Current	V_{EAOUT} = 4V	–0.5	–1.3		mA
Output High Voltage	I_{EAOUT} = –0.5mA	4.5	4.7	5	V
Output Low Voltage	I_{EAOUT} = 1mA	0	0.5	1	V
Gain Bandwidth Product	F = 200kHz	6	12		MHz
Slew Rate	(Note 1)	6	9		V/µs
PWM Comparator					
RAMP Bias current	V_{RAMP} = 0V		–1	–8	µA
Minimum Duty Cycle				0	%
Maximum Duty Cycle		85			%
Leading Edge Blanking	R = 2k, C = 470pF	300	375	450	ns
LEB Resistor	$V_{CLK/LEB}$ = 3V	8.5	10	11.5	kohm
EAOUT Zero D.C. Threshold	V_{RAMP} = 0V	1.1	1.25	1.4	V
Delay to Output	V_{EAOUT} = 2.1V, V_{RAMP} = 0 to 2V Step (Note 1)		50	80	ns
Current Limit/Start Sequence/Fault Section					
Soft Start Charge Current	V_{SS} = 2.5V	8	14	20	µA
Full Soft Start Threshold		4.3	5		V
Restart Discharge Current	V_{SS} = 2.5V	100	250	350	µA
Restart Threshold			0.3	0.5	V
ILIM Bias Current	0 < V_{ILIM} < 2V			15	µA
Current Limit Threshold		0.95	1	1.05	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit/Start Sequence/Fault Section (cont.)					
Over Current Threshold		1.14	1.2	1.26	V
ILIM Delay to Output	V_{ILIM} = 0 to 2V Step (Note 1)		50	80	ns
Output Section					
Output Low Saturation	I_{OUT} = 20mA		0.25	0.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Saturation	I_{OUT} = 20mA		1.9	2.9	V
	I_{OUT} = 200mA		2	3	V
UVLO Output Low Saturation	I_O = 20mA		0.8	1.2	V
Rise/Fall Time	C_L = 1nF (Note 1)		20	45	ns
UnderVoltage Lockout					
Start Threshold	UCX823B and X825B only		16	17	V
Stop Threshold	UCX823B and X825B only	9	10		V
UVLO Hysteresis	UCX823B and X825B only	5	6	7	V
Start Threshold	UCX823A and X825A only	8.4	9.2	9.6	V
UVLO Hysteresis	UCX823A and X825A only	0.4	0.8	1.2	V
Supply Current					
Startup Current	VC = VCC = V_{TH}(start) - 0.5V		100	300	µA
Icc			28	36	mA

Note 1: Guaranteed by design. Not 100% tested in production.

APPLICATIONS INFORMATION

OSCILLATOR

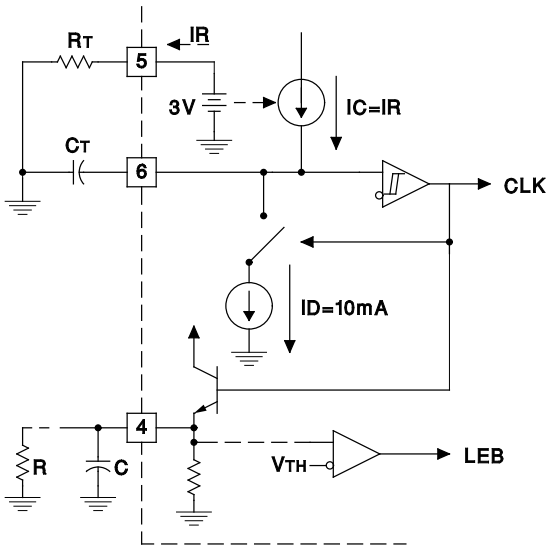
The UC3823A,B/3825A,B oscillator is a saw tooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin. The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on desired frequency, RT, and D_{MAX}. The design equations are:

$$RT = \frac{3V}{(10mA)\,(1 - D_{MAX})}$$

$$CT = \frac{(1.6 \bullet D_{MAX})}{(RT \bullet F)}$$

Recommended values for RT range from 1k to 100k. Control of D_{MAX} less than 70% is not recommended.

Oscillator

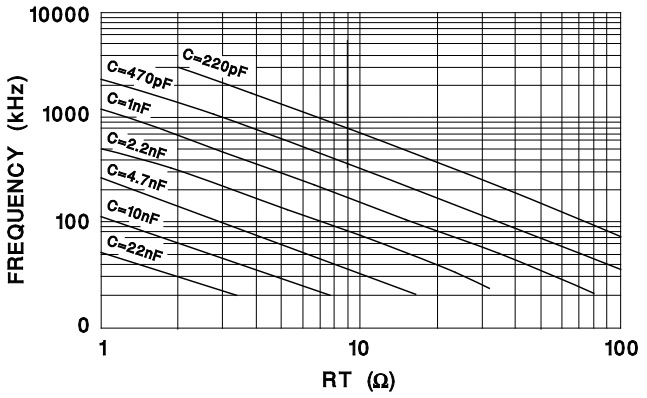


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APPLICATIONS INFORMATION (cont.)

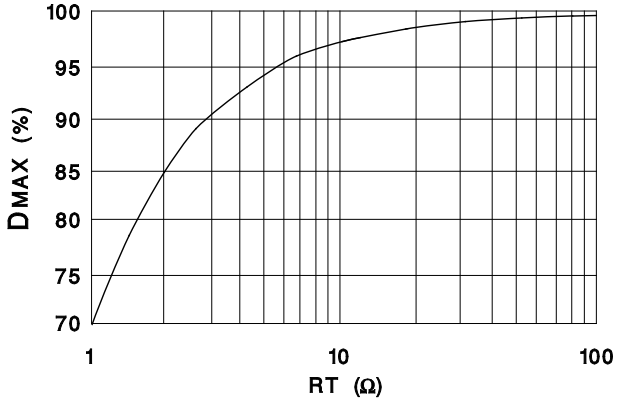
OSCILLATOR (cont.)

Oscillator Frequency vs. R_T and C_T Curve



UDG-95103

Maximum Duty Cycle vs R_T Curve



UDG-95104

LEADING EDGE BLANKING

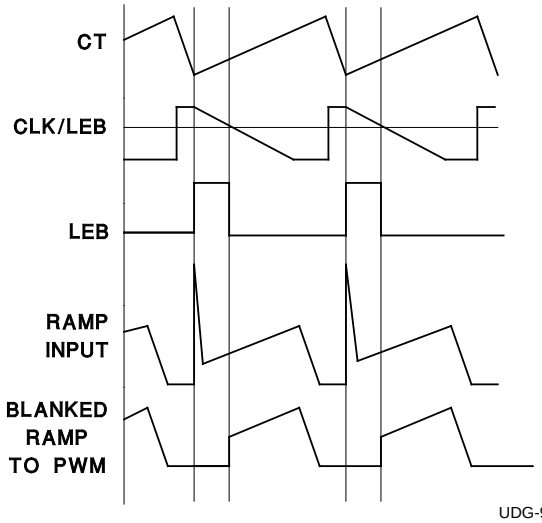
The UC3823A,B/3825A,B performs fixed frequency pulse width modulation control. The UC3823A,B outputs operate together at the switching frequency and can vary from 0 to some value less than 100%. The UC3825A,B outputs are alternately controlled. During every other cycle, one output will be off. Each output then, switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

Normally the PWM comparator will sense a ramp crossing a control voltage (error amp output) and terminate the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a Leading Edge Blanking period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10k resistor will determine the blanked interval. The 10k resistor has a 10% tolerance. For more accuracy, an external 2k 1% resistor, R, can be added, resulting in an equivalent resistance of 1.66k with a tolerance of 2.4%. The design equation is:

LEB Operational Waveforms



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$t_{LEB} = 0.5 \bullet (R \,||\, 10k) \bullet C.$

Values of R less than 2k should not be used

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the one volt threshold, the pulse is terminated. The over current comparator, however, is not blanked. It will catch catastrophic over current faults without a blanking delay. Any time the ILIM pin exceeds 1.2V, the fault latch will be set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.

APPLICATIONS INFORMATION (cont.)

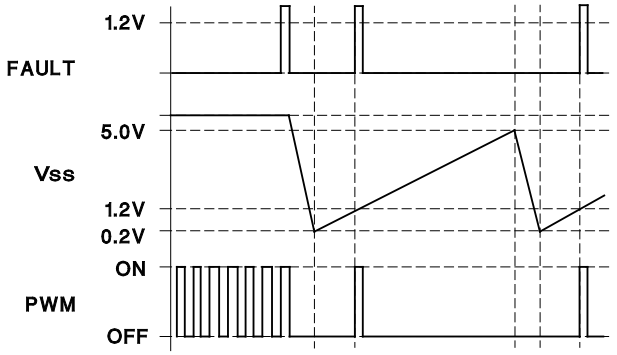
UVLO, SOFT START AND FAULT MANAGEMENT

Soft start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amp output is also forced low. As the internal 9µA source charges the SS pin, the error amp output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2V, the fault latch will be set and the output pins will be driven low. The soft start cap is then discharged by a 250µA current sink. No more output pulses are allowed until soft start is fully discharged, and ILIM is below 1.2V. At this point the fault latch will be reset and the chip will execute a soft start.

Should the fault latch be set during soft start, the outputs will be immediately terminated, but the soft start cap will not be discharged until it has been fully charged. This results in a controlled hiccup interval for continuous fault conditions.

Soft Start and Fault Waveforms

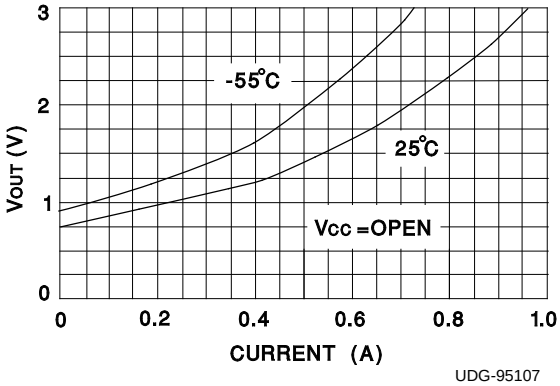


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ACTIVE LOW OUTPUTS DURING UVLO

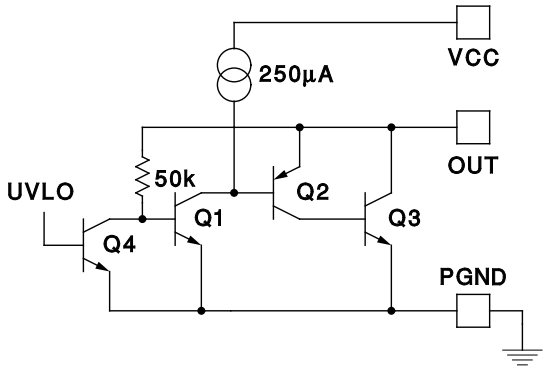
The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

Simplified Schematic



UDG-95107

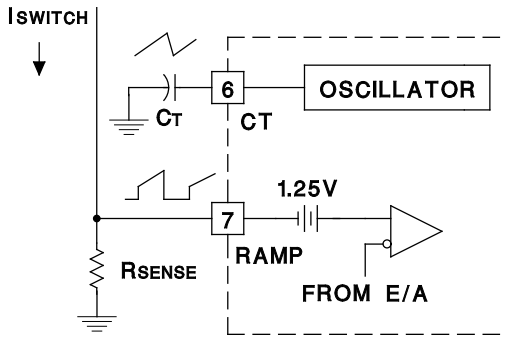
Output V and I During UVLO



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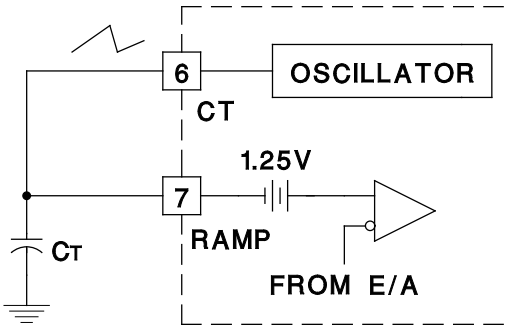
PWM APPLICATIONS

Current Mode



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Voltage Mode



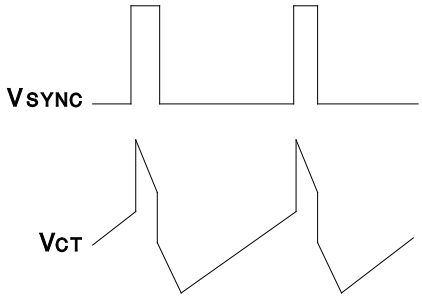
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APPLICATIONS INFORMATION (cont.)

SYNCHRONIZATION

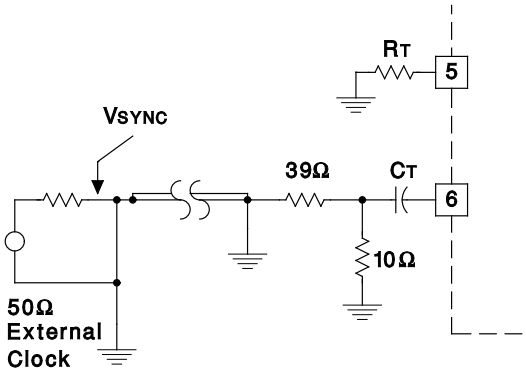
The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10 to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that, the CLK/LEB pin will no longer accept an incoming synchronizing signal.

Operational Waveforms



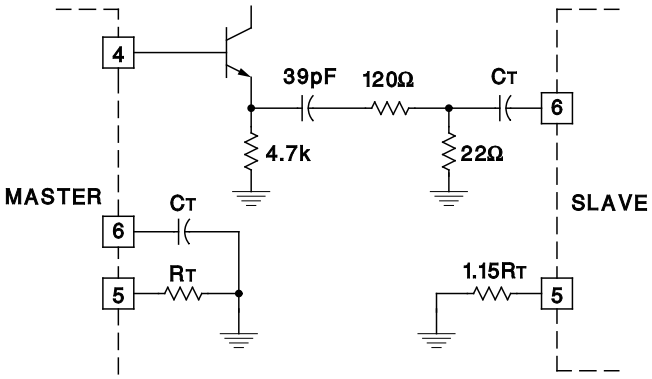
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General Oscillator Synchronization



UDG-95111

Two Units



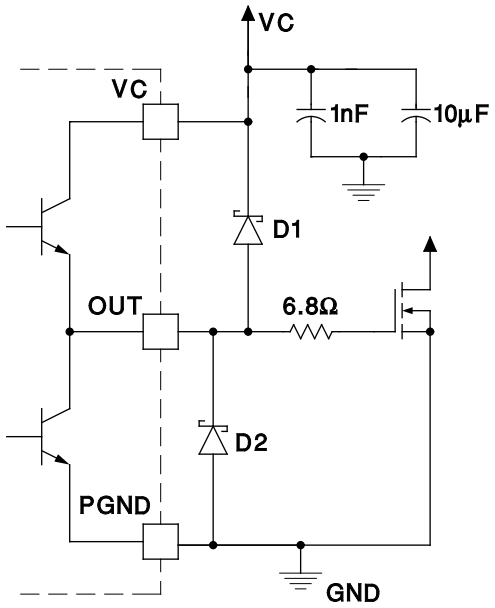
UDG-95113

HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A,B and UC3825A,B can deliver a 2 amp peak current into a capacitive load. The output can slew a 1000pF capacitor 15 volts in approximately 20 nanoseconds. Separate collector supply (VC) and power ground (PGND) pins help decouple the IC's analog circuitry from the high power gate drive noise. The use of 3 Amp Schottky diodes (1N5120, USD245 or equivalent) as shown in the figure from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

Although a "single ended" device, two output drivers are available on the UC3823A,B devices. These can be “paralleled” by the use of a one-half ohm (noninductive) resistor connected in series with each output for a combined peak current of 4 Amps.

Power MOSFET Drive Circuit



D1, D2 = 1N5820

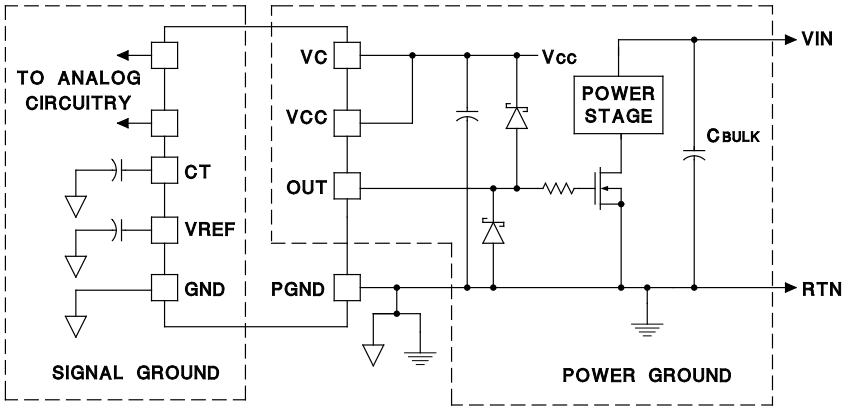
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APPLICATIONS INFORMATION (cont.)

GROUND PLANES

Each output driver of these devices is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

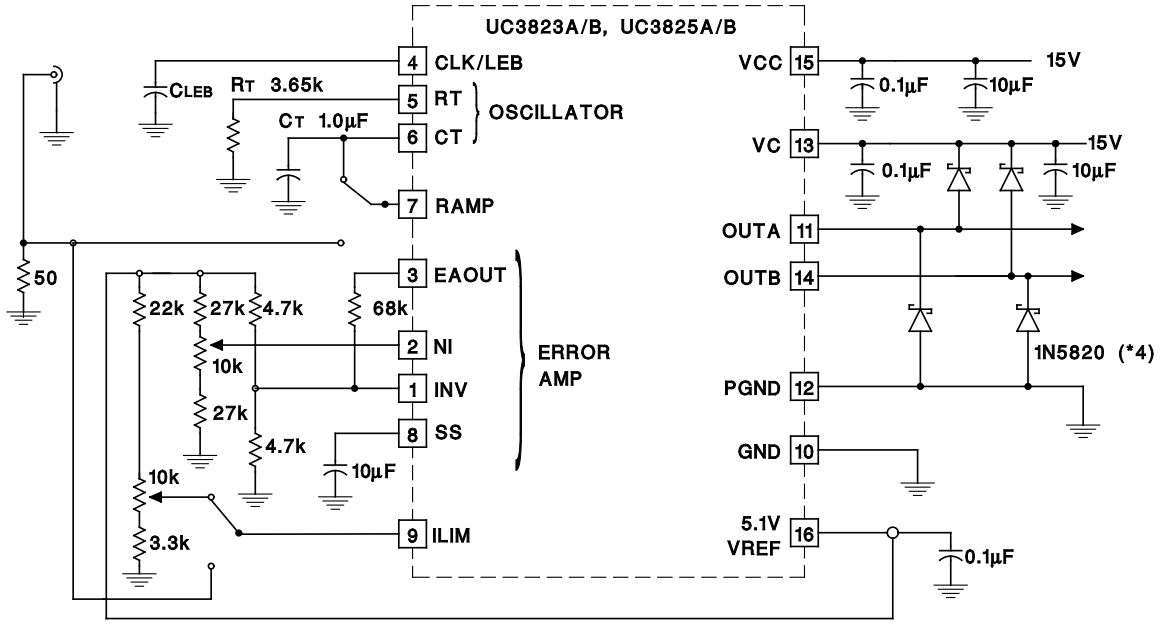
VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1µF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.



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Open Loop Test Circuit

This test fixture is useful for exercising many of the UC3823A,B, UC3825A,B functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.



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