CUSTOMER PROCUREMENT SPECIFICATION

Z89302/04/06

DIGITAL TELEVISION CONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed MHz
Z89302	24	640	12
Z89304	16	640	12
Z89306	12	640	12

Note: * General-Purpose

- 40-Pin DIP Packages
- 4.75- to 5.25-Volt Operating Range
- 0°C to +70°C Temperature Range
- Fully Customized Character Set
- Character-Control and Closed-Caption Modes
- Keypad User Control
- TV Tuner Serial Interface
- Direct Video Signals

GENERAL DESCRIPTION

The Z89302/04/06 Digital Television Controllers are designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The Television Controllers feature a Z89C00 RISC processor core that controls the on-board peripheral functions and registers using the standard processor instruction set.

Character attributes can be controlled through two modes: the on-screen display Character-Control Mode and the Closed-Caption Mode. The Character-Control Mode provides access to the full set of attribute controls, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tuning adjustments, may be accessed through the industry-standard I^2C port.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

The Z89302/04/06 has two internal 12 MHz VCOs that are referenced to a 32 kHz internal oscillator to provide the system clock. In Sleep Mode, the controller uses the 32 kHz clock for the system clock to reduce power consumption. The processor can be suspended by placing it into STOP Mode when main power is not available for low-power consumption.

GENERAL DESCRIPTION (Continued)

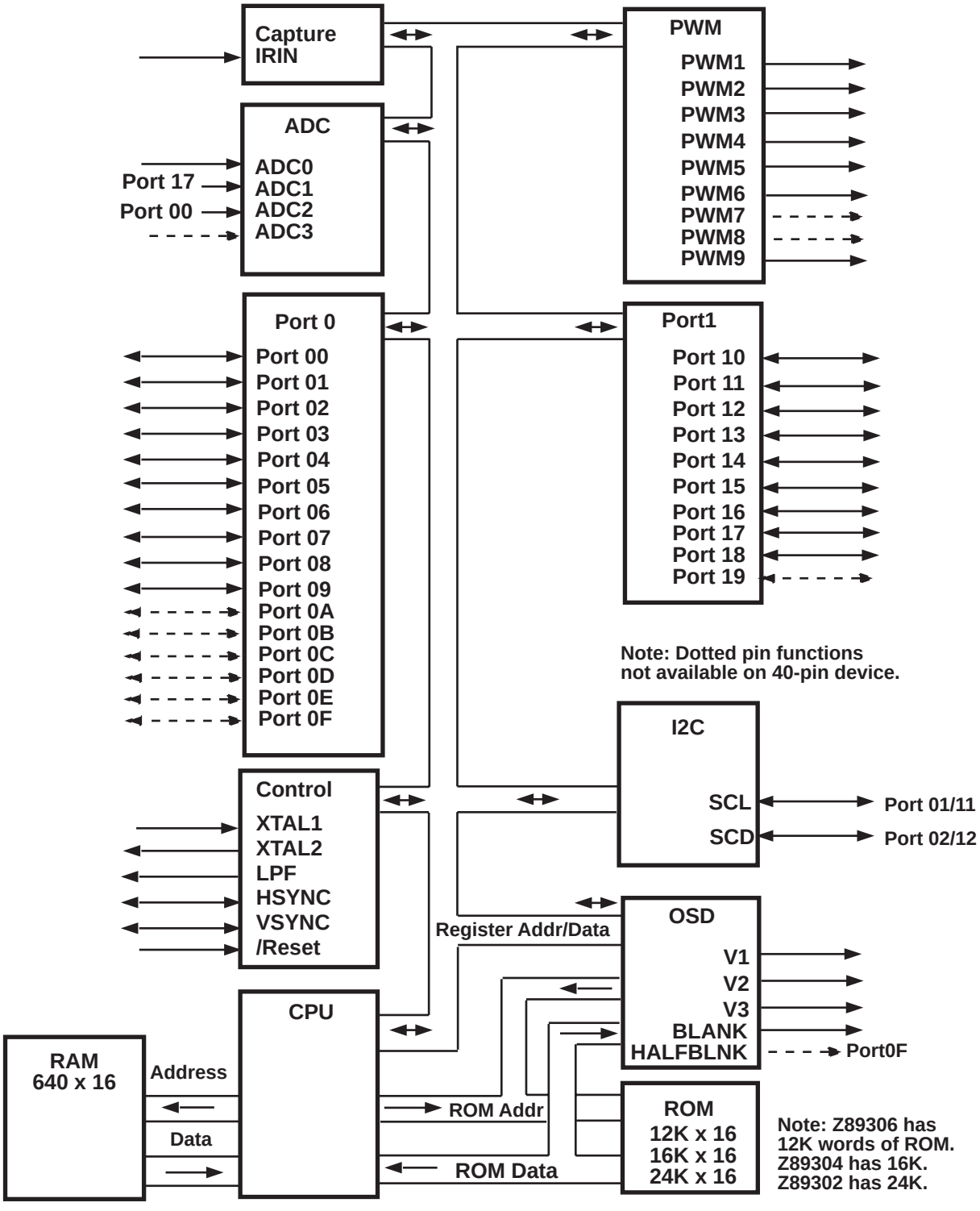


Figure 1. Z8930X Functional Block Diagram

PIN DESCRIPTION

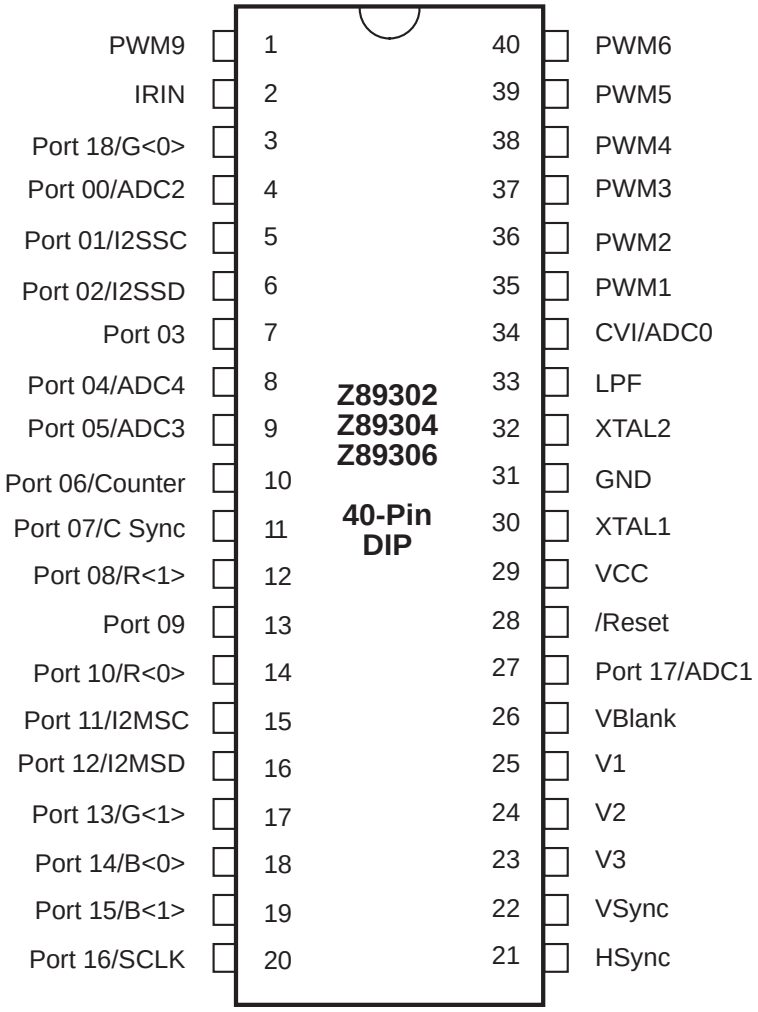


Figure 2. 40-Pin DIP Configuration

PIN DESCRIPTIONS

Z89302/03/06/07

Pin Name	Function	40-Pin, Z89302/04/06	Direction	Reset Configuration
V_{CC}	+5V	29,–		PWR–
GND	0V	31,–		PWR–
IRIN	Infrared Remote Capture Input	2	I	I
ADC[5:0]	4-Bit Analog to Digital Converter Input	–,9,8,4,27,34	nAI	I
PWM9	14-Bit Pulse Width Modulator Output	1	OD/O[a]	O
PWM[8:1]	8-Bit Pulse Width Modulator Output	–,–,40,39,38	OD/O[a]	O
Port0[F:0]	Bit Programmable Input/Output Ports	–,–,–,–,–,–,13,12,11,10,9,8,7,6,5,4	B	I
Port1[9:0]	Bit Programmable Input/Output Ports	–,3,27,20,19,18,17,16,15,14	B	I
SCL[b]	I^2C Clock I/O	5 or 15	BOD	
SCD[c]	I^2C Data I/O	6 or 16	BOD	
XTAL1	Crystal Oscillator Input	30	AI	I
XTAL2	Crystam Oscillator Output	32	AO	O
LPF	Loop Filter	33	AB	O
HSYNC	H_Sync	21	B	I
VSYNC	V_Sync	22	B	I
/RESET	Device Reset	28	I	I
V[3:1]	OSD Video Output (Typically Drive B, G, and R Outputs)	23,24,25	O	O
Blank	OSD Blank Output	26	O	O
Half Blank[d]	OSD Half Blank Output	–	O	I
RGB Digital Outputs[e]	R[1:0],G[1:0], and B[1:0] Outputs of the RGB Matrix	19,18,17,14,12,3	O	
SCLK[f]	Internal Processor SCLK		O	

Notes:

a) Port19 is not available on the 40-pin DIP Version, Revision D is Push-Pull.

b) SCL I/O pin is shared with Port01 or Port11

c) SCD I/O pin is shared with Port02 or Port12

d) Half Blank output is a function shared with Port0F. Half Blank output is not available on the 40-pin DIP version.

e) Digital RGB outputs and the internal SCLK are shared with Port1[5:0].

f) Internal processor SCLK is shared with Port16.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Power Supply Voltage	0	7	V	
V_{ID}	Input Voltage	–0.3	V_{CC} +0.3	V	Digital Inputs
V_{IA}	Input Voltage	–0.3	V_{CC} +0.3	V	Analog Inputs (A/D0-A/D4)
V_O	Output Voltage	–0.3	V_{CC} +0.3	V	All Push-Pull Digital Output
V_O	Output Voltage	–0.3	V_{CC} +0.3	V	Open-Drain/Push-Pull PWM Outputs (PWM1-PWM8)
I_{OH}	Output Current High		–10	mA	One Pin
I_{OH}	Output Current High		–100	mA	All Pins
I_{OL}	Output Current Low		20	mA	One Pin
I_{OL}	Output Current Low		200	mA	All Pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	–65	150	°C	

Note: Revision D and later have push-pull PWM outputs.

DC CHARACTERISTICS

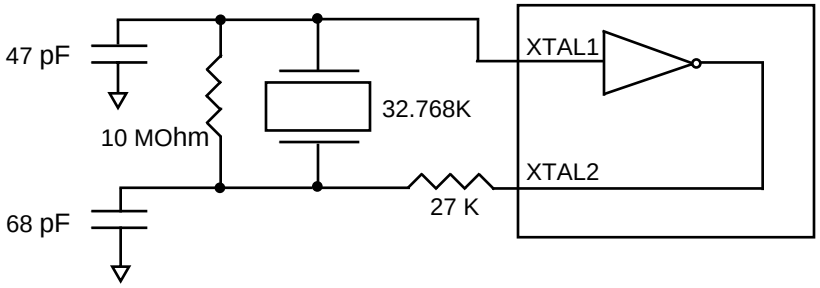
T_A = 0°C to + 70°C; V_{CC} = 4.5 V to + 5.5 V; F_{OSC} = 32.768 kHz

Symbol	Parameter	Min	Max	Typical	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	0.4	V	
V_{IH}	Input Voltage High	0.6 V_{CC}	V_{CC}	3.6	V	
V_{PU}	Max. Pull-Up Voltage		5		V	All Pins
V_{OL}	Output Voltage Low		0.4	0.16	V	@ I_{OL} = 1 mA
V_{OL}	Output Voltage High	V_{CC}–0.9		4.75	V	@ I_{OL} = 0.75 mA
V_{XL}	Input Voltage XTAL1 Low		0.3 V_{CC}	1.0	V	External Clock
V_{XH}	Input Voltage XTAL1 High	V_{CC}–2.0		3.5	V	Generator Driven
V_{HY}	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I_{IR}	Reset Input Current		150	90	µA	V_{RL} = 0V
I_{IL}	Input Leakage	–3.0	3.0	0.01	µA	@ 0 V and V_{CC}
I_{CC}	Supply Current		100	60	mA	
I_{CC1E}	Supply Current of the OTP		700	300	µA	Sleep Mode @ 32 kHz
I_{CC1}	Supply Current		300	100	µA	Sleep Mode @ 32 kHz
I_{CC2}	Supply Current		10	5	µA	Sleep Mode
I_{ADC}	Input Current		0.5		mA	C Revision
I_{ADC}	Input Current		10		µA	D Revision

V1,V2,V3 ANALOG OUTPUT

Condition	4.75 V	5.25 V	
11	3.6 – 4.4	4.0 – 5.0	V_{II}
10	79% of V_{II} ±5%		
01	50% of V_{II} ±5%		
00	0.0 – 0.8V		

Notes:
Maximum Variance Between V1, V2, V3 is 100 mV
Settling Time 70% of DC Level, 10pF Load <50n Sec



32K Oscillator Recomended Circuit

Figure 3. 32K Oscillator Recommended Circuit

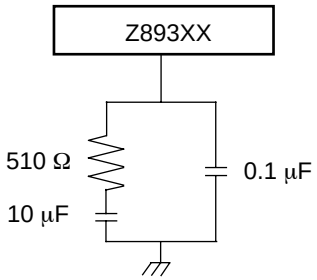


Figure 4. Low Pass Filter

AC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to 5.5 V; F_{OSC} = 32.768 kHz

Symbol	Parameter	Min	Max	Typical	Units
T_PC	Input Clock Period	16	100	32	µs
T_RC,T_FC	Clock Input Rise and Fall			12	µs
T_DPOR	Power-On Reset Delay	0.8		1.2	s

AC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to 5.5 V; F_{OSC} = 32.768 kHz

Symbol	Parameter	Min.	Max.	Typical	Units
T_WRES	Power-On Reset Min. Width		5TPC		µs
T_DH_S	H_Sync Incoming Signal Width	5.5	12.5	11	µs
T_DV_S	V_Sync Incoming Signal Width	0.15	1.5	1.0	ms
T_DE_S	Time Delay Between Leading Edge of V_Sync and H_Sync on Even Field	–12	+12	0	µs
T_DO_S	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	µs
T_WHV_S	H_Sync/V_Sync Edge Width		2.0	0.5	µs

Note: All timing of the I^2C bus interface is defined by related specifications of the I^2C bus interface.

ANALOG INPUT

ADC0

Step	Min.	Max
1	1.45	1.55
15	Step 1 + 0.468	Step 1 + 0.532

ADC1

Step	Min.	Max
1	0.2	0.4
15	Step_1 + 4.95	Step_1 + 5.15

Note: V_{CC} = 5V

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