



# 128MB - 16Mx72 DDR SDRAM REGISTERED, ECC w/PLL

## FEATURES

- Double-data-rate architecture
- DDR200 and DDR266
- BI-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2, 2.5 (clock)
- Programmable Burst Length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- Power supply: 2.5V ± 0.20V
- 184 pin DIMM package
  - D3 = 26.67 (1.05")

## DESCRIPTION

The W3EG7217S is a 16Mx72 Double Data Rate SDRAM memory module based on 128Mb DDR SDRAM component. The module consists of nine 16Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin FR4 substrate.

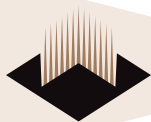
Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

\* This product is subject to change without notice.

Note: Consult factory for availability of lead-free products (F = Lead-Free, G = RoHS compliant)

## OPERATING FREQUENCIES

	DDR266 @CL=2	DDR266 @CL=2.5	DDR200 @CL=2
Clock Speed	133MHz	133MHz	100MHz
CL-trCD-trP	2-2-2	2.5-3-3	2-2-2



**PIN CONFIGURATION**

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V <sub>REF</sub>	47	DQS8	93	V <sub>SS</sub>	139	V <sub>SS</sub>
2	DQ0	48	A0	94	DQ4	140	DQM8
3	V <sub>SS</sub>	49	CB2	95	DQ5	141	A10
4	DQ1	50	V <sub>SS</sub>	96	V <sub>CCQ</sub>	142	CB6
5	DQS0	51	CB3	97	DQM0	143	V <sub>CCQ</sub>
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V <sub>CC</sub>	53	DQ32	99	DQ7	145	V <sub>SS</sub>
8	DQ3	54	V <sub>CCQ</sub>	100	V <sub>SS</sub>	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	RESET#	56	DQS4	102	NC	148	V <sub>CC</sub>
11	V <sub>SS</sub>	57	DQ34	103	NC	149	DQM4
12	DQ8	58	V <sub>SS</sub>	104	V <sub>CCQ</sub>	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V <sub>SS</sub>
15	V <sub>CCQ</sub>	61	DQ40	107	DQM1	153	DQ44
16	*CK1	62	V <sub>CCQ</sub>	108	V <sub>CC</sub>	154	RAS#
17	*CK1#	63	WE#	109	DQ14	155	DQ45
18	V <sub>SS</sub>	64	DQ41	110	DQ15	156	V <sub>CCQ</sub>
19	DQ10	65	CAS#	111	CKE1*	157	CS0#
20	DQ11	66	V <sub>SS</sub>	112	V <sub>CCQ</sub>	158	CS1#*
21	CKE0	67	DQS5	113	*BA2	159	DQM5
22	V <sub>CCQ</sub>	68	DQ42	114	DQ20	160	V <sub>SS</sub>
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V <sub>CC</sub>	116	V <sub>SS</sub>	162	DQ47
25	DQS2	71	*CS2#	117	DQ21	163	A13*
26	V <sub>SS</sub>	72	DQ48	118	A11	164	V <sub>CCQ</sub>
27	A9	73	DQ49	119	DQM2	165	DQ52
28	DQ18	74	V <sub>SS</sub>	120	V <sub>CC</sub>	166	DQ53
29	A7	75	*CK2#	121	DQ22	167	A13
30	V <sub>CCQ</sub>	76	*CK2	122	A8	168	V <sub>CC</sub>
31	DQ19	77	V <sub>CCQ</sub>	123	DQ23	169	DQM6
32	A5	78	DQS6	124	V <sub>SS</sub>	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V <sub>SS</sub>	80	DQ51	126	DQ28	172	V <sub>CCQ</sub>
35	DQ25	81	V <sub>SS</sub>	127	DQ29	173	NC
36	DQS3	82	V <sub>CCID</sub>	128	V <sub>CCQ</sub>	174	DQ60
37	A4	83	DQ56	129	DQM3	175	DQ61
38	V <sub>CC</sub>	84	DQ57	130	A3	176	V <sub>SS</sub>
39	DQ26	85	V <sub>CC</sub>	131	DQ30	177	DQS16
40	DQ27	86	DQ57	132	V <sub>SS</sub>	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V <sub>SS</sub>	88	DQ59	134	CB4	180	V <sub>CCQ</sub>
43	A1	89	V <sub>SS</sub>	135	CB5	181	SA0
44	CB0	90	NC	136	V <sub>CCQ</sub>	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V <sub>CC</sub>	92	SCL	138	CK0#	184	V <sub>CCSPD</sub>

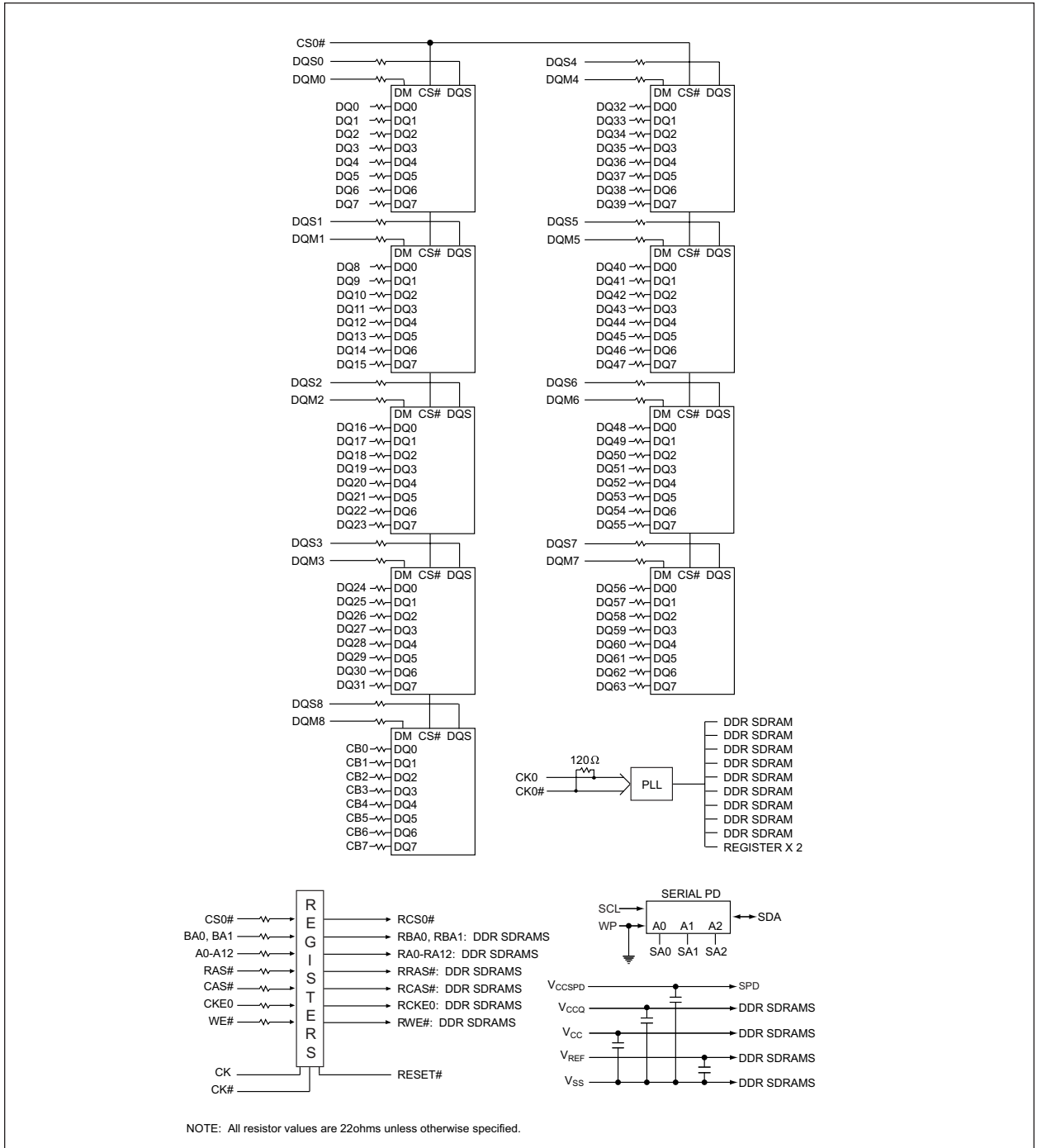
**PIN NAMES**

A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check bits
DQS0-DQS8	Data Strobe Input/Output
CK0	Clock Input
CK0#	Clock input
CKE0	Clock Enable input
CS0#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-DQM8	Data-In Mask
V <sub>CC</sub>	Power Supply
V <sub>CCQ</sub>	Power Supply for DQS
V <sub>SS</sub>	Ground
V <sub>REF</sub>	Power Supply for Reference
V <sub>CCSPD</sub>	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
V <sub>CCID</sub>	V <sub>CC</sub> Identification Flag
NC	No Connect
RESET#	Reset Enable

\* Not Used



FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22ohms unless otherwise specified.



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Voltage on any pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 ~ 3.6	V
Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub>	V <sub>CC</sub> , V <sub>CCQ</sub>	-1.0 ~ 3.6	V
Storage Temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power Dissipation	P <sub>D</sub>	9	W
Short Circuit Current	I <sub>OS</sub>	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
 Functional operation should be restricted to recommended operating condition.  
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**DC CHARACTERISTICS**

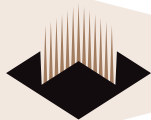
T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 2.5V ± 0.2V

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	2.3	2.7	V
Supply Voltage	V <sub>CCQ</sub>	2.3	2.7	V
Reference Voltage	V <sub>REF</sub>	1.15	1.35	V
Termination Voltage	V <sub>TT</sub>	1.15	1.35	V
Input High Voltage	V <sub>IH</sub>	V <sub>REF</sub> +0.15	V <sub>CCQ</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	V <sub>REF</sub> +0.15	V
Output High Voltage	V <sub>OH</sub>	V <sub>TT</sub> +0.76	—	V
Output Low Voltage	V <sub>OL</sub>	—	V <sub>TT</sub> -0.76	V

**CAPACITANCE**

T<sub>A</sub> = 25°C, f = 1MHz, V<sub>CC</sub> = 2.5V

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C <sub>IN1</sub>	6.25	pF
Input Capacitance (RAS#,CAS#,WE#)	C <sub>IN2</sub>	6.25	pF
Input Capacitance (CKE0)	C <sub>IN3</sub>	6.25	pF
Input Capacitance (CK0#,CK0)	C <sub>IN4</sub>	5.5	pF
Input Capacitance (CS0#)	C <sub>IN5</sub>	6.25	pF
Input Capacitance (DQM0-DQM8)	C <sub>IN6</sub>	8.0	pF
Input Capacitance (BA0-BA1)	C <sub>IN7</sub>	6.25	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C <sub>OUT</sub>	8.0	pF
Data input/output capacitance (CB0-CB7)	C <sub>OUT</sub>	8.0	pF

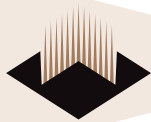


## IDD SPECIFICATIONS AND TEST CONDITIONS

0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>CCQ</sub> = 2.5V ± 0.2V, V<sub>CC</sub> = 2.5V ± 0.2V

Includes PLL and Register Power

Parameter	Symbol	Conditions	DDR266@CL = 2 Max	DDR266@CL = 2.5 Max	DDR200@CL = 2 Max	Units
Operating Current	I <sub>DD0</sub>	One device bank; Active = Precharge; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	1266	1221	1221	mA
Operating Current	I <sub>DD1</sub>	One device bank; Active-Read-Precharge; Burst = 2; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle.	1356	1356	1356	mA
Precharge Power-Down Standby Current	I <sub>DD2P</sub>	All device banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = (low)	27	27	27	mA
die Standby Current	I <sub>DD2F</sub>	CS# = High; All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS and DM.	750	705	705	mA
Active Power-Down Standby Current	I <sub>DD3P</sub>	One device bank active; Power-down mode; t <sub>CK</sub> (MIN); CKE = (low)	225	180	180	mA
Active Standby Current	I <sub>DD3N</sub>	CS# = High; CKE = High; One device bank; Active-Precharge; t <sub>RC</sub> = t <sub>RAS</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	795	750	750	mA
Operating Current	I <sub>DD4R</sub>	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA.	1446	1401	1401	mA
Operating Current	I <sub>DD4W</sub>	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing twice per clock cycle.	1401	1356	1356	mA
Auto Refresh Current	I <sub>DD5</sub>	t <sub>RC</sub> = t <sub>RC</sub> (MIN)	2325	2325	2325	mA
Self Refresh Current	I <sub>DD6</sub>	CKE ≤ 0.2V	372	363	363	mA
Operating Current	I <sub>DD7A</sub>	Four bank interleaving Reads (BL = 4) with auto precharge with t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); Address and control inputs change only during Active Read or Write commands.	3246	3201	3201	mA



**I<sub>DD</sub> SPECIFICATIONS AND TEST CONDITIONS**

0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>CCQ</sub> = 2.5V ± 0.2V, V<sub>CC</sub> = 2.5V ± 0.2V

Includes DDR SDRAM Component Only

Parameter	Symbol	Conditions	DDR266@CL = 2 Max	DDR266@CL = 2.5 Max	DDR200@CL = 2 Max	Units
Operating Current	I <sub>DD0</sub>	One device bank; Active = Precharge; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	900	945	945	mA
Operating Current	I <sub>DD1</sub>	One device bank; Active-Read-Precharge; Burst = 2; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle.	1080	1080	1080	mA
Precharge Power-Down Standby Current	I <sub>DD2P</sub>	All device banks idle; Power- down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = (low)	27	27	27	mA
die Standby Current	I <sub>DD2F</sub>	CS# = High; All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS and DM.	405	360	360	mA
Active Power-Down Standby Current	I <sub>DD3P</sub>	One device bank active; Power-down mode; t <sub>CK</sub> (MIN); CKE = (low)	225	180	180	mA
Active Standby Current	I <sub>DD3N</sub>	CS# = High; CKE = High; One device bank; Active-Precharge; t <sub>RC</sub> = t <sub>RAS</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	450	405	405	mA
Operating Current	I <sub>DD4R</sub>	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA.	1170	1125	1125	mA
Operating Current	I <sub>DD4W</sub>	Burst = 2; Writes; Continous burst; One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ,DM and DQS inputs changing twice per clock cycle.	1125	1080	1080	mA
Auto Refresh Current	I <sub>DD5</sub>	t <sub>RC</sub> = t <sub>RC</sub> (MIN)	1980	1980	1980	mA
Self Refresh Current	I <sub>DD6</sub>	CKE ≤ 0.2V	27	18	18	mA
Operating Current	I <sub>DD7A</sub>	Four bank interleaving Reads (BL = 4) with auto precharge with t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); Address and control inputs change only during Active Read or Write commands.	2970	2925	2925	mA



**DETAILED TEST CONDITIONS FOR DDR SDRAM I<sub>DD1</sub> & I<sub>DD7A</sub>**

**I<sub>DD1</sub> : OPERATING CURRENT : ONE BANK**

1. Typical Case : V<sub>CC</sub>=2.5V, T=25°C
2. Worst Case : V<sub>CC</sub>=2.7V, T=10°C
3. Only one bank is accessed with t<sub>RC</sub> (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I<sub>OUT</sub> = 0mA
4. Timing Patterns :
  - DDR200 (100 MHz, CL=2) : t<sub>CK</sub>=10ns, CL2, BL=4, t<sub>RCD</sub>=2\*t<sub>CK</sub>, t<sub>TRAS</sub>=5\*t<sub>CK</sub>  
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
  - DDR266 (133MHz, CL=2.5) : t<sub>CK</sub>=7.5ns, CL=2.5, BL=4, t<sub>RCD</sub>=3\*t<sub>CK</sub>, t<sub>RC</sub>=9\*t<sub>CK</sub>, t<sub>TRAS</sub>=5\*t<sub>CK</sub>  
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
  - DDR266 (133MHz, CL=2) : t<sub>CK</sub>=7.5ns, CL=2, BL=4, t<sub>RCD</sub>=3\*t<sub>CK</sub>, t<sub>RC</sub>=9\*t<sub>CK</sub>, t<sub>TRAS</sub>=5\*t<sub>CK</sub>  
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

**I<sub>DD7A</sub> : OPERATING CURRENT : FOUR BANKS**

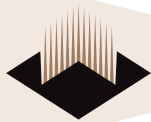
1. Typical Case : V<sub>CC</sub>=2.5V, T=25°C
2. Worst Case : V<sub>CC</sub>=2.7V, T=10°C
3. Four banks are being interleaved with t<sub>RC</sub> (min), Burst Mode, Address and Control inputs on NOP edge are not changing. I<sub>OUT</sub>=0mA
4. Timing Patterns :
  - DDR200 (100 MHz, CL=2) : t<sub>CK</sub>=10ns, CL2, BL=4, t<sub>RRD</sub>=2\*t<sub>CK</sub>, t<sub>RCD</sub>=3\*t<sub>CK</sub>, Read with Autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 repeat the same timing with random address changing; 100% of data changing at every burst
  - DDR266 (133MHz, CL=2.5) : t<sub>CK</sub>=7.5ns, CL=2.5, BL=4, t<sub>RRD</sub>=3\*t<sub>CK</sub>, t<sub>RCD</sub>=3\*t<sub>CK</sub>  
Read with Autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
  - DDR266 (133MHz, CL=2) : t<sub>CK</sub>=7.5ns, CL2=2, BL=4, t<sub>RRD</sub>=2\*t<sub>CK</sub>, t<sub>RCD</sub>=2\*t<sub>CK</sub>  
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend:

A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3

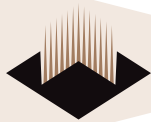


**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

0°C ≤ T<sub>A</sub> ≤ +70°C; V<sub>CC</sub> = +2.5V ±0.2V, V<sub>CCQ</sub> = +2.5V ±0.2V

AC Characteristics		262/265		202				
Parameter	Symbol	Min	Max	Min	Max	Units	Notes	
Access window of DQs from CK, CK#	t <sub>AC</sub>	-0.75	+0.75	-0.8	+0.8	ns		
CK high-level width	t <sub>CH</sub>	0.45	0.55	0.45	0.55	t <sub>CK</sub>	16	
CK low-level width	t <sub>CL</sub>	0.45	0.55	0.45	0.55	t <sub>CK</sub>	16	
Clock cycle time	CL=2.5	t <sub>CK</sub> (2.5)	7.5	13	8	13	ns	22
	CL=2	t <sub>CK</sub> (2)	7.5/10	13	10	13	ns	22
DQ and DM input hold time relative to DQS	t <sub>DH</sub>	0.5		0.6		ns	14,17	
DQ and DM input setup time relative to DQS	t <sub>DS</sub>	0.5		0.6		ns	14,17	
DQ and DM input pulse width (for each input)	t <sub>DIPW</sub>	1.75		2		ns	17	
Access window of DQS from CK, CK#	t <sub>DQSQCK</sub>	-0.75	+0.75	-0.8	+0.8	ns		
DQS input high pulse width	t <sub>DQSH</sub>	0.35		0.35		t <sub>CK</sub>		
DQS input low pulse width	t <sub>DQSL</sub>	0.35		0.35		t <sub>CK</sub>		
DQS-DQ skew, DQS to last DQ valid, per group, per access	t <sub>DQSQ</sub>		0.5		0.6	ns	13,14	
Write command to first DQS latching transition	t <sub>DQSS</sub>	0.75	1.25	0.75	1.25	t <sub>CK</sub>		
DQS falling edge to CK rising - setup time	t <sub>DSS</sub>	0.2		0.2		t <sub>CK</sub>		
DQS falling edge from CK rising - hold time	t <sub>DSH</sub>	0.2		0.2		t <sub>CK</sub>		
Half clock period	t <sub>HP</sub>	t <sub>CH</sub> , t <sub>CL</sub>		t <sub>CH</sub> , t <sub>CL</sub>		ns	18	
Data-out high-impedance window from CK, CK#	t <sub>HZ</sub>		+0.75		+0.8	ns	8,19	
Data-out low-impedance window from CK, CK#	t <sub>LZ</sub>	-0.75		-0.8		ns	8,20	
Address and control input hold time (fast slew rate)	t <sub>IHF</sub>	0.90		1.1		ns	6	
Address and control input set-up time (fast slew rate)	t <sub>ISF</sub>	0.90		1.1		ns	6	
Address and control input hold time (slow slew rate)	t <sub>IHS</sub>	1		1.1		ns	6	
Address and control input setup time (slow slew rate)	t <sub>ISS</sub>	1		1.1		ns	6	
Address and control input pulse width (for each input)	t <sub>IPW</sub>	2.2		2.2		ns		
LOAD MODE REGISTER command cycle time	t <sub>MRD</sub>	15		16		ns		
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t <sub>QH</sub>	t <sub>HP</sub> -t <sub>QHS</sub>		t <sub>HP</sub> -t <sub>QHS</sub>		ns	13,14	
Data hold skew factor	t <sub>QHS</sub>		0.75		1	ns		
ACTIVE to PRECHARGE command	t <sub>RAS</sub>	40	120,000	40	120,000	ns	15	
ACTIVE to READ with Auto precharge command	t <sub>RAP</sub>	15		20		ns		
ACTIVE to ACTIVE/AUTO REFRESH command period	t <sub>RC</sub>	60		70		ns		
AUTO REFRESH command period	t <sub>RFC</sub>	75		80		ns	21	





**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED AC OPERATING CONDITIONS (continued)**

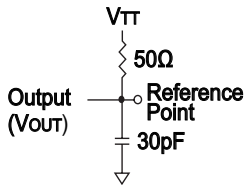
0°C ≤ T<sub>A</sub> ≤ +70°C; V<sub>CC</sub> = +2.5V ±0.2V, V<sub>CCQ</sub> = +2.5V ±0.2V

AC Characteristics		262/265		202			
Parameter	Symbol	Min	Max	Min	Max	Units	Notes
ACTIVE to READ or WRITE delay	t <sub>RCD</sub>	15		20		ns	
PRECHARGE command period	t <sub>RP</sub>	15		20		ns	
DQS read preamble	t <sub>RPRE</sub>	0.9	1.1	0.9	1.1	t <sub>CK</sub>	19
DQS read postamble	t <sub>RPST</sub>	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
ACTIVE bank a to ACTIVE bank b command	t <sub>RRD</sub>	12		15		ns	
DQS write preamble	t <sub>WPRE</sub>	0.25		0.25		t <sub>CK</sub>	
DQS write preamble setup time	t <sub>WPRES</sub>	0		0		ns	10,11
DQS write postamble	t <sub>WPST</sub>	0.4	0.6	0.4	0.6	t <sub>CK</sub>	9
Write recovery time	t <sub>WR</sub>	15		15		ns	
Internal WRITE to READ command delay	t <sub>WTR</sub>	1		1		t <sub>CK</sub>	
Data valid output window	NA	t <sub>AH</sub> -t <sub>DOAQ</sub>		t <sub>AH</sub> -t <sub>DOAQ</sub>		ns	13
REFRESH to REFRESH command interval	t <sub>REFC</sub>		140.6		140.6	μs	12
Average periodic refresh interval	t <sub>REFI</sub>		15.6		15.6	μs	12
Terminating voltage delay to V <sub>CC</sub>	t <sub>1TD</sub>	0		0		ns	
Exit SELF REFRESH to non-READ command	t <sub>XSNR</sub>	75		80		ns	
Exit SELF REFRESH to READ command	t <sub>XSRD</sub>	200		200		t <sub>CK</sub>	



## Notes

1. All voltages referenced to  $V_{SS}$
2. Tests for AC timing,  $I_{DD}$ , and electrical AC and DC characteristics may be conducted at normal reference / supply voltage levels, but the related specifications and device operations are guaranteed for the full voltage range specified.
3. Outputs are measured with equivalent load:



4. AC timing and  $I_{DD}$  tests may use a  $V_{IL}$ -to- $V_{IH}$  swing of up to 1.5V in the test environment, but input timing is still referenced to  $V_{REF}$  (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between  $V_{IL}(AC)$  and  $V_{IH}(AC)$ .
5. The AC and DC input level specifications are defined in the SSTL\_2 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [high] level).
6. For slew rates less than 1V/ns and greater than or equal to 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated:  $t_{is}$  has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns.  $t_{IH}$  has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain. For 266, slew rates must be greater than or equal to 0.5V/ns.
7. Inputs are not recognized as valid until  $V_{REF}$  stabilizes. Exception: during the period before  $V_{REF}$  stabilizes,  $CKE \leq 0.3 \times V_{CCQ}$  is recognized as LOW.
8.  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) and begins driving (LZ).
9. The intent of the "Don't Care" state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW, or high-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above  $V_{IHDC}$  (MIN)) then it must not transition LOW (below  $V_{IHDC}$ ) prior to  $t_{DQSH}$  (MIN).
10. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
11. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be high during this time, depending on  $t_{DQSS}$ .
12. The refresh period is 64ms. This equates to an average refresh rate of 15.625 $\mu$ s. However, an AUTO REFRESH command must be asserted at least once every 140.6 $\mu$ s; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
13. The valid data window is derived by achieving other specifications -  $t_{HP}$  ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycled variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
14. Referenced to each output group:  $x8 = DQS$  with DQ0-DQ7.
15. READs and WRITEs with auto precharge are not allowed to be issued until  $t_{RAS}$  (MIN) can be satisfied prior to the internal precharge command being issued.
16. JEDEC specifies CK and CK# input slew rate must be  $\geq 1V/ns$  (2V/ns differentially).
17. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to  $t_{DS}$  and  $t_{DH}$  for each 100mV/ns reduction in slew rate. If slew rates exceed 4V/ns, functionality is uncertain.
18.  $t_{HP}$  min is the lesser of  $t_{CL}$  min and  $t_{CH}$  min actually applied to the device CK and CK# inputs, collectively during bank active.
19.  $t_{HZ}$  (MAX) will prevail over the  $t_{DQSQ}$  (MAX) +  $t_{RPST}$  (MAX) condition.  $t_{LZ}$  (MIN) will prevail over  $t_{DQSQ}$  (MIN) + PRE (MAX) condition.
20. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
21. CKE must be active (High) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until  $t_{RFC}$  has been satisfied.
22. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).

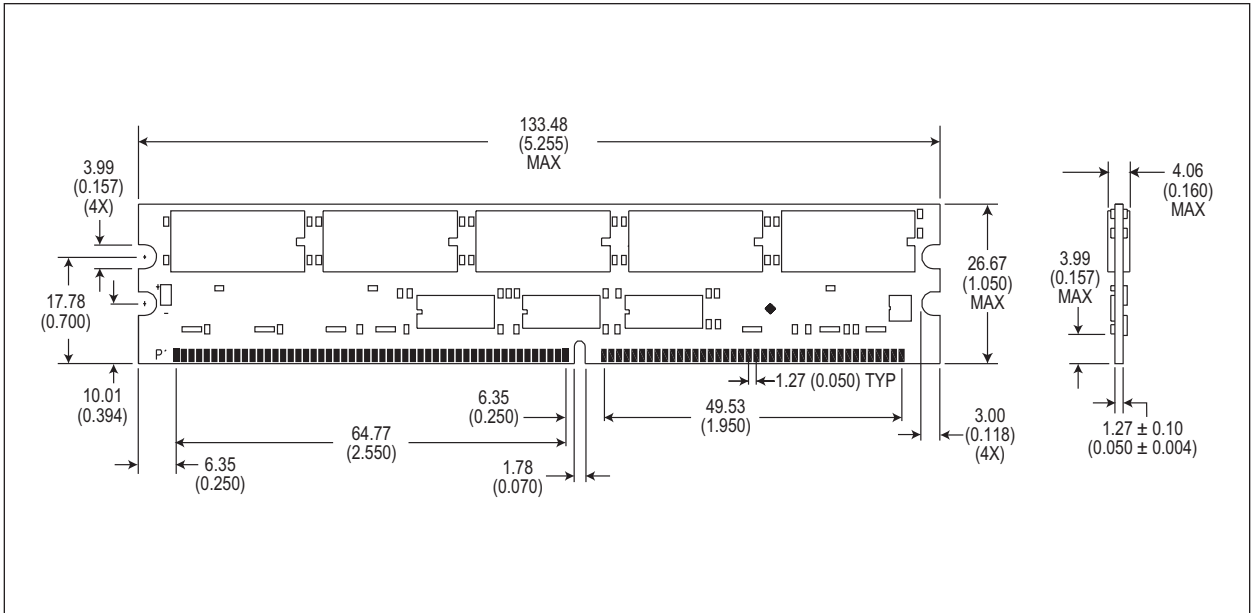


ORDER INFORMATION FOR D3

Part Number	Speed	CAS Latency	trCD	trP	Height*
W3EG7217S262D3	133MHz/266Mbps	2	2	2	26.67 (1.05")
W3EG7217S265D3	133MHz/266Mbps	2.5	3	3	26.67 (1.05")
W3EG7217S202D3	100MHz/200Mbps	2	2	2	26.67 (1.05")

Note: Consult factory for availability of lead-free products (F = Lead-Free, G = RoHS compliant)

PACKAGE DIMENSIONS FOR D3



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

**Document Title**

128MB – 16Mx72 DDR SDRAM REGISTERED

**Revision History**

<b>Rev #</b>	<b>History</b>	<b>Release Date</b>	<b>Status</b>
Rev A	Created	5-22-02	Advanced
Rev 0	0.1 Updated I <sub>DD</sub> and CAP specs 0.2 Added AC Specs 0.3 Moved from Advanced to Preliminary	11-04	Preliminary
Rev 1	1.0 Added lead-free and RoHS notes 1.1 Moved from Preliminary to Final	12-04	Final