3W Mono Fully Differential Audio Power Amplifier

Features

- **Operating Voltage: 2.4V~5.5V**
- **Fully Differential Class-AB Amplifier**
- **High PSRR and Excellent RF Rectification Immunity**
- **Low Crosstalk**
- **3W Output Power into 3Ω Load at V_{DD}=5V**
- **Thermal and Over-Current Protections**
- **Low Supply Current :1.5mA Typical**
- **Space Saving Package**
  -MSOP-8
  -MSOP-8P
  -TDFN3x3-8
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APA0715 is a Mono, fully differential Class-AB audio amplifier which can operate with supply voltage from 2.4V to 5V and is available in a MSOP8, MSOP8P, or TDFN3x3-8 package.

High PSRR and fully differential architecture increase immunity to noise and RF rectification. In addition to these features, a short startup time and small package size make the APA0715 an ideal choice for Mobil Phones and Portable Devices.

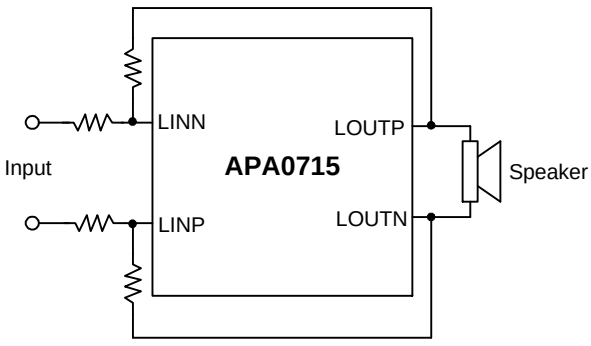
The APA0715 also integrates the de-pop circuitry that reduces the pops and click noises during power on/off and shutdown mode operation. Both Thermal and over-current protections are integrated to avoid the IC being destroyed by over temperature and short-circuit.

The APA0715 is capable of driving 3W at 5V into 3Ω speaker.

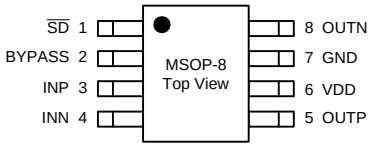
Applications

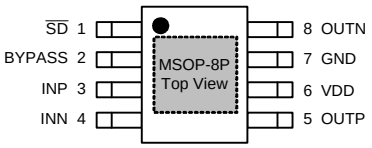
- **Mobil Phones**
- **Portable Devices**

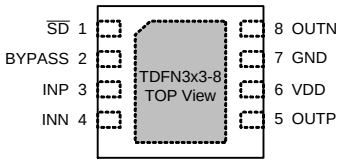
Simplified Application Circuit



Pin Configuration



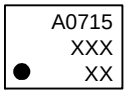
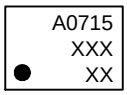
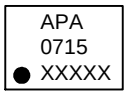




=Thermal Pad (connected the Thermal Pad to GND plane for better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APA0715 □□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code X : MSOP-8 XA : MSOP-8P QB : TDFN3x3-8 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APA0715 X : 	XXXXX - Date Code
APA0715 XA : 	XXXXX - Date Code
APA0715 QB : 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6	V
V_{IN}	Input Voltage (INN, INP, $\overline{SD}$ to GND)	-0.3 to 6	V
	Input Voltage (OUTN, OUTP to GND)	-0.3 to V_{DD} +0.3	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Soldering Temperature Range, 10 Seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Thermal Characteristics (Note 2,3)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient MSOP-8 MSOP-8P TDFN3x3-8	 200 52 54	°C /W
θ_{JC}	Thermal Resistance -Junction to Case MSOP-8P TDFN3x3-8	 10 11	°C /W

Note 2: Please refer to " Layout Recommendation", the Thermal Pad on the bottom of the IC should soldered directly to the PCB's ThermalPad area that with several thermal vias connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Note 3: The case temperature is measured at the center of the Thermal Pad on the underside of the MSOP-8P and TDFN3x3-8 package.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		2.4 ~ 5.5	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$	1.8 ~ V_{DD}	V
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$	0 ~ 0.35	V
V_{IC}	Common Mode Input Voltage		0.5 ~ V_{DD}-0.5	
	Operating Ambient Temperature Range		-40 ~ 85	°C
	Operating Junction Temperature Range		-40 ~ 125	°C
	Speaker Resistance		3 ~	Ω

Electrical Characteristics

V_{DD}=5V, GND=0V, A_V=1V/V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA0715 Min.	APA0715 Typ.	APA0715 Max.	Unit
I_{DD}	Supply Current			-	1.5	3	mA
I_{SD}	Shutdown Current	$\overline{SD}$ = 0V		-	-	5	μA
I_I	Input Current	$\overline{SD}$		-	0.1	-	μA
$T_{START-UP}$	Start-Up Time from End of Shutdown	C_b=0.22μF		-	50	-	ms
R_{SD}	Resistance from Shutdown to GND			90	100	110	kΩ
V_{DD}=5V, T_A=25°C							
P_O	Output Power	THD+N = 1%	R_L = 3Ω	-	2.4	-	W
			R_L = 4Ω	-	2.1	-	
			R_L = 8Ω	1	1.3	-	
		THD+N = 10% f_{in} = 1kHz	R_L = 3Ω	-	3	-	
			R_L = 4Ω	-	2.6	-	
			R_L = 8Ω	-	1.6	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in} = 1kHz	R_L = 8Ω P_O= 0.9W	-	0.035	-	%
PSRR	Power Supply Rejection Ratio	C_b= 0.22μF, R_L = 8Ω, V_{RR}=0.2V_{PP}, f_{in} = 217Hz		-	75	-	dB

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Electrical Characteristics (Cont.)

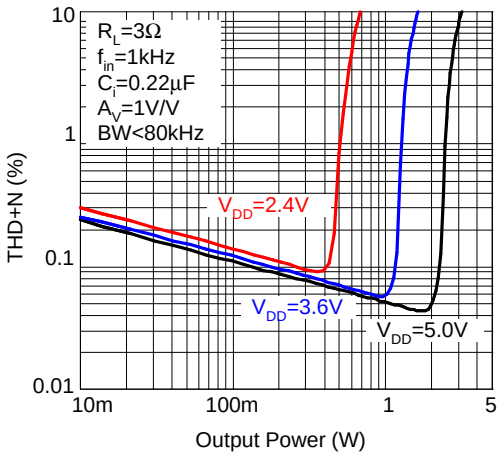
V_{DD}=5V, GND=0V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA0715			Unit
				Min.	Typ.	Max.	
V_{DD}=5V, T_A=25℃ (CONT.)							
CMRR	Common-Mode Rejection Ratio	C_b= 0.22µF, R_L = 8Ω, V_{IC}=0.2V_{PP}, f_{in} = 217Hz		-	85	-	dB
S/N	Signal to Noise Ratio	With A-weighting Filter P_O = 1.3W, R_L = 8Ω		-	112	-	dB
V_{OS}	Output Offset Voltage	R_L = 8Ω		-	5	20	mV
Vn	Noise Output Voltage	C_b= 0.22µF, With A-weighting Filter		-	8	-	µV (rms)
V_{DD}=3.6V, T_A=25℃							
P_O	Output Power	THD+N = 1%	R_L = 3Ω	-	1.2	-	W
			R_L = 4Ω	-	1	-	
			R_L = 8Ω	-	0.65	-	
		THD+N = 10% f_{in} = 1kHz	R_L = 3Ω	-	1.5	-	
			R_L = 4Ω	-	1.3	-	
			R_L = 8Ω	-	0.8	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in} = 1kHz	R_L = 8Ω P_O= 0.45W	-	0.05	-	%
PSRR	Power Supply Rejection Ratio	C_b= 0.22µF, R_L = 8Ω, V_{RR}=0.2V_{PP}, f_{in} = 217Hz		-	85	-	dB
CMRR	Common-Mode Rejection Ratio	C_b= 0.22µF, R_L = 8Ω, V_{IC}=0.2V_{PP}, f_{in} = 217Hz		-	75	-	
S/N	Signal to Noise Ratio	With A-weighting Filter P_O = 0.65W, R_L = 8Ω		-	110	-	
V_{OS}	Output Offset Voltage	R_L = 8Ω		-	5	20	mV
Vn	Noise Output Voltage	C_b= 0.22µF, With A-weighting Filter		-	7	-	µV (rms)
V_{DD}=2.4V, T_A=25℃							
P_O	Output Power	THD+N = 1%	R_L = 3Ω	-	0. 5	-	W
			R_L = 4Ω	-	0.45	-	
			R_L = 8Ω	-	0.3	-	
		THD+N = 10% f_{in} = 1kHz	R_L = 3Ω	-	0.7	-	
			R_L = 4Ω	-	0.6	-	
			R_L = 8Ω	-	0.35	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in} = 1kHz	P_O = 0.2W, R_L = 8Ω	-	0.08	-	%
PSRR	Power Supply Rejection Ratio	C_b= 0.22µF, R_L = 8Ω, V_{RR}=0.2V_{PP}, f_{in} = 217Hz		-	80	-	dB
CMRR	Common-Mode Rejection Ratio	C_b= 0.22µF, R_L = 8Ω, V_{IC}=0.2V_{PP}, f_{in} = 217Hz		-	65	-	
S/N	Signal to Noise Ratio	With A-weighting Filter P_O = 0.3W, R_L = 8Ω		-	106	-	
V_{OS}	Output Offset Voltage	R_L = 8Ω		-	5	20	mV
Vn	Noise Output Voltage	C_b= 0.22µF, With A-weighting Filter		-	7	-	µV (rms)

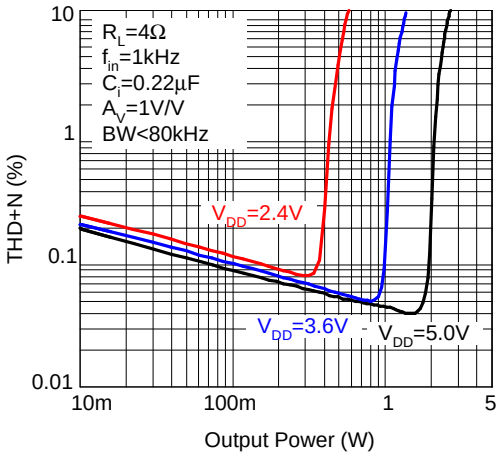
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Typical Operating Characteristics

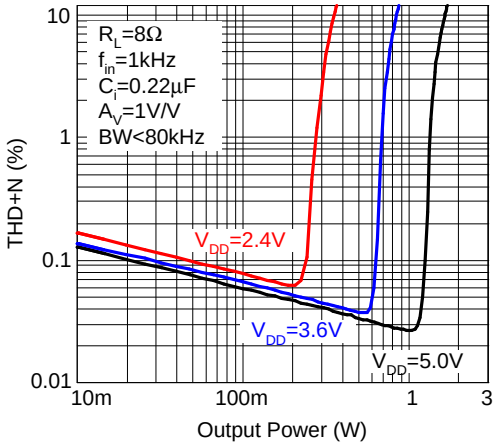
THD+N vs. Output Power



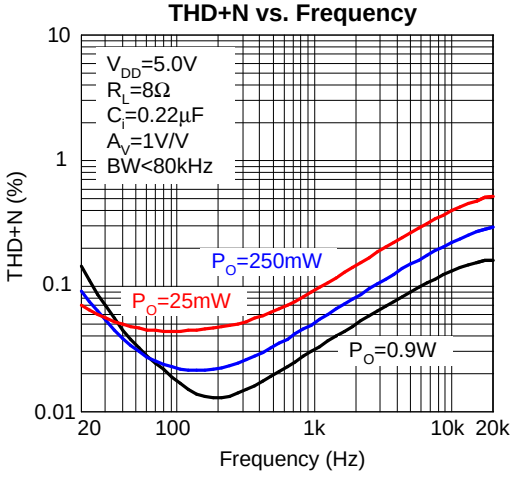
THD+N vs. Output Power



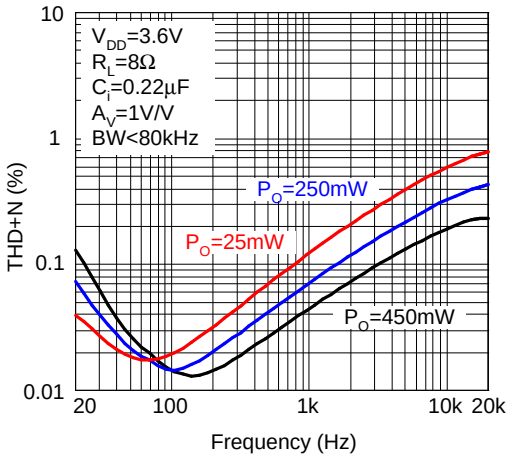
THD+N vs. Output Power



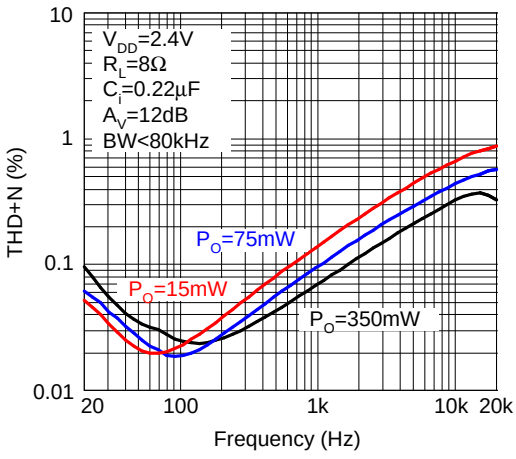
THD+N vs. Frequency



THD+N vs. Frequency



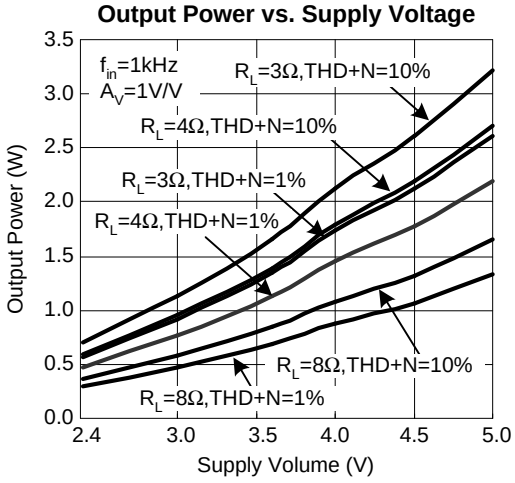
THD+N vs. Frequency



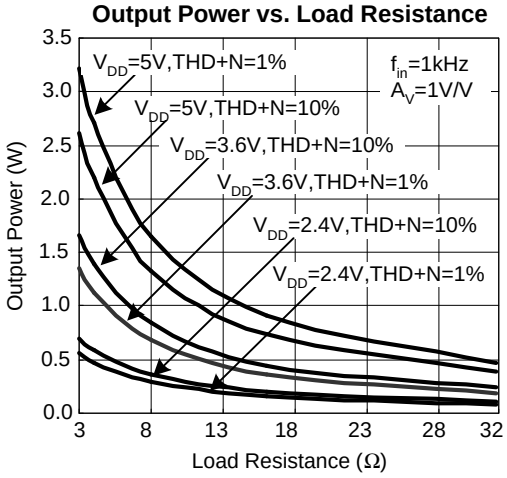
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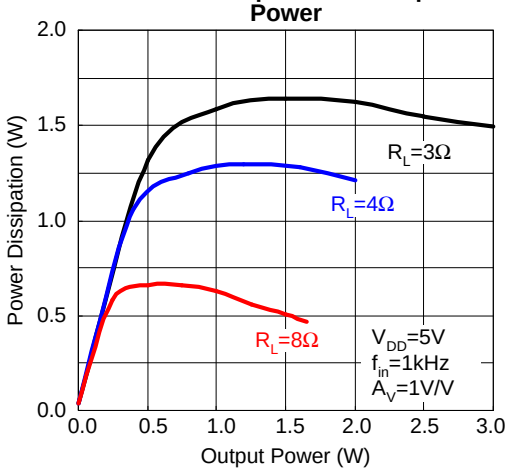
Output Power vs. Supply Voltage



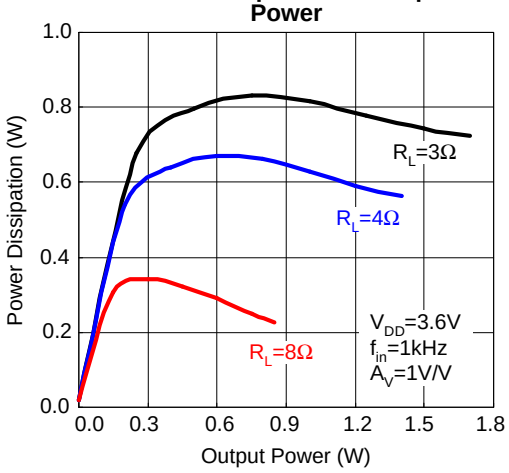
Output Power vs. Load Resistance



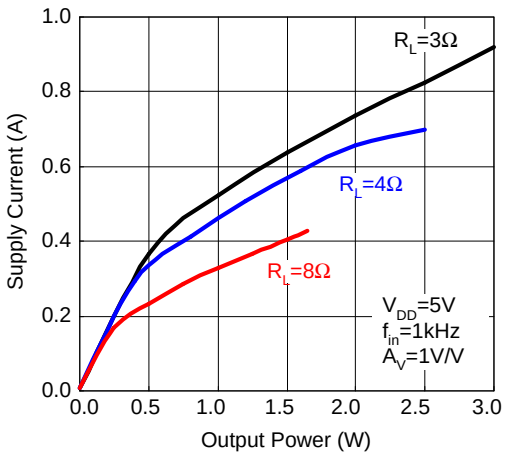
Power Dissipation vs. Output Power



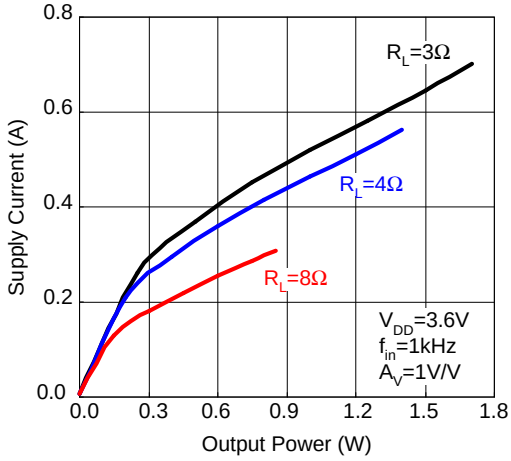
Power Dissipation vs. Output Power



Supply Current vs. Output Power



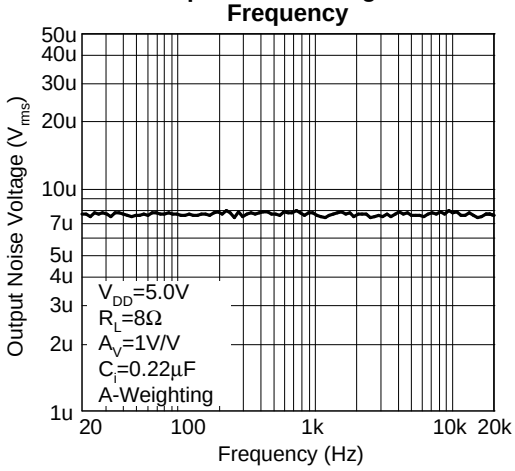
Supply Current vs. Output Power



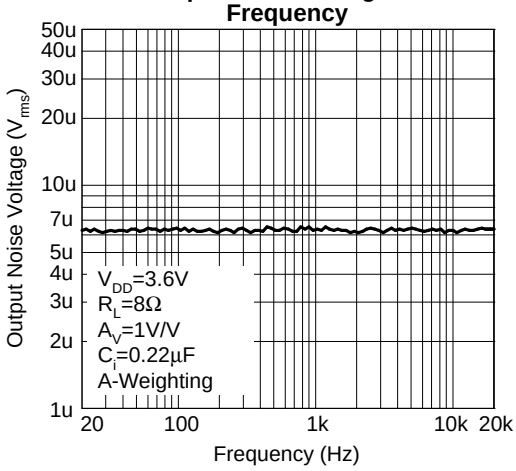
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Typical Operating Characteristics (Cont.)

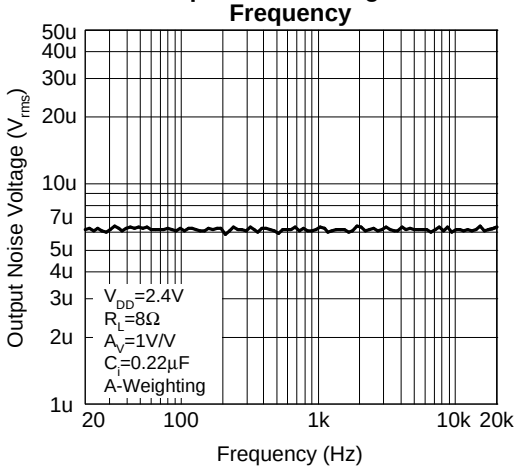
Output Noise Voltage vs. Frequency



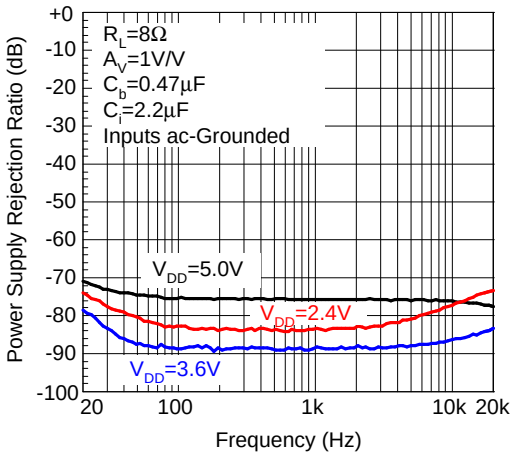
Output Noise Voltage vs. Frequency



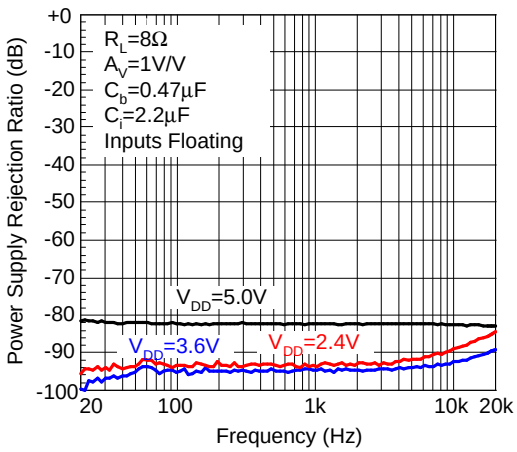
Output Noise Voltage vs. Frequency



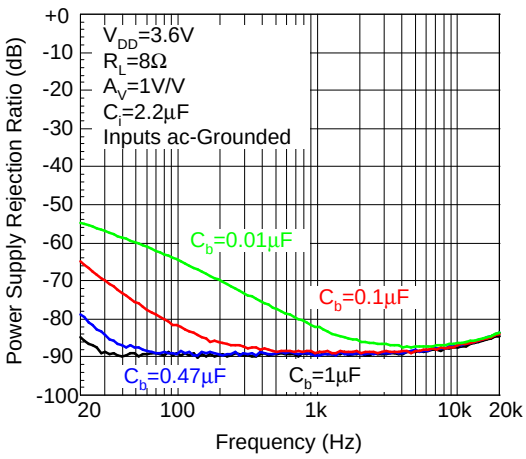
PSRR vs. Frequency



PSRR vs. Frequency



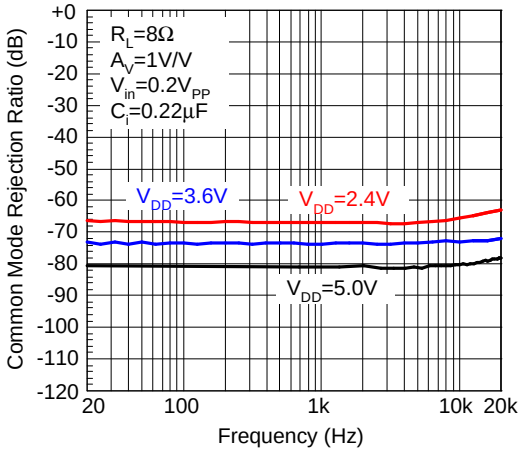
PSRR vs. Frequency



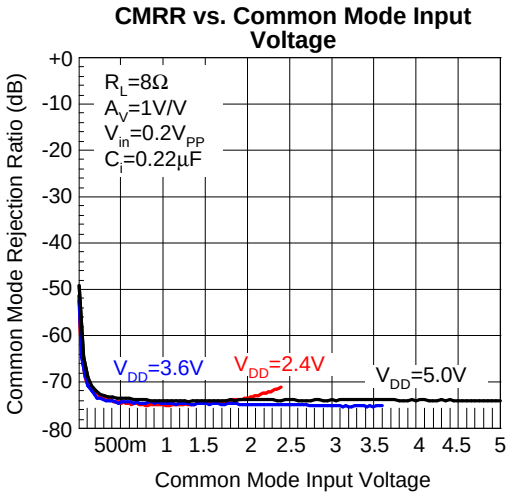
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Typical Operating Characteristics (Cont.)

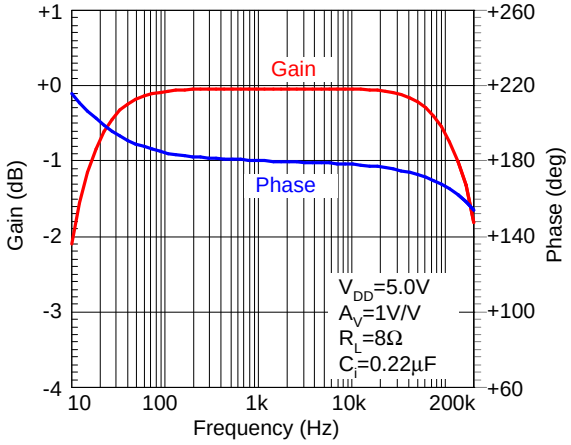
CMRR vs. Frequency



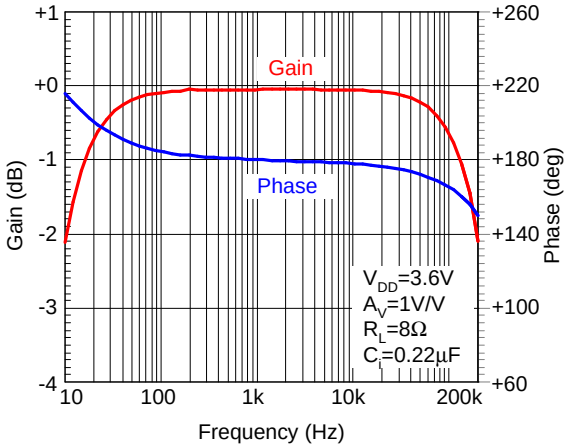
CMRR vs. Common Mode Input Voltage



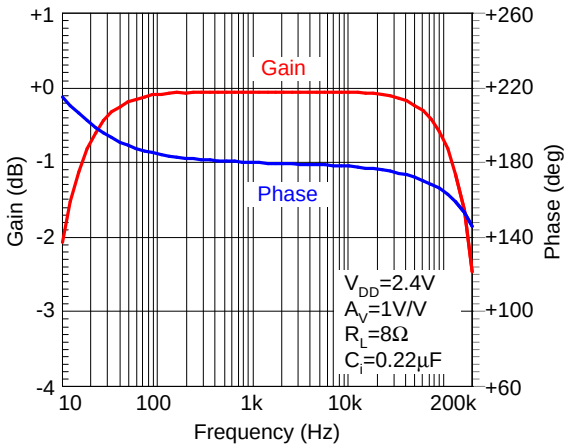
Frequency Response



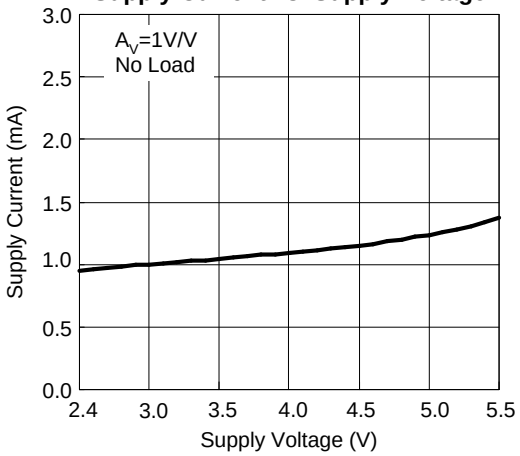
Frequency Response



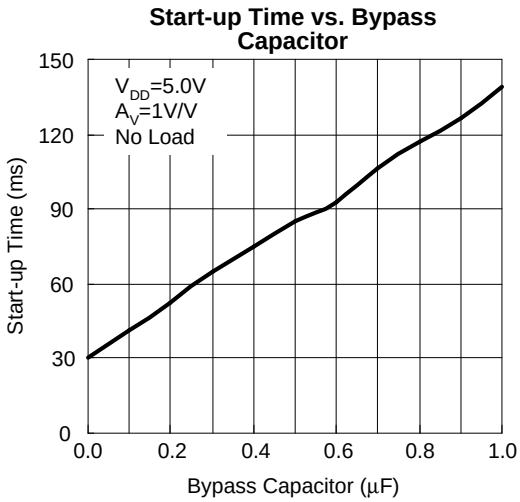
Frequency Response

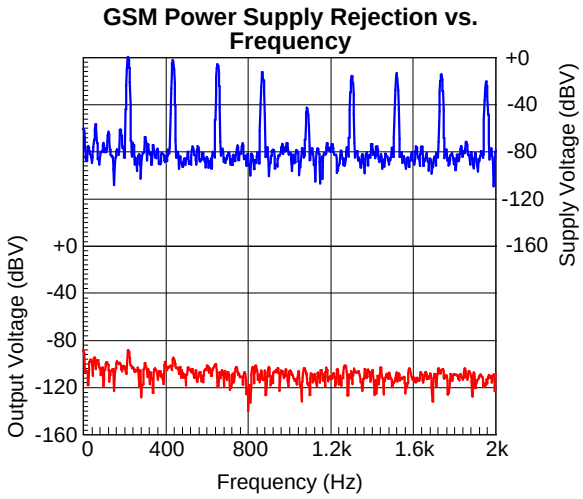


Supply Current vs. Supply Voltage



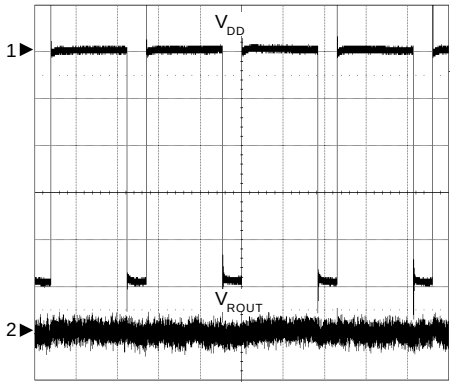
Typical Operating Characteristics (Cont.)





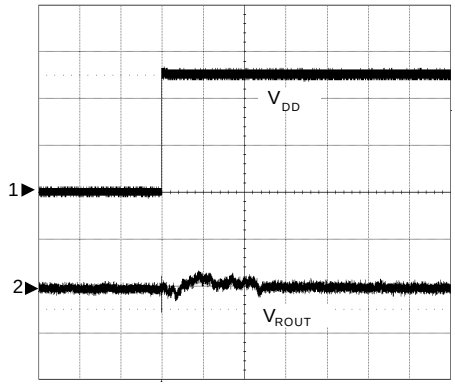
Operating Waveforms

GSM Power Supply Rejection vs. Time



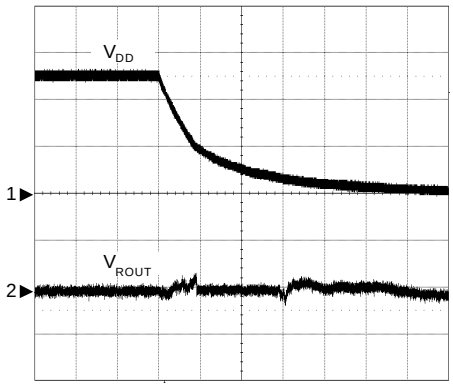
CH1: V_{DD}, 100mV/Div, DC, V_{DD} Offset =5.0V
CH2: V_{ROUT}, 20mV/Div, DC
TIME: 2ms/Div

Power On



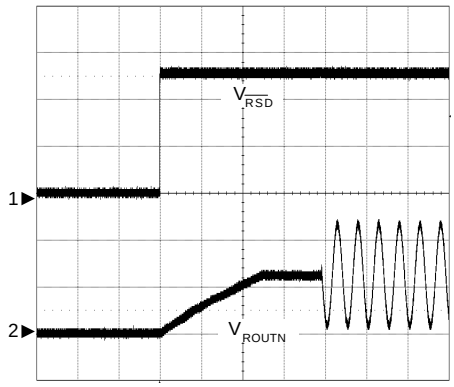
CH1: V_{DD}, 2V/Div, DC
CH2: V_{ROUT}, 50mV/Div, DC
TIME: 20ms/Div

Power Off



CH1: V_{DD}, 2V/Div, DC
CH2: V_{ROUT}, 50mV/Div, DC
TIME: 50ms/Div

Shutdown Release

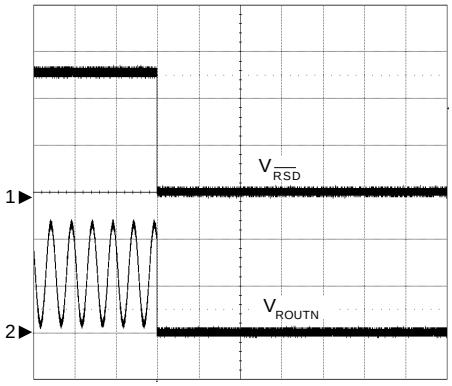


CH1: $V_{\overline{RSD}}$, 2V/Div, DC
CH2: V_{ROUTN}, 2V/Div, DC
TIME: 20ms/Div

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Operating Waveforms (Cont.)

Shutdown



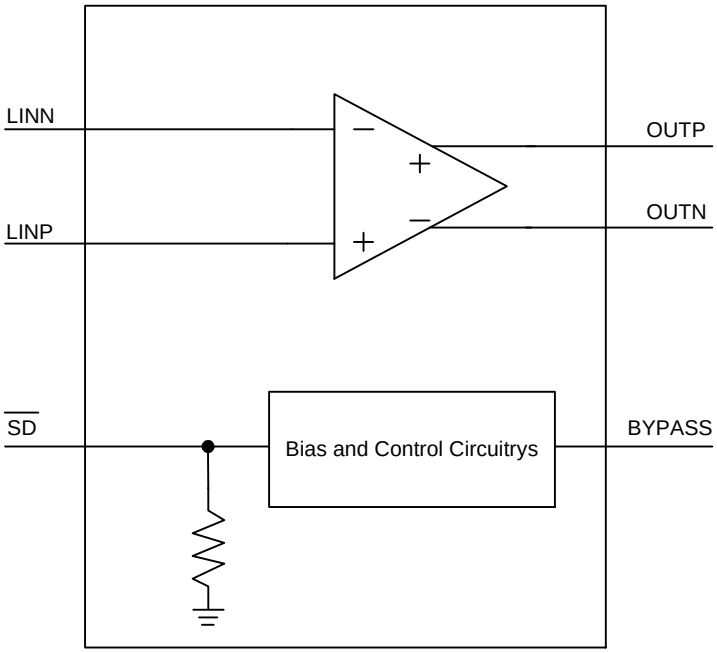
CH1: $V_{\overline{RSD}}$, 2V/Div, DC
CH2: V_{ROUTN}, 2V/Div, DC
TIME: 20ms/Div

Pin Description

PIN		I/O/P	FUNCTION
NO.	NAME		
1	$\overline{SD}$	I	Shutdown mode control signal input, place left channel speaker amplifier in shutdown mode when held low.
2	BYPASS	P	Bypass voltage input pin
3	INP	I	The non-inverting input of amplifier. INP is via a capacitor to Gnd for single-end (SE) input signal.
4	INN	I	The inverting input of amplifier. INN is used as audio input terminal, typically.
5	ROUTP	O	The positive output terminal of speaker amplifier.
6	VDD	P	Supply voltage input pin
7	GND	P	Ground connection for circuitry.
8	LOUTN	O	The negative output terminal of speaker amplifier.

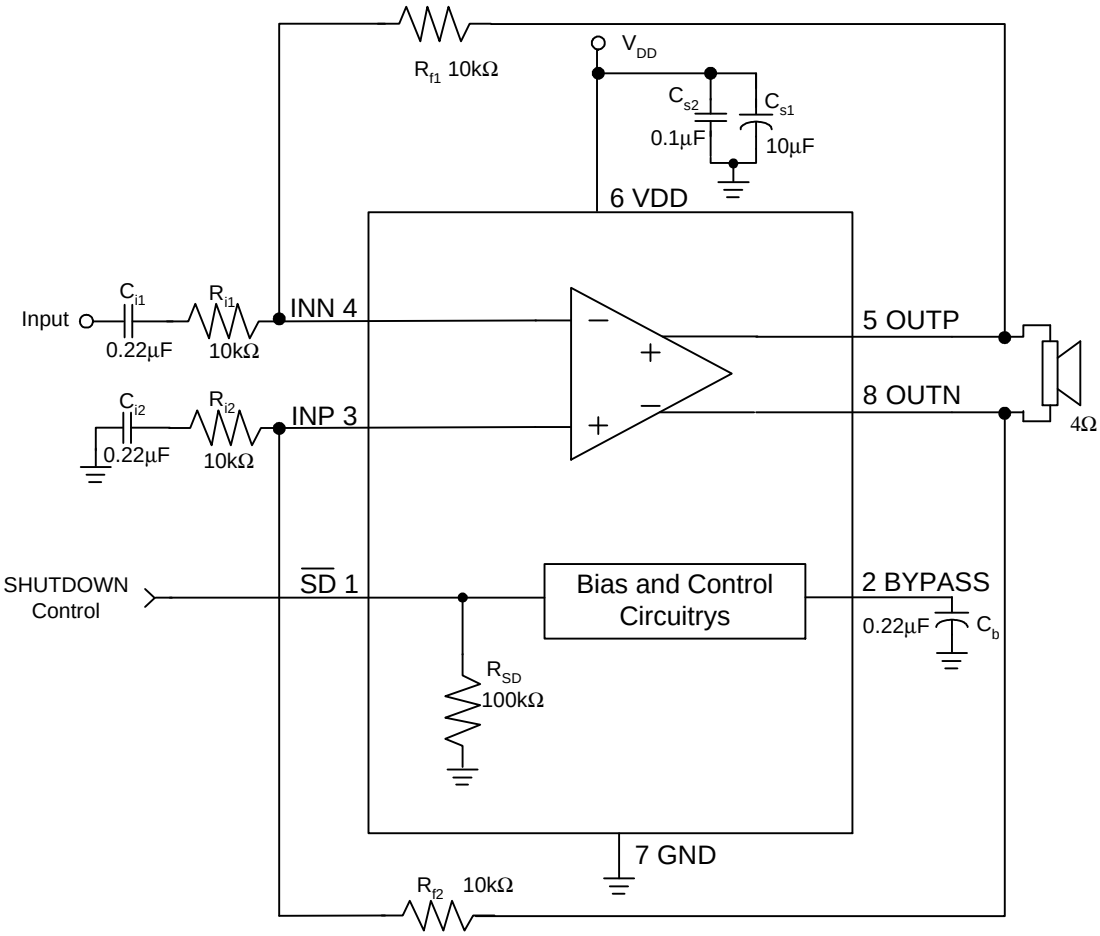
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Block Diagram



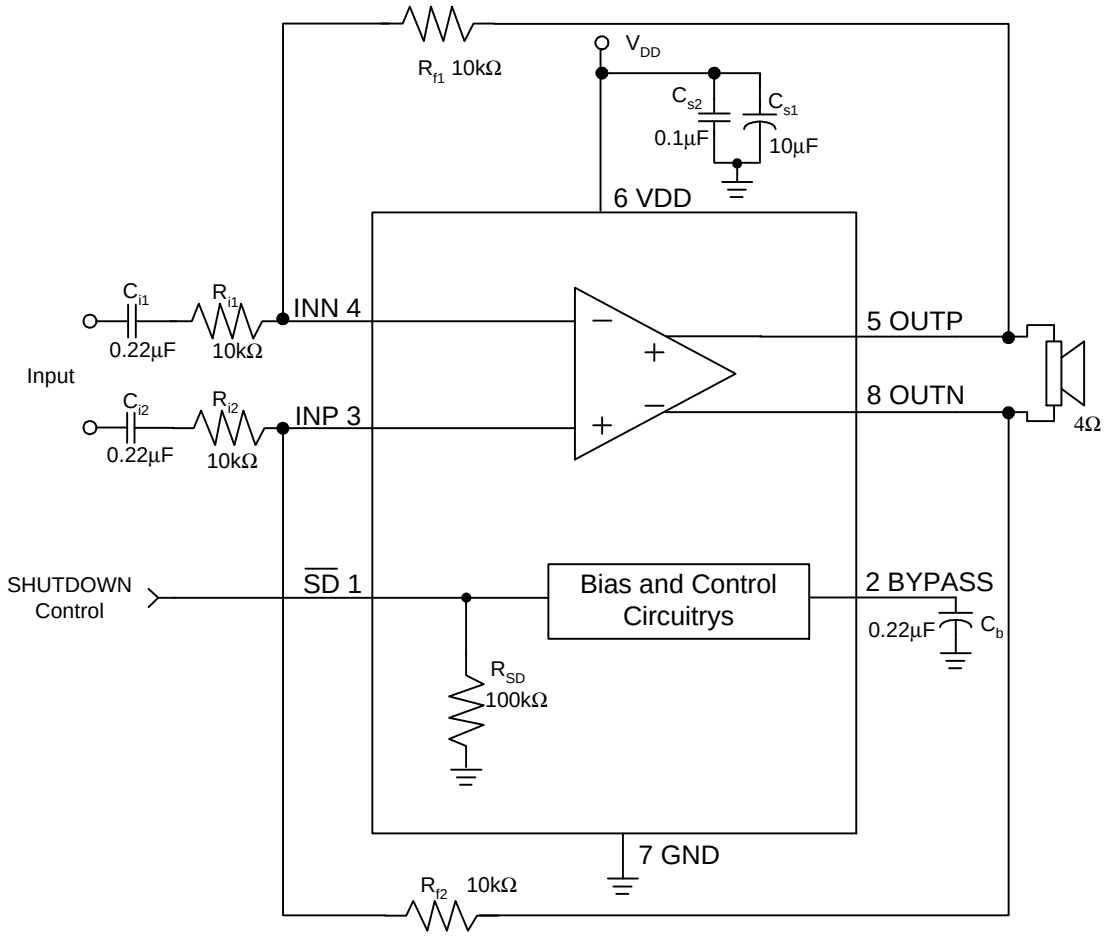
Typical Application Circuits

Single-ended input mode



Typical Application Circuits (Cont.)

Differential input mode



Function Description

Fully Differential Amplifier

The power amplifiers are fully differential amplifiers with differential inputs and outputs. The fully differential amplifier has some advantages versus traditional amplifiers. First, don't need the input coupling capacitors because the common-mode feedback compensates the input bias. The inputs can be biased from 0.5V to V_{DD}-0.5V, and the outputs are still biased at mid-supply of the power amplifier. If the inputs are biased out of the input range, the coupling capacitors are required. Second, the fully differential amplifier has outstanding immunity against supply voltage ripple (217Hz) cuased by the GSM RF transmitters' signal which is better than the typical audio amplifier.

Thermal Protection

The over-temperature circuit limits the junction temperature of the APA0715. When the junction temperature exceeds T_J = +150°C, a thermal sensor turns off the amplifiers, allowing the device to cool. The thermal sensor allows the amplifiers to start-up after the junction temperature cools down to about 125 °C. The thermal protection is designed with a 25 °C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Over-Current Protection

The APA0715 monitors the output buffers' current. When the over-current occurs, the output buffers' current will be reduced and limited to a fold-back current level.
The power amplifier will go back to normal operation until the over-current situation has been removed. In addition, if the over-current period is long enough and the IC's junction temperature reaches the thermal protection threshold, the IC enters thermal protection mode.

Shutdown Function

In order to reduce power consumption while not in use, the APA0715 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the SD pin for APA0715. The trigger point between a logic high and logic low level is typically 1.8V. It is best to switch between the ground and the supply voltage VDD to provide maximum device performance. By switching the SD pin to a low level, the amplifier enters a low-consumption-current state, IDD for APA0715 is in shutdown mode. Under normal operating, APA0715's SD pin should pull to a high level to keep the IC out of the shutdown mode. The SD pin should be tied to a definite voltage to avoid unwanted state changing.

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Application Information

Input Resistance (R_i) and Feedback Resistance (R_f)

The gain for the APA0715 is set by the external input resistors (R_i) and external feedback resistors (R_f).

$$Av = \frac{R_f}{R_i} \quad (1)$$

R_i and R_f should range from 1kΩ to 100kΩ. R_i is 10kΩ recommended. For the performance of a fully differential amplifier, it's better to select matching input resistors R_{i1} and R_{i2}. Therefore, 1% tolerance resistors are recommended. If the input resistors are not matched, the CMRR and PSRR performance are worse than using matching devices.

Input Capacitor (C_i)

When the APA0715 is driven by a differential input source, the input capacitor may not be required.

In the single-ended input application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input resistance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$F_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (2)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where R_i is 10kΩ and the specification that calls for a flat bass response down to 100Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i F_c} \quad (3)$$

When the input resistance variation is considered, the C_i is 0.16μF. Therefore, a value in the range of 0.22μF to 0.47μF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input of the amplifier. The offset reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications because the DC level of the amplifiers' inputs are held at V_{DD}/2. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor (C_{BYPASS})

The BYPASS pin sets the V_{DD}/2 for internal reference by voltage divider. Adding capacitors at this pin to filter the noise and regulator the mid-supply rail will increase the PSRR and noise performance.

The capacitors should be as close to the device as possible. The effect of a larger bypass capacitor will improve PSRR due to increased supply stability.

The bypass capacitance also affects to the start time. The large capacitors will increase the start time when device in shutdown.

Optimizing Depop Circuitry

Circuitry has been included in the APA0715 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry.

The value of C_i will also affect turn-on pops. The bypass voltage ramp up should be slower than input bias voltage. Although the BYPASS pin current source cannot be modified, the size of C_{BYPASS} can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of C_{BYPASS}, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_{BYPASS} and the turn-on time.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. Hence, it is advantageous to use low-gain configurations.

Power Supply Decoupling Capacitor (C_s)

The APA0715 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is

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Application Information (Cont.)

Power Supply Decoupling Capacitor (C_s) (Cont.)

as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noises on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically 0.1μF, is placed as close as possible to the device VDD lead works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Fully Differential Amplifier Efficiency

The traditional class AB power amplifier efficiency can be calculated starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating the amplifier efficiency.

$$\text{Efficiency}(\eta) = \frac{P_O}{P_{SUP}} \qquad (4)$$

where:

$$P_O = \frac{V_{Orms}^2}{R_L} = \frac{V_P^2}{2R_L}$$

$$V_{Orms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD} X I_{DD\ (AVG)} = \frac{2V_{DD}V_{PP}}{\pi R_L} \qquad (5)$$

$$I_{DD\ (AVG)} = \frac{2V_P}{\pi R_L}$$

So the Efficiency (η) is:

$$\text{Efficiency}(\eta) = \frac{\pi V_P}{4V_{DD}} = \frac{\pi\sqrt{2P_O R_L}}{4V_{DD}} \qquad (6)$$

Table 1 calculates efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than the dissipation in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a Mono 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 1.63W.

R_L (W)	P_O (W)	Efficiency (%)	I_{DD}(A)	P_D (W)	P_{SUP} (W)
8	0.25	30.1	0.17	0.58	0.83
	0.50	43.1	0.23	0.66	1.16
	1	61.5	0.33	0.63	1.63
	1.6	77.7	0.43	0.46	2.06
4	0.4	27.5	0.29	1.06	1.46
	1.2	48.1	0.51	1.30	2.50
	2	62.4	0.66	1.21	3.21
	2.6	74.1	0.70	0.91	3.51
3	0.5	27.5	0.37	1.32	1.82
	1	38.7	0.52	1.58	2.58
	2	55.1	0.74	1.63	3.63
	3	66.8	0.92	1.49	4.49

Table 1: Efficiency vs. Output Power in 5-V Differential Amplifier Syetems

A final point to remember about linear amplifiers (either SE or Differential) is how to manipulate the terms in the efficiency equation to an utmost advantage when possible. Note that in equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Layout Recommendation

1. All components should be placed close to the APA0715. For example, the input capacitor (C_i) should be close to APA0715's input pins to avoid causing noise coupling to APA0715's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA0715's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The MSOP-8P and DFN3x3-8 Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short circuit) except the Thermal PAD area.

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Application Information (Cont.)

Layout Recommendation (Cont.)

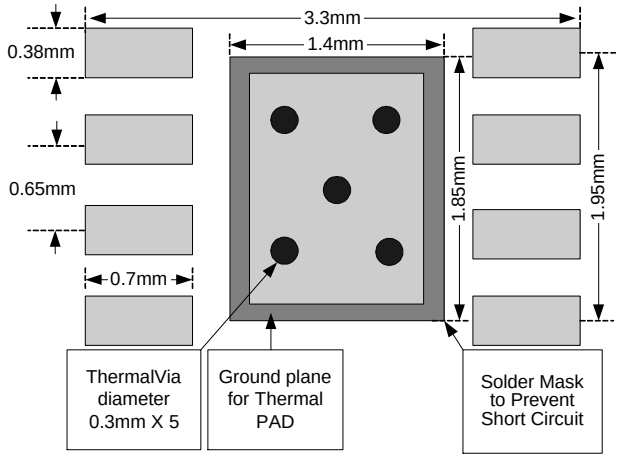
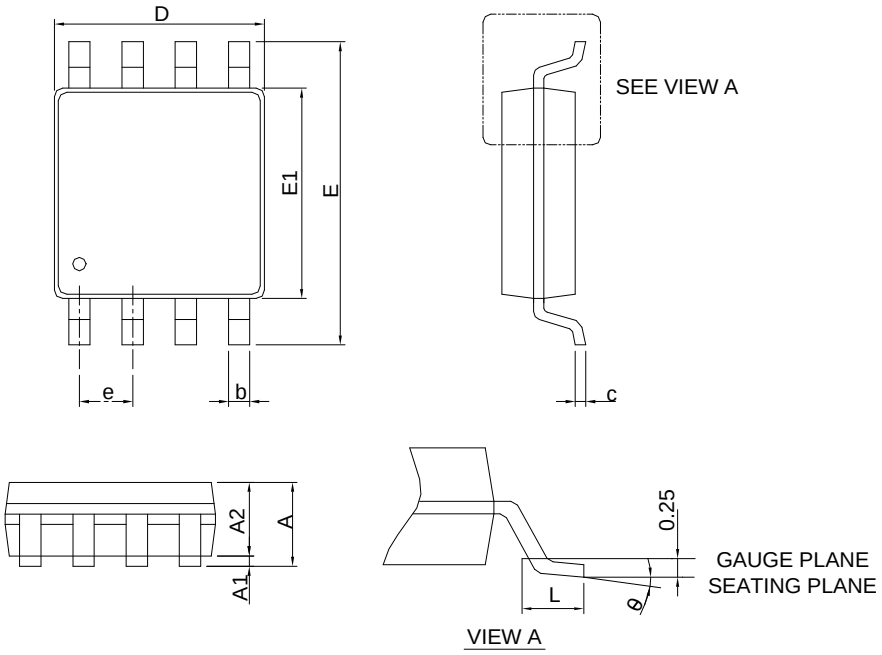


Figure 1:TDFN3X3-8 Land Pattern Recommendation

Package Information

MSOP-8



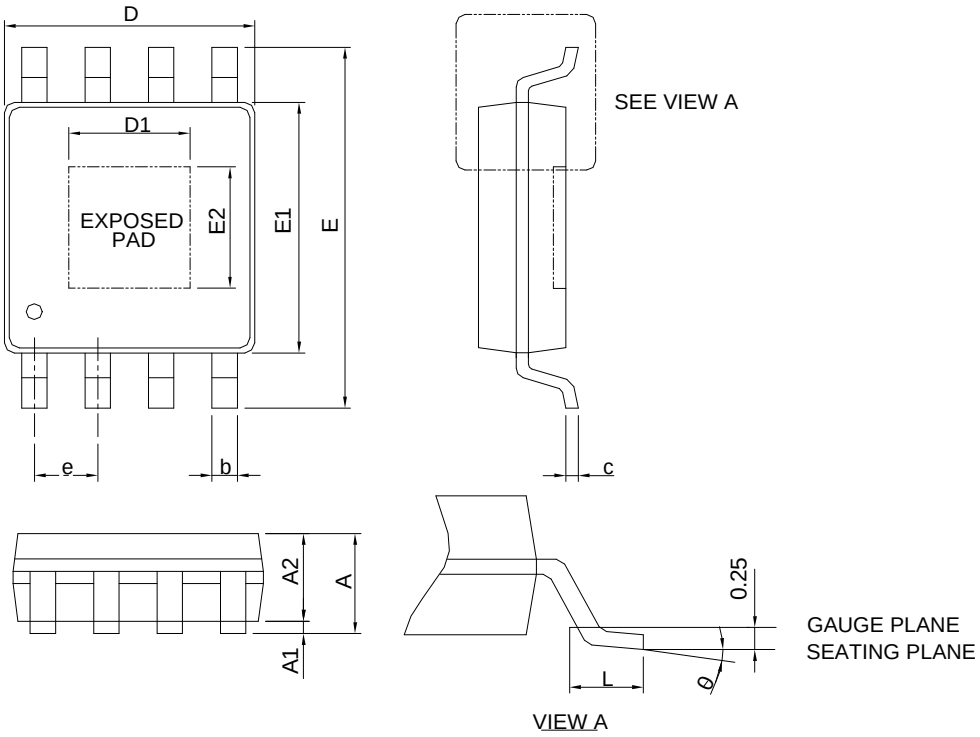
SYMBOL	MSOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.22	0.38	0.009	0.015
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
e	0.65 BSC		0.026 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 AA.
2. Dimension " D " does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension " E1 " does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 5 mil per side.

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Package Information

MSOP-8P



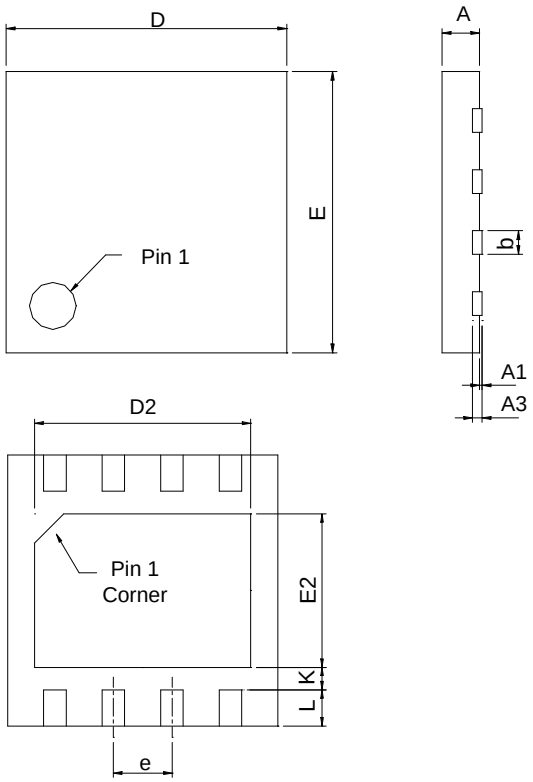
SYMBOL	MSOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.22	0.38	0.009	0.015
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
D1	1.50	2.50	0.059	0.098
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
E2	1.50	2.50	0.059	0.098
e	0.65 BSC		0.026 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 AA-T
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not flash or protrusions.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 6 mil per side.

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Package Information

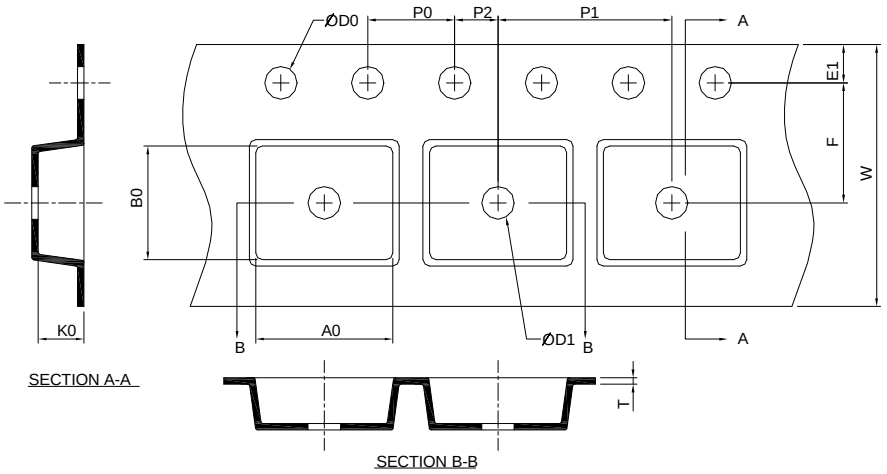
TDFN3x3-8

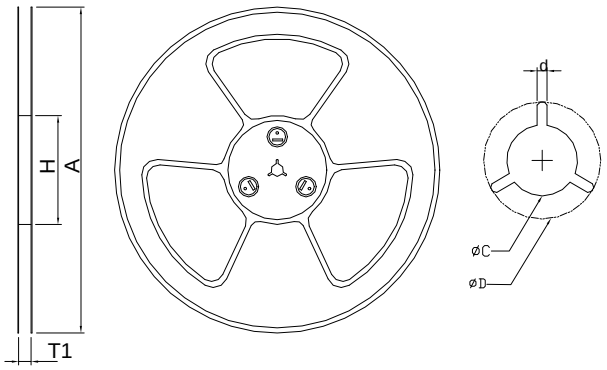


SYMBOL	TDFN3*3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	2.90	3.10	0.114	0.122
D2	1.90	2.40	0.075	0.094
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.65 BSC		0.026 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

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Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
MSOP-8(P)	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	3.30±0.20	1.40±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN3x3-8	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

(mm)

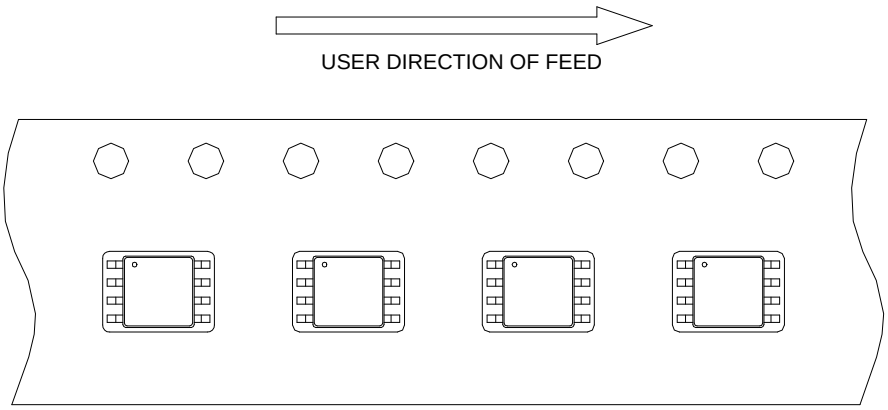
Devices Per Unit

Package Type	Unit	Quantity
MOSP-8(P)	Tape & Reel	3000
TDFN3x3-8	Tape & Reel	3000

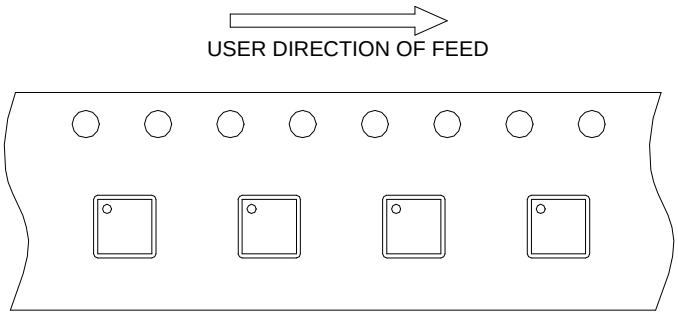
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Taping Dircetion Information

MSOP-8(P)

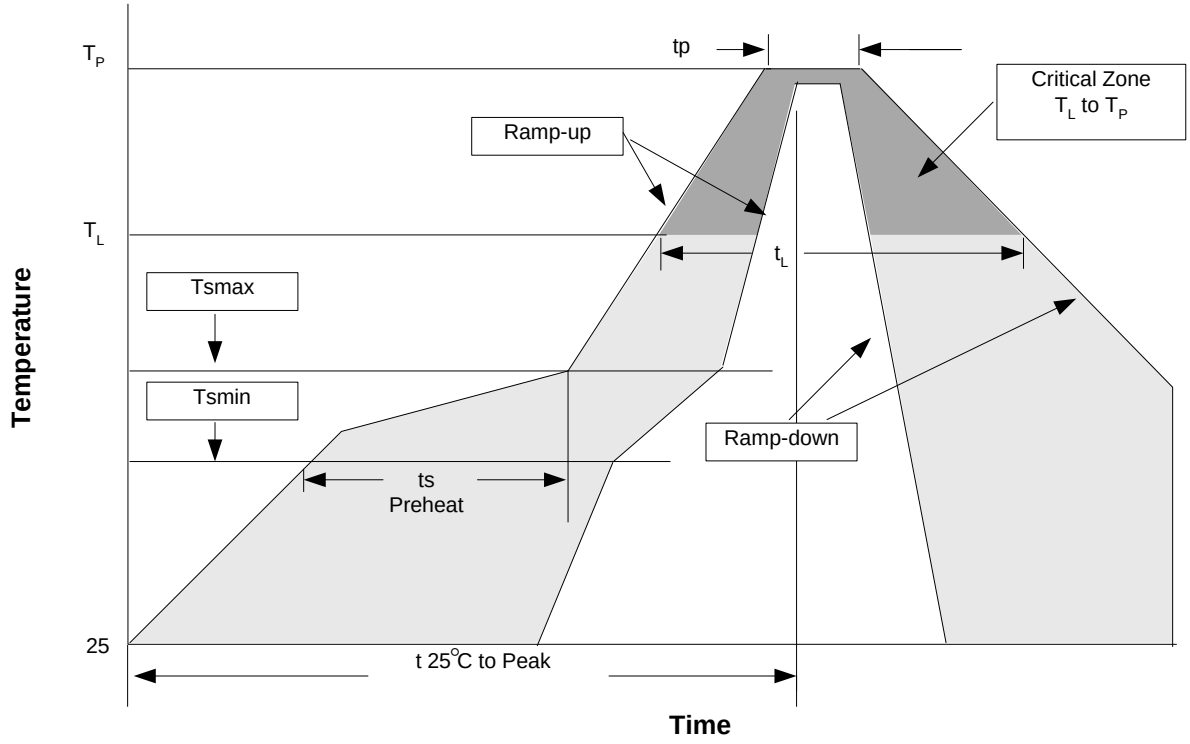


TDFN3x3-8



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Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

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Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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