



UTRS3085

Preliminary

CMOS IC

FAIL-SAFE, 2.5MBPS, RS-485 / RS-422 TRANSCEIVERS WITH $\pm 12\text{KV}$ ESD-PROTECTED

DESCRIPTION

The UTC **UTRS3085** high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. The device features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be logic high if all transmitters on a terminated bus are disabled (high impedance). The UTC **UTRS3085** offer higher driver output slew-rate limits, allowing transmission up to 2.5Mbps.

The transceiver typically draws 375 μA of supply current when unloaded or when fully loaded with the drivers disabled.

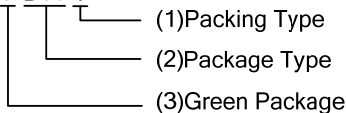
A device has a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

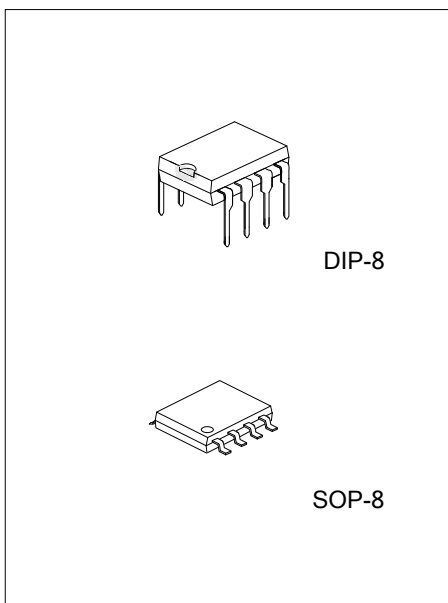
FEATURES

- * True fail-safe receiver while maintaining EIA/TIA-485 compatibility.
- * Enhanced slew-rate limiting facilitates Error-Free data transmission.
- * 5.0V single power supply.
- * 1 μA low-current shutdown mode.
- * Allow up to 256 transceivers on the Bus.
- * HBM $\pm 12\text{kV}$ ESD protection for Transmitter Output
- * Driver short circuit current limit.
- * Thermal shutdown for overload protection.

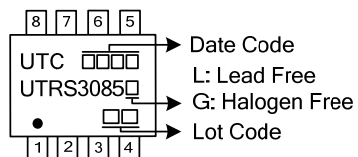
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UTRS3085L-D08-T	UTRS3085G-D08-T	DIP-8	Tube
UTRS3085L-S08-R	UTRS3085G-S08-R	SOP-8	Tape Reel

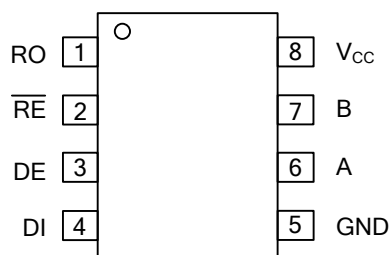
<p>UTRS3085G-D08-T</p> 	<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



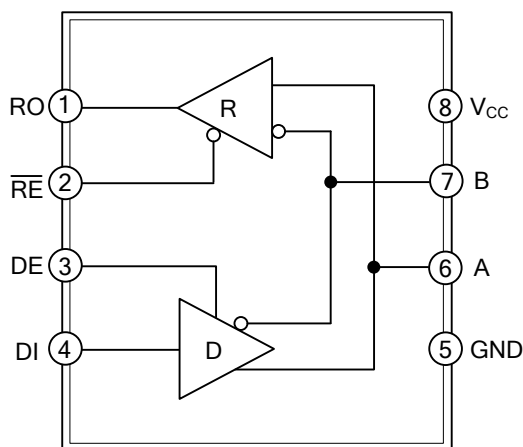
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	RO	Receiver output.
2	RE	Receiver output enable. Drive RE low to enable RO; RO is high impedance when RE is high. Drive RE high and DE low to enter low-power shutdown mode.
3	DE	Driver output enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive RE high and DE low to enter low-power shutdown mode.
4	DI	Driver input. With DE high, a low on DI forces non-inverting output low and inverting output high. Similarly, a high on DI forces non-inverting output high and inverting output low.
5	GND	Ground
6	A	Non-inverting receiver input and non-inverting driver output
7	B	Inverting receiver input and inverting driver output
8	VCC	Positive supply, $4.75V \leq V_{CC} \leq 5.25V$

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V _{CC}	+7.0	V
Control Input Voltage ($\overline{RE}$, DE)			-0.3 ~ (V _{CC} +0.3)	V
Driver Input Voltage		DI	-0.3 ~ (V _{CC} +0.3)	V
Receiver Input Voltage (A, B)			±12.5	V
Receiver Output Voltage (RO)			-0.3 ~ (V _{CC} +0.3)	V
Continuous Power Dissipation (Derate 5.88mW/°C above +70°C)	DIP-8	P _D	550	mW
	SOP-8		471	mW
Operating Temperature Ranges		T _{OPR}	-40 ~ +85	°C
Storage Temperature Range		T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are only stress ratings and it is not implied for functional device operation.
Absolute maximum ratings are the values beyond which the device will be damaged permanently.

■ DC ELECTRICAL CHARACTERISTICS

($V_{CC}=+5.0V \pm 5\%$, $T_A=T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC}=+5.0V$ and $T_A=+25^\circ C$) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
Differential Driver Output (No Load)	V _{OD1}	Fig.1				5.0	V
Differential Driver Output	V _{OD2}	Fig.1, R=50Ω (RS-422)		1.8			V
		Fig.1, R=27Ω (RS-485)		1.4			V
Change in Magnitude of Differential Output Voltage (Note 2)	ΔV _{OD}	Fig.1, R=50Ω or R=27Ω				0.2	V
Driver Common-Mode Output Voltage	V _{OC}	Fig.1, R=50Ω or R=27Ω				3.0	V
Change In Magnitude of Common-Mode Voltage (Note 2)	ΔV _{OC}	Fig.1, R=50Ω or R=27Ω				0.2	V
Input High Voltage	V _{IH1}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V _{IL1}	DE, DI, $\overline{RE}$				0.8	V
DI Input Hysteresis	V _{HYS}				100		mV
Input Current	I _{IN1}	DE, DI, $\overline{RE}$				±2.0	μA
Input Current (A and B)	I _{IN2}	DE=GND, V _{CC} =GND or 5.25V	V _{IN} =12V			125	μA
			V _{IN} =-7V			-75	μA
Driver Short-Circuit Output Current (Note 4)	V _{OD1}	-7V≤V _{OUT} ≤V _{CC}		-250			mA
		0V≤V _{OUT} ≤12V				250	mA
		0V≤V _{OUT} ≤V _{CC}		±25			mA
RECEIVER							
Receiver Differential Threshold Voltage	V _{TH}	V _{CM} =+2.5V		-200		-20	mV
Receiver Input Hysteresis	ΔV _{TH}				25		mV
Receiver Output High Voltage	V _{OH}	I _O =-4mA, V _{ID} =-20mV		V _{CC} -1.5			V
Receiver Output Low Voltage	V _{OL}	I _O =4mA, V _{ID} =-200mV				0.4	V
Three-State Output Current at Receiver	I _{OZR}	0.4V≤V _O ≤2.4V				±1.0	μA
Receiver Input Resistance	R _{IN}	-7V≤V _{CM} ≤+12V		96			kΩ
Receiver Output Short-Circuit Current	I _{OSR}	0V≤V _{RO} ≤V _{CC}		±7		±95	mA

DC ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
Supply Current	I_{CC}	No Load, $\overline{RE} = \overline{DI} = V_{CC}$ or GND	$\overline{DE} = V_{CC}$	430	900	μA
			$\overline{DE} = \text{GND}$	375	600	μA
Supply Current in Shutdown Mode	I_{SHDN}	$\overline{DE} = \text{GND}, V_{\overline{RE}} = V_{CC}$		1.0	10	μA

Notes: 1. All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.

2. ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.

3. Maximum current level applies to peak current just prior to foldback-current limiting; minimum current level applies during current limiting.

■ SWITCHING CHARACTERISTICS

($V_{CC} = +5.0V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Input to Output	t_{DPLH}	Fig.3 and 5, $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$		100		ns
	t_{DPHL}			100		ns
Driver Output Skew $t_{DPLH} - t_{DPHL}$	t_{DSKEW}	Fig.3 and 5, $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$		5	200	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Fig.3 and 5, $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$		200		ns
Maximum Data Rate	f_{MAX}		2.5			Mbps
Driver Enable to Output High	t_{DZH}	Fig.4 and 6, $C_L = 100pF$, S2 Closed			3500	ns
Driver Enable to Output Low	t_{DZL}	Fig.4 and 6, $C_L = 100pF$, S1 Closed			3500	ns
Driver Disable Time from Low	t_{DLZ}	Fig.4 and 6, $C_L = 15pF$, S1 Closed			200	ns
Driver Disable Time from High	t_{DHZ}	Fig.4 and 6, $C_L = 15pF$, S2 Closed			200	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Fig.7 and 9, $ V_{ID} \geq 2.0V$; Rise and Fall Time of $V_{ID} \leq 15ns$		200		ns
$t_{RPLH} - t_{RPHL}$ Differential Receiver Skew	t_{RSKD}	Fig.7 and 9, $ V_{ID} \geq 2.0V$; Rise and Fall Time of $V_{ID} \leq 15ns$		50		ns
Receiver Enable to Output Low	t_{RZL}	Fig.2 and 8, $C_L = 100pF$, S1 Closed		50		ns
Receiver Enable to Output High	t_{RZH}	Fig.2 and 8, $C_L = 100pF$, S2 Closed		50		ns
Receiver Disable Time from Low	t_{RLZ}	Fig.2 and 8, $C_L = 100pF$, S1 Closed		50		ns
Receiver Disable Time from High	t_{RHZ}	Fig.2 and 8, $C_L = 100pF$, S2 Closed		50		ns
Time to Shutdown	t_{SHDN}	Note 1		200		ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Fig.4 and 6, $C_L = 15pF$, S2 Closed			4500	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Fig.4 and 6, $C_L = 15pF$, S1 Closed			4500	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Fig.2 and 8, $C_L = 100pF$, S2 Closed			3500	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Fig.2 and 8, $C_L = 100pF$, S1 Closed			3500	ns

Note: The device is put into shutdown by bringing $\overline{RE}$ high and $\overline{DE}$ low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

■ FUNCTION TABLE

TRANSMITTING

INPUTS			OUTPUTS	
$\overline{\text{RE}}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

RECEIVING

INPUTS			OUTPUT
$\overline{\text{RE}}$	DE	A-B	RO
0	X	$\geq -0.02\text{V}$	1
0	X	$\leq -0.2\text{V}$	0
0	X	Open/Shorted	1
1	1	X	High-Z
1	0	X	Shutdown

X = Don't care

Shutdown mode, driver and receiver outputs high impedance

■ TEST CIRCUIT

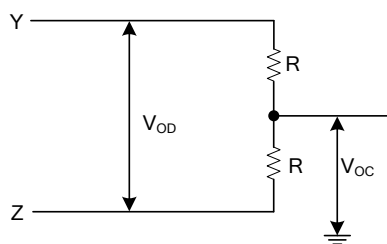


Fig. 1 Driver DC Test Circuit

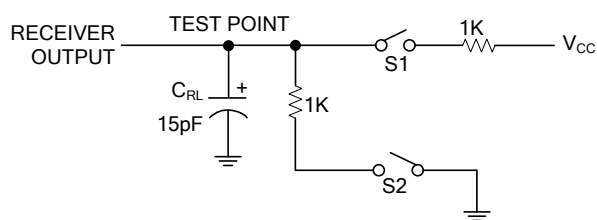


Fig. 2 Receiver Enable/Disable Timing Test Load

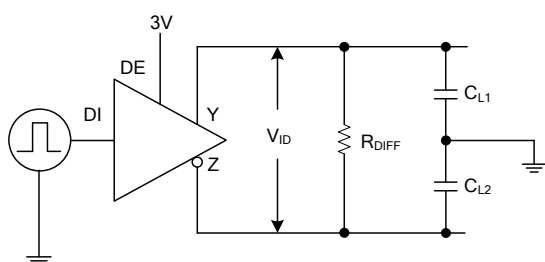


Fig. 3 Driver Timing Test Circuit

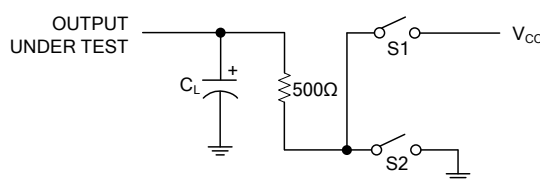


Fig. 4 Driver Enable/Disable Timing Test Load

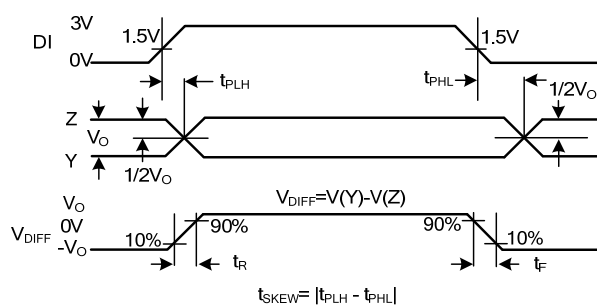


Fig. 5 Driver Propagation Delays

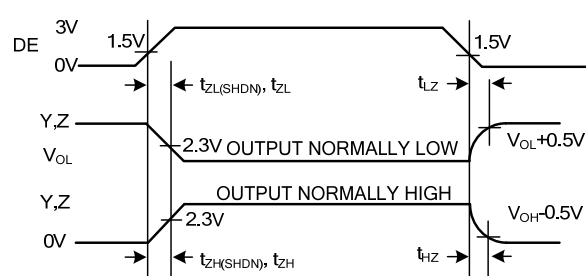


Fig. 6 Driver Enable and Disable Times

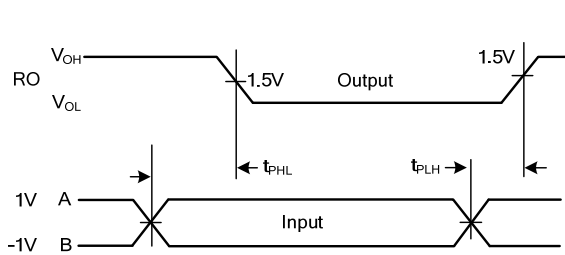


Fig. 7 Receiver Propagation Delays

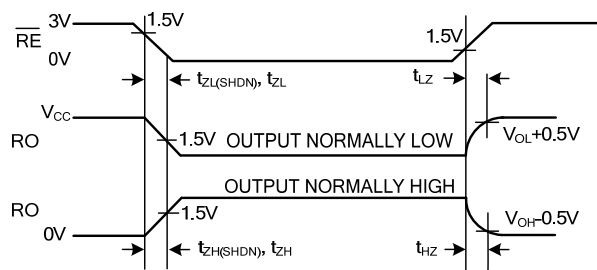


Fig. 8 Receiver Enable and Disable Times

■ TEST CIRCUIT (Cont.)

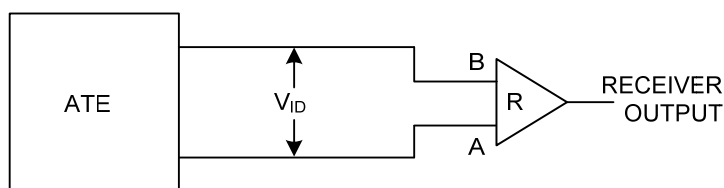
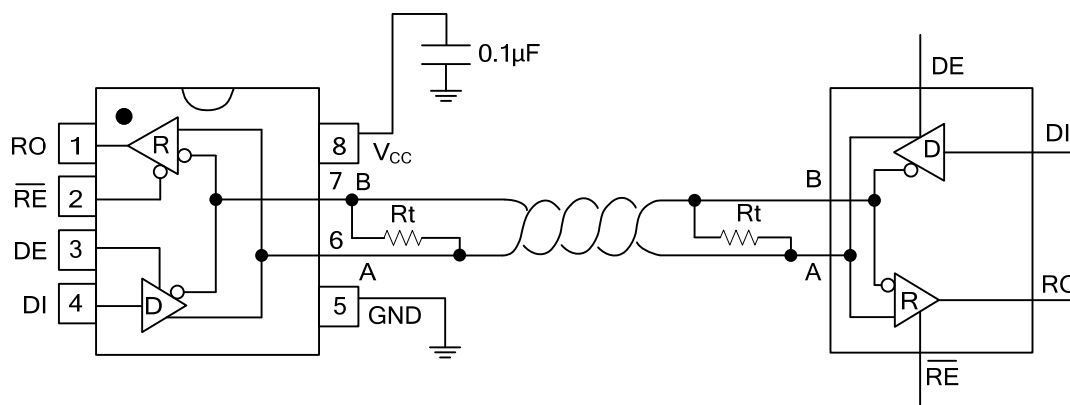


Fig. 9 Receiver Propagation Delay Test Circuit

■ TYPICAL APPLICATION CIRCUIT



Note: Pin labels Y and Z on timing, test, and waveform diagrams refer to pins A and B when DE is high.

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