

## 256K (32K x 8) Static RAM

### Features

- **Temperature Ranges**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive-A: -40°C to 85°C
  - Automotive-E: -40°C to 125°C
- **High speed: 55 ns**
- **Voltage range: 4.5V–5.5V operation**
- **Low active power**
  - 275 mW (max.)
- **Low standby power (LL version)**
  - 82.5 μW (max.)
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in pb-free and non Pb-free 28-lead (600-mil) PDIP, 28-lead (300-mil) narrow SOIC, 28-lead TSOP-I and 28-lead Reverse TSOP-I packages**

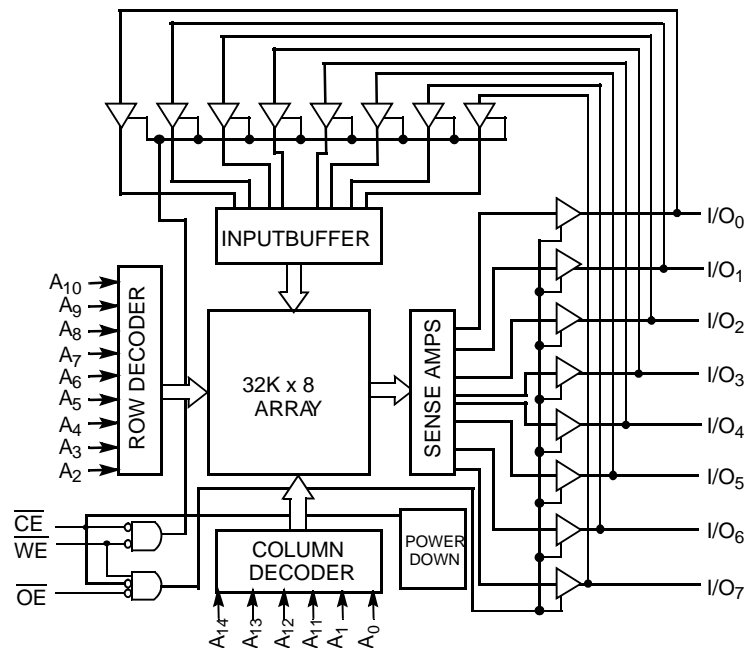
### Functional Description<sup>[1]</sup>

The CY62256N is a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{\text{CE}}$ ) and active LOW output enable ( $\overline{\text{OE}}$ ) and tri-state drivers. This device has an automatic power-down feature, reducing the power consumption by 99.9% when deselected.

An active LOW write enable signal ( $\overline{\text{WE}}$ ) controls the writing/reading operation of the memory. When  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  inputs are both LOW, data on the eight data input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is written into the memory location addressed by the address present on the address pins ( $\text{A}_0$  through  $\text{A}_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  active LOW, while  $\overline{\text{WE}}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{\text{WE}}$ ) is HIGH.

### Logic Block Diagram



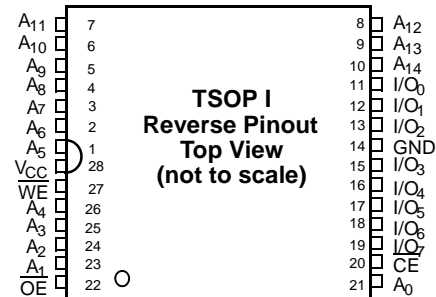
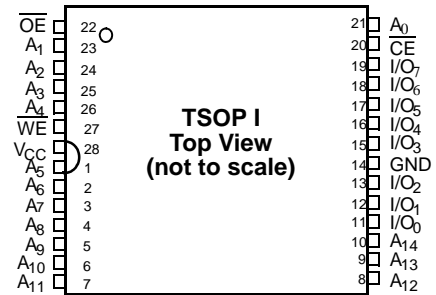
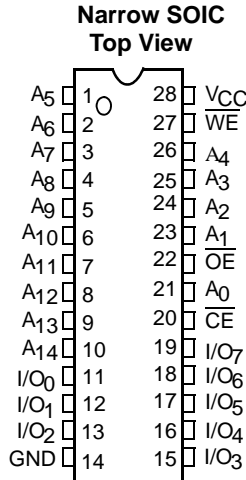
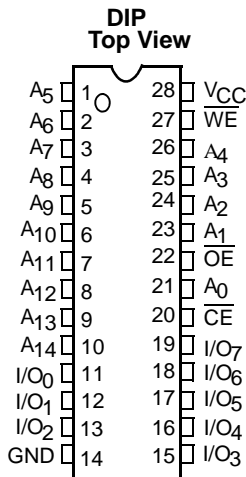
**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product		V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation			
						Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
		Min.	Typ. <sup>[2]</sup>	Max.		Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.
CY62256NL	Com'l / Ind'l	4.5	5.0	5.5	70	25	50	2	50
CY62256NLL	Commercial				70	25	50	0.1	5
CY62256NLL	Industrial				55/70	25	50	0.1	10
CY62256NLL	Automotive-A				55/70	25	50	0.1	10
CY62256NLL	Automotive-E				55	25	50	0.1	15

Pin Configurations



Pin Definitions

Pin Number	Type	Description
1–10, 21, 23–26	Input	<b>A<sub>0</sub>–A<sub>14</sub></b> . Address Inputs
11–13, 15–19,	Input/Output	<b>I/O<sub>0</sub>–I/O<sub>7</sub></b> . Data lines. Used as input or output lines depending on operation
27	Input/Control	<b>WE</b> . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	<b>CE</b> . When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	<b>OE</b> . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
14	Ground	<b>GND</b> . Ground for the device
28	Power Supply	<b>V<sub>CC</sub></b> . Power supply for the device

Note:

2. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T<sub>A</sub> = 25°C, V<sub>CC</sub>). Parameters are guaranteed by design and characterization, and not 100% tested.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

### Operating Range

Range	Ambient Temperature ( $T_A$ ) <sup>[7]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Automotive-A	-40°C to +85°C	5V ± 10%
Automotive-E	-40°C to +125°C	5V ± 10%

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	2.4			2.4			V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$			0.4			0.4	V
$V_{IH}$	Input HIGH Voltage		2.2		$V_{CC} + 0.5V$	2.2		$V_{CC} + 0.5V$	V
$V_{IL}$	Input LOW Voltage		-0.5		0.8	-0.5		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-0.5		+0.5	-0.5		+0.5	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-0.5		+0.5	-0.5		+0.5	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	L-Comm'l/Ind'l				25	50	mA
			LL-Comm'l				25	50	mA
			LL - Ind'l	25	50		25	50	mA
			LL - Auto-A	25	50		25	50	mA
			LL - Auto-E	25	50				mA
$I_{SB1}$	Automatic CE Power-down Current—TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	L				0.4	0.6	mA
			LL-Comm'l				0.3	0.5	mA
			LL - Ind'l	0.3	0.5		0.3	0.5	mA
			LL - Auto-A	0.3	0.5		0.3	0.5	mA
			LL - Auto-E	0.3	0.5				mA
$I_{SB2}$	Automatic CE Power-down Current—CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$	L				2	50	μA
			LL-Comm'l				0.1	5	μA
			LL - Ind'l	0.1	10		0.1	10	μA
			LL - Auto-A	0.1	10		0.1	10	μA
			LL - Auto-E	0.1	15				μA

### Capacitance<sup>[8]</sup>

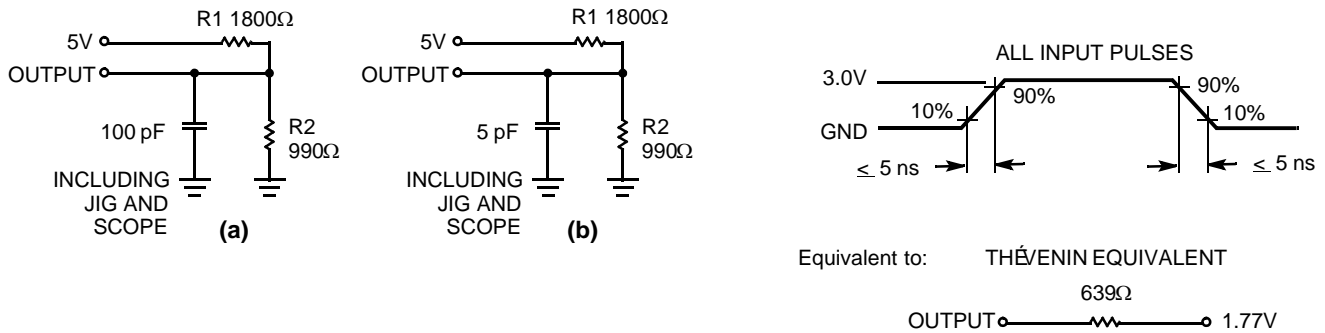
Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 5.0V$	6	pF
$C_{OUT}$	Output Capacitance		8	pF

**Notes:**

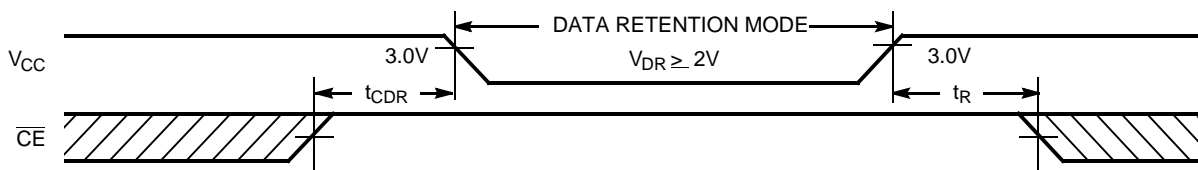
- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "Instant-On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

**Thermal Resistance<sup>[5]</sup>**

Parameter	Description	Test Conditions	DIP	SOIC	TSOP	RTSOP	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	75.61	76.56	93.89	93.89	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		43.12	36.07	24.64	24.64	°C/W

**AC Test Loads and Waveforms**

**Data Retention Characteristics**

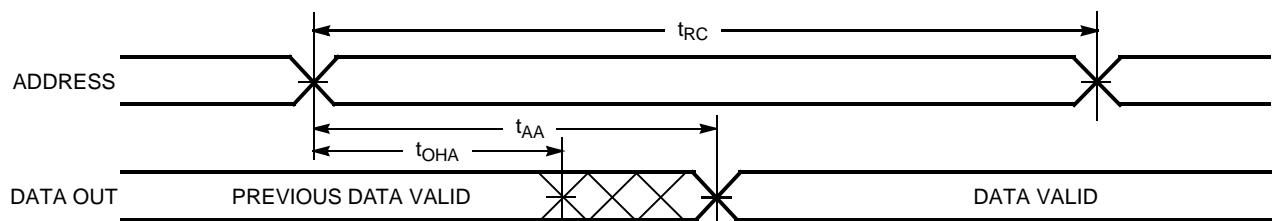
Parameter	Description	Conditions <sup>[6]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0			V
$I_{CCDR}$	Data Retention Current	L	$V_{CC} = 2.0V, CE \geq V_{CC} - 0.3V, V_{IN} \geq V_{CC} - 0.3V, \text{ or } V_{IN} \leq 0.3V$	2	50	$\mu A$
		LL-Comm'l		0.1	5	$\mu A$
		LL - Ind'l/Auto-A		0.1	10	$\mu A$
		LL - Auto-E		0.1	10	$\mu A$
$t_{CDR}^{[8]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform**

**Note:**

6. No input may exceed  $V_{CC} + 0.5V$ .

**Switching Characteristics** Over the Operating Range<sup>[7]</sup>

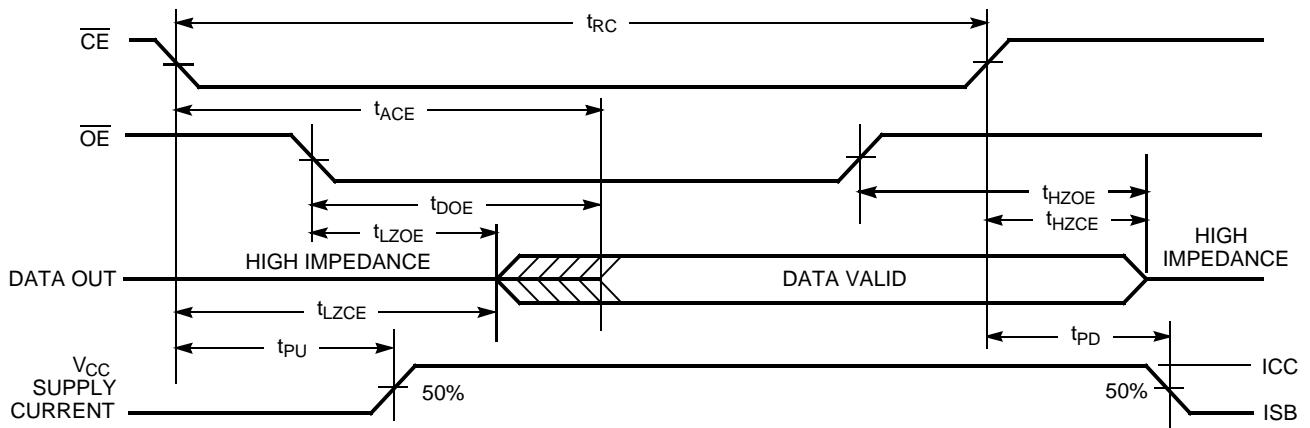
Parameter	Description	CY62256N-55		CY62256N-70		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	5		5		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[8]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[8, 9]</sup>		20		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[8]</sup>	5		5		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[8, 9]</sup>		20		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-down		55		70	ns
<b>Write Cycle<sup>[10, 11]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	45		60		ns
$t_{AW}$	Address Set-up to Write End	45		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		50		ns
$t_{SD}$	Data Set-up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[8, 9]</sup>		20		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[8]</sup>	5		5		ns

**Switching Waveforms**
**Read Cycle No. 1<sup>[12, 13]</sup>**

**Notes:**

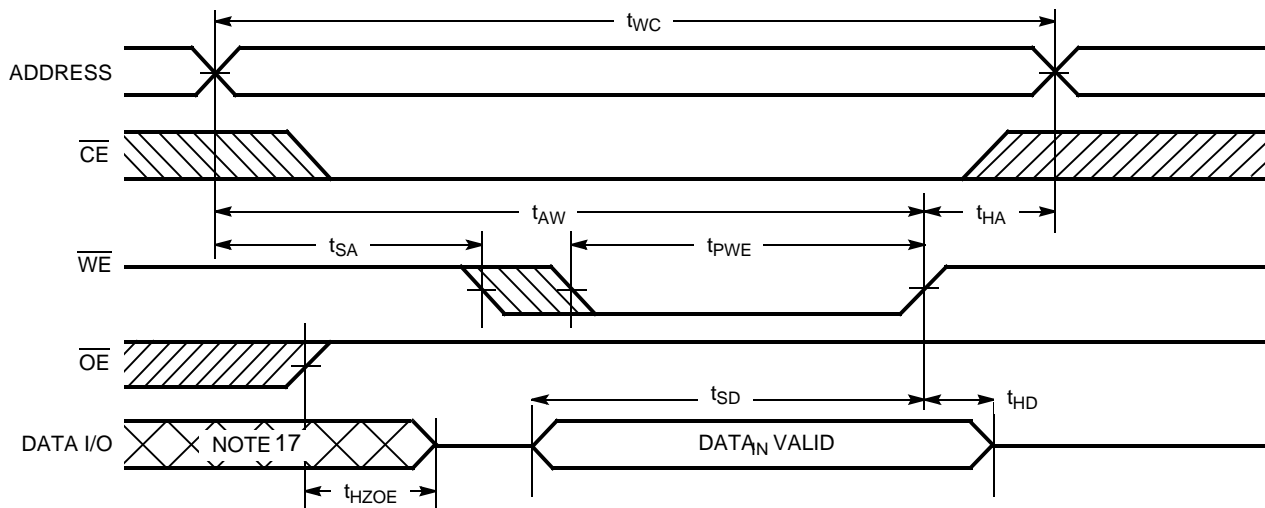
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 100-pF load capacitance.
8. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
9.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
10. The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
13.  $\overline{WE}$  is HIGH for Read cycle.

Switching Waveforms (continued)

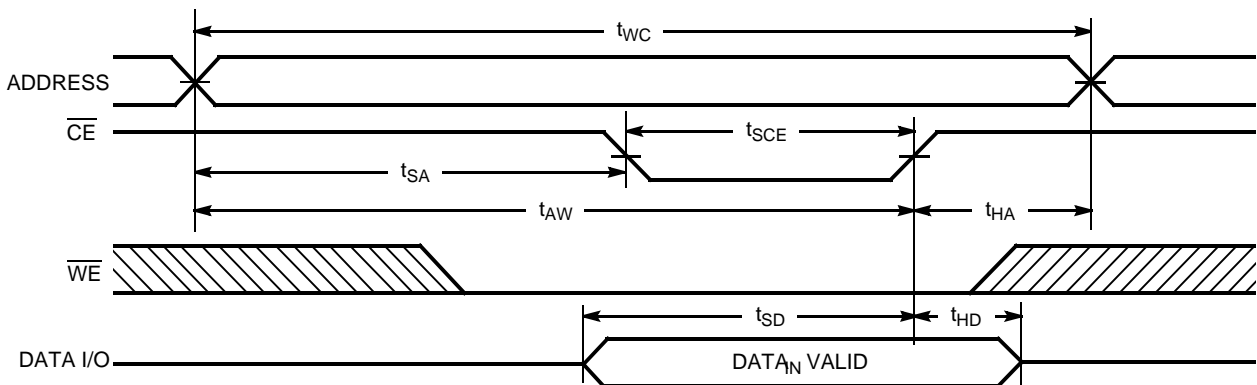
Read Cycle No. 2<sup>[13, 14]</sup>



Write Cycle No. 1 (WE Controlled)<sup>[10, 15, 16]</sup>



Write Cycle No. 2 (CE Controlled)<sup>[10, 15, 16]</sup>

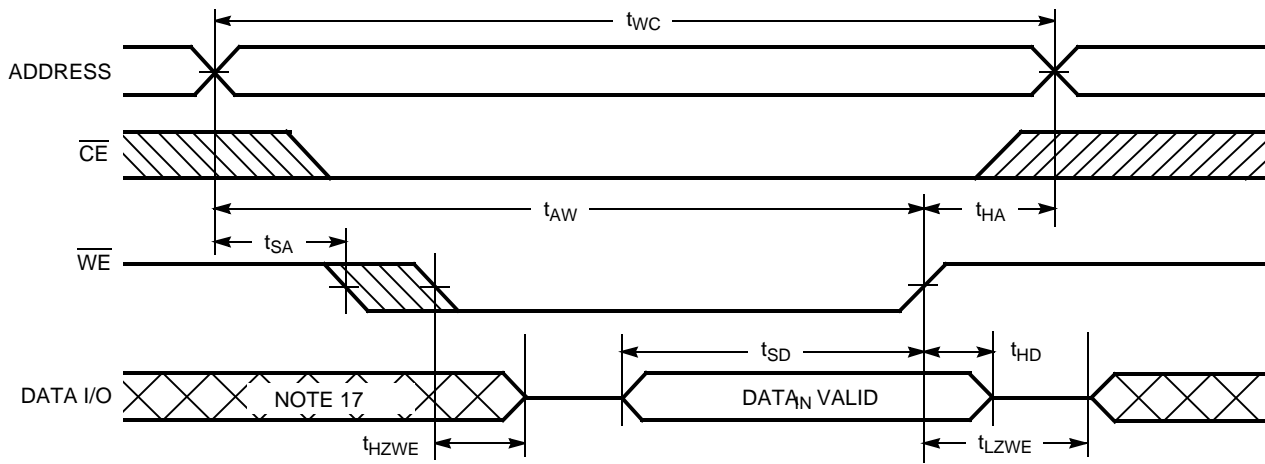


Notes:

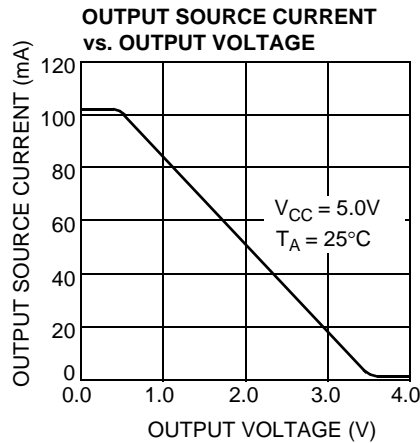
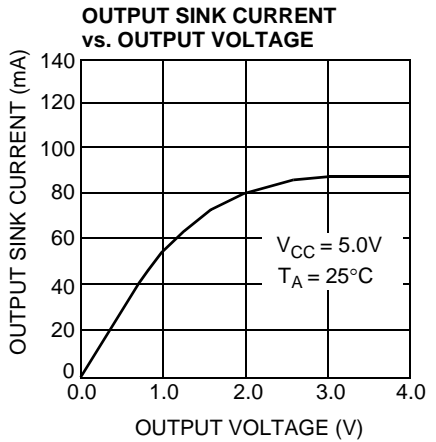
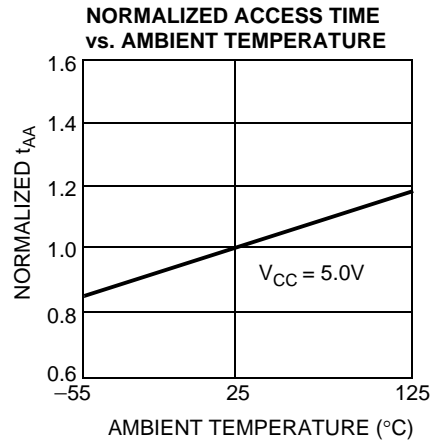
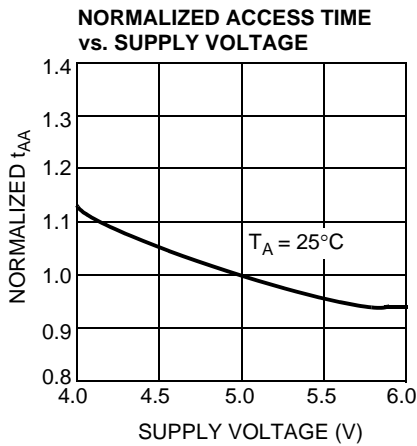
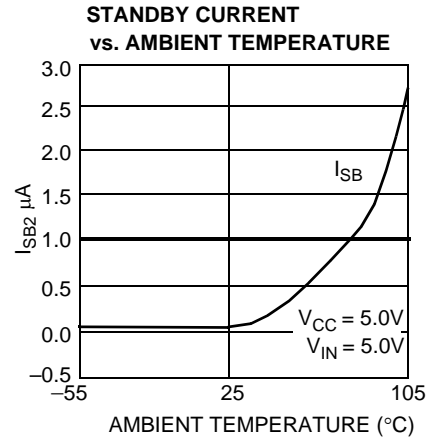
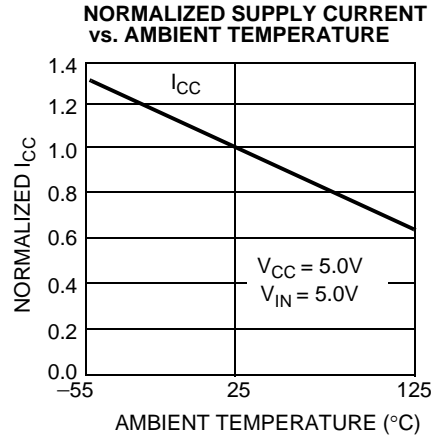
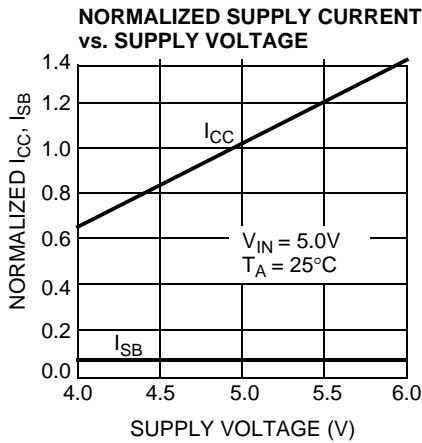
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 15. Data I/O is high impedance if  $OE = V_{IH}$ .
- 16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
- 17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[11, 16]</sup>

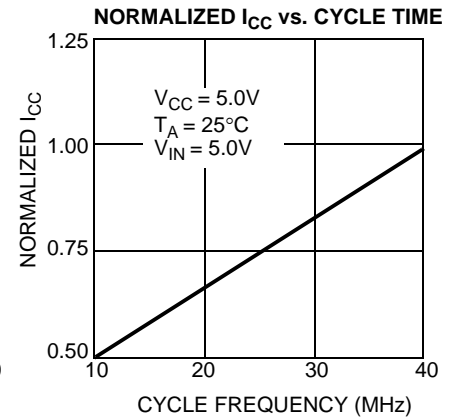
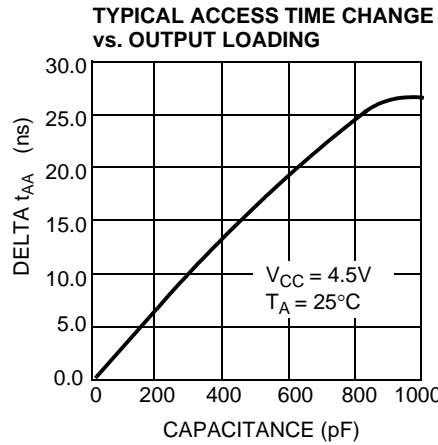
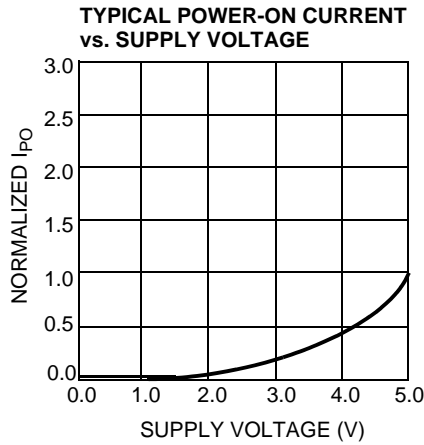


Typical DC and AC Characteristics





**Typical DC and AC Characteristics** (continued)



**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data Out	Read	Active ( $I_{\text{CC}}$ )
L	L	X	Data In	Write	Active ( $I_{\text{CC}}$ )
L	H	H	High-Z	Output Disabled	Active ( $I_{\text{CC}}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62256NLL-55SNI	51-85092	28-lead (300-Mil) Narrow SOIC	Industrial
	CY62256NLL-55SNXI		28-lead (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL-55ZI	51-85071	28-lead TSOP I	
	CY62256NLL-55ZXI		28-lead TSOP I (Pb-Free)	
	CY62256NLL-55ZXA	51-85071	28-lead TSOP I (Pb-Free)	Automotive-A
	CY62256NLL-55SNXE	51-85092	28-lead (300-Mil) Narrow SOIC (Pb-Free)	Automotive-E
	CY62256NLL-55ZXE	51-85071	28-lead TSOP I (Pb-Free)	
	CY62256NLL-55ZRXE	51-85074	28-lead Reverse TSOP I (Pb-Free)	
70	CY62256NL-70PC	51-85017	28-lead (600-Mil) Molded DIP	Commercial
	CY62256NL-70PXC		28-lead (600-Mil) Molded DIP (Pb-Free)	
	CY62256NLL-70PC		28-lead (600-Mil) Molded DIP	
	CY62256NLL-70PXC		28-lead (600-Mil) Molded DIP (Pb-Free)	
	CY62256NL-70SNC	51-85092	28-lead (300-Mil) Narrow SOIC	
	CY62256NL-70SNXC		28-lead (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL-70SNC		28-lead (300-Mil) Narrow SOIC	
	CY62256NLL-70SNXC		28-lead (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL-70ZC	51-85071	28-lead TSOP I	
	CY62256NLL-70ZXC		28-lead TSOP I (Pb-Free)	
	CY62256NL-70SNI	51-85092	28-lead (300-Mil) Narrow SOIC	Industrial
	CY62256NL-70SNXI		28-lead (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL-70SNI		28-lead (300-Mil) Narrow SOIC	
	CY62256NLL-70SNXI		28-lead (300-Mil) Narrow SOIC (Pb-Free)	
	CY62256NLL-70ZI	51-85071	28-lead TSOP I	
	CY62256NLL-70ZXI		28-lead TSOP I (Pb-Free)	
	CY62256NLL-70ZRI	51-85074	28-lead Reverse TSOP I	
	CY62256NLL-70ZRXI		28-lead Reverse TSOP I (Pb-Free)	
CY62256NLL-70SNXA	51-85092	28-lead (300-Mil) Narrow SOIC (Pb-Free)	Automotive-A	

Please contact your local Cypress sales representative for availability of these parts

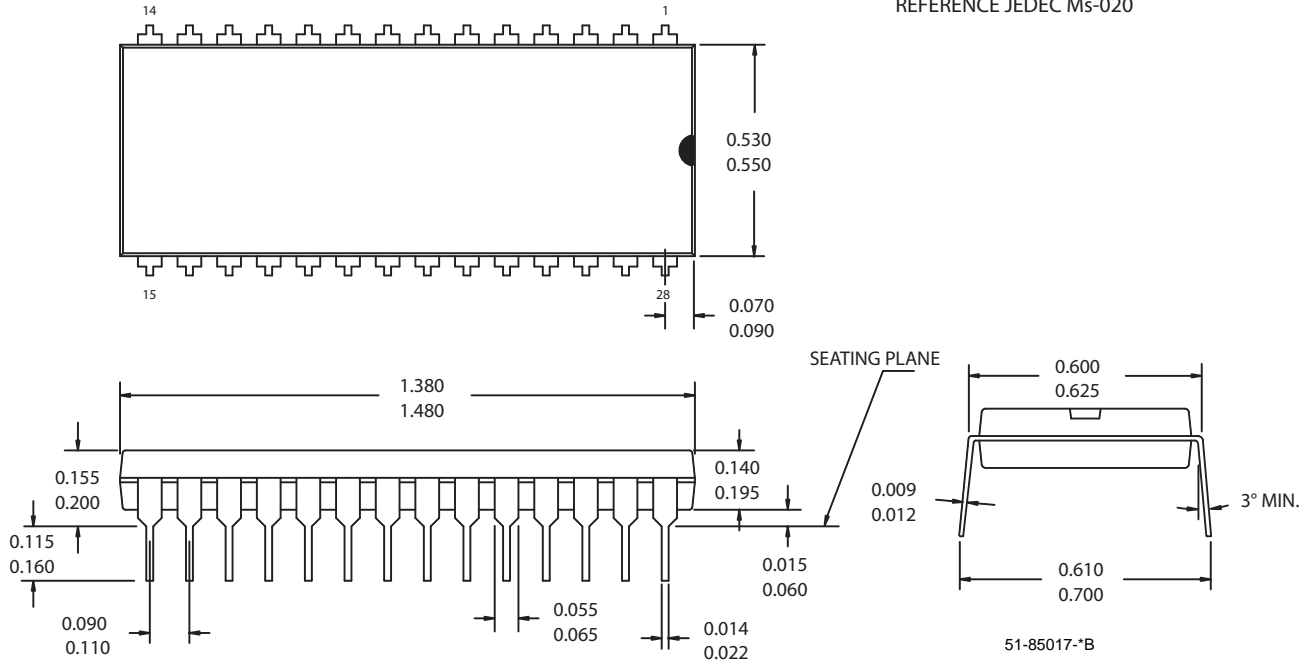
**Package Diagrams**

**28-lead (600-Mil) Molded DIP (51-85017)**

DIMENSIONS IN INCHES

MIN.  
MAX.

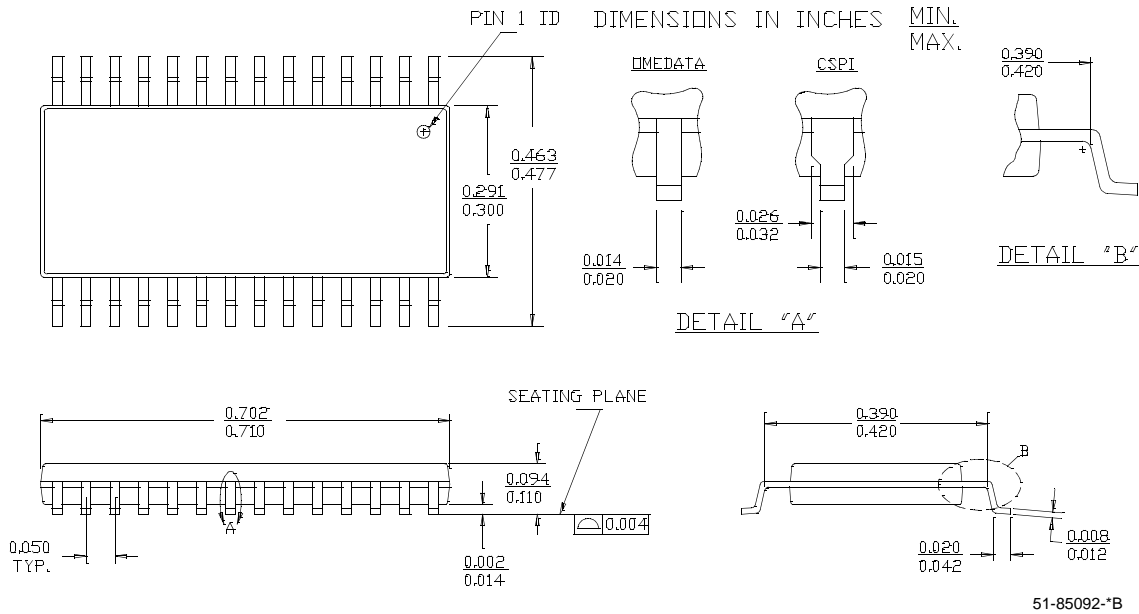
REFERENCE JEDEC Ms-020



**28-lead (300-mil) SNC (Narrow Body) (51-85092)**

DIMENSIONS IN INCHES

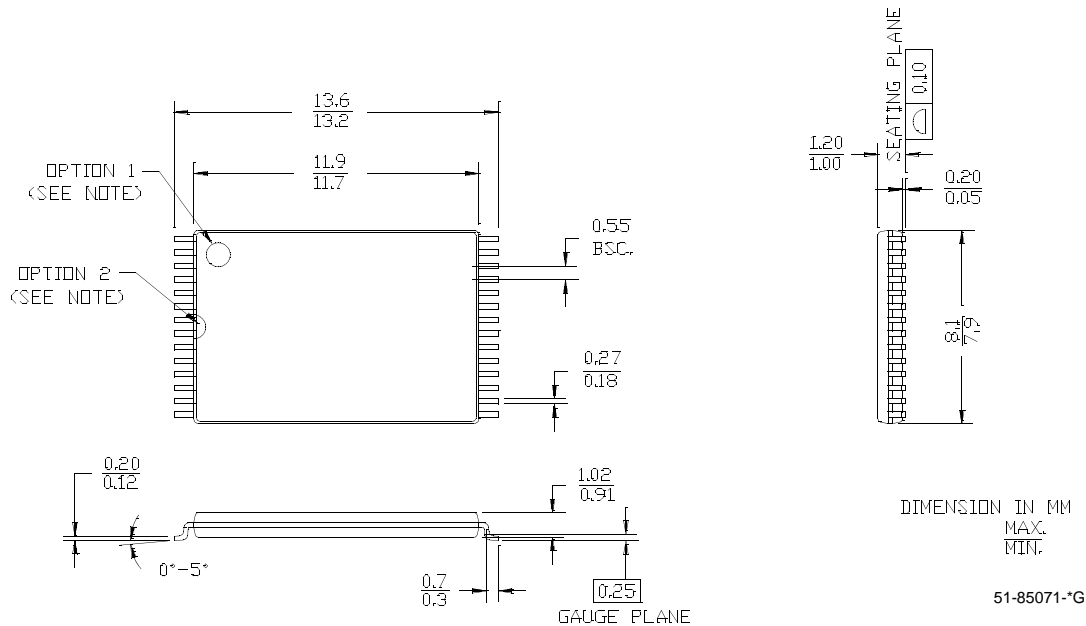
MIN.  
MAX.



**Package Diagrams (continued)**

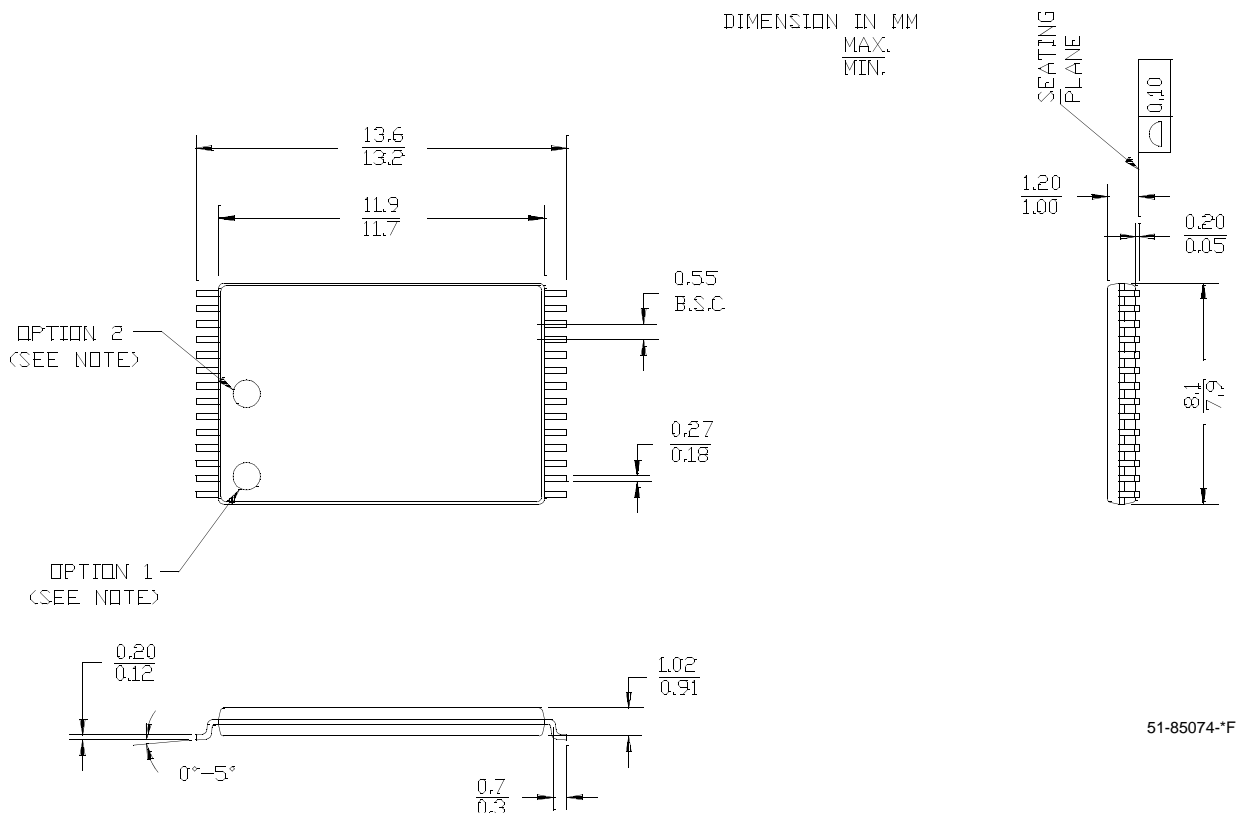
**28-lead TSOP I (8 x 13.4 mm) (51-85071)**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



**28-Lead RTSOP I (8 x 13.4 mm) (51-85074)**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



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**Document History Page**

<b>Document Title: CY62256N 256K (32K x 8) Static RAM</b> <b>Document Number: 001- 06511</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	426504	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table