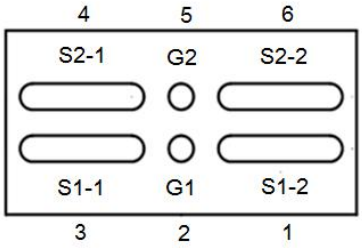
WNMD2185

Dual N-Channel, 12V, 27A Power MOSFET

Http://www.sh-willsemi.com

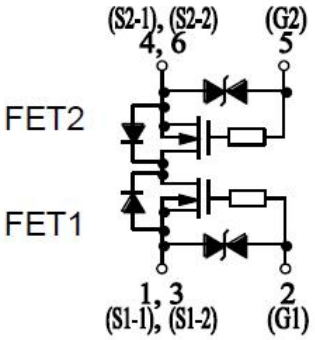
V_{sss} (V)	Typ $R_{ss(on)}$ (mΩ)
12	2.2 @ V_{GS}=4.5V
	2.3 @ V_{GS}=4.0V
	2.4 @ V_{GS}=3.8V
	2.8 @ V_{GS}=3.1V
	3.4 @ V_{GS}=2.5V



CSP-6L

Descriptions

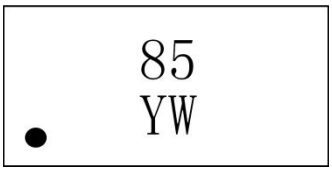
The WNMD2185 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent $R_{SS(ON)}$ with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2185 is available in CSP-6L package. Standard Product WNMD2185 is Pb-free and Halogen-free.



Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Common-drain type
- Small package CSP-6L



85 = Device Code
Y = Year
W = Week(A~z)

Marking

Applications

- Lithium-Ion battery protection circuit

Order information

Device	Package	Shipping
WNMD2185-6/TR	CSP-6L	3000/Reel&Tape

Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Source to Source Voltage	V_{SSS}	V_{GS} = 0 V, I_S = 250uA	12			V
Zero Gate Voltage Drain Current	I_{SSS}	V_{SS} =10 V, V_{GS} = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I_{GSS}	V_{SS} = 0 V, V_{GS} = ±10V TEST CIRCUIT 2			±10	uA
ON CHARACTERISTICS						
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{GS} = V_{SS}, I_S = 250uA TEST CIRCUIT 3	0.45	0.65	1.0	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS} = 4.5V, I_S = 5.0A TEST CIRCUIT 5	1.6	2.2	3.1	mΩ
		V_{GS} = 4.0V, I_S = 5.0A TEST CIRCUIT 5	1.6	2.3	3.2	
		V_{GS} = 3.8V, I_S = 5.0A TEST CIRCUIT 5	1.7	2.4	3.2	
		V_{GS} = 3.1V, I_S = 5.0A TEST CIRCUIT 5	1.8	2.8	4.0	
		V_{GS} = 2.5V, I_S = 5.0A TEST CIRCUIT 5	1.9	3.4	6.1	
BODY DIODE CHARACTERISTICS						
Body Diode Forward Voltage	$V_{F(S-S)}$	V_{GS} = 0 V, I_F = 5.0A TEST CIRCUIT 6		0.7	1.3	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = 4.5 V, V_{SS}=8V, I_S=5A,R_G=6Ω TEST CIRCUIT 8		1.9		us
Rise Time	tr			5.8		
Turn-Off Delay Time	td(OFF)			5.7		
Fall Time	tf			16.5		
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1kHz, V_{SS} = 10 V TEST CIRCUIT 7		4520		pF
Output Capacitance	C_{OSS}			1100		
Reverse Transfer Capacitance	C_{RSS}			1058		
Total Gate Charge	$Q_{G(TOT)}$	V_{G1S1} = 4.5 V, V_{SS} = 10V, I_S =6A TEST CIRCUIT 9		70		nC
Threshold Gate Charge	$Q_{G(TH)}$			5		
Gate-to-Source Charge	Q_{GS}			14		
Gate-to-Drain Charge	Q_{GD}			19		

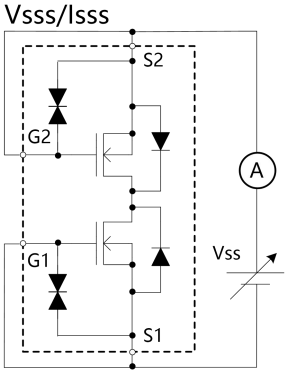
Absolute Maximum ratings

Parameter	Symbol	Rating	Unit
Source to Source Voltage (V_{GS} = 0 V)	V_{SSS}	12	V
Gate to Source Voltage (V_{SS} = 0 V)	V_{GSS}	±10	
Source Current (pulse)Note.1	$I_{S(pulse)}$	100	A
Source Current (DC)	I_S	27	A
Channel Temperature	T_{ch}	-55 to150	°C
Storage Temperature Range	T_{stg}	-55 to150	°C

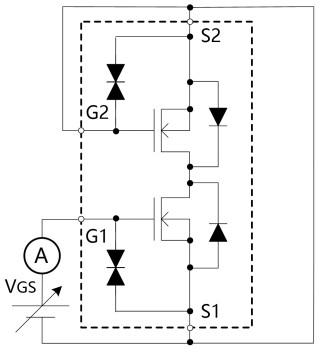
Note.1 PW≤10μs, duty cycle≤1%;

Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

Test Circuit 1
Vsss/Isss

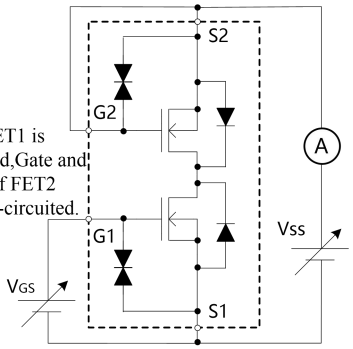


Test Circuit 2
I_{GSS}



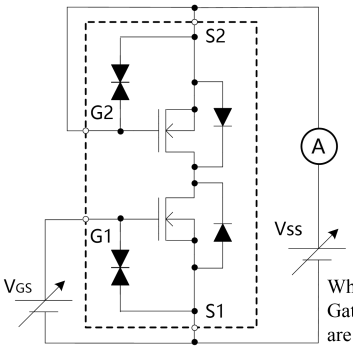
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
V_{GS}(th)



When FET1 is measured,Gate and Source of FET2 are short-circuited.

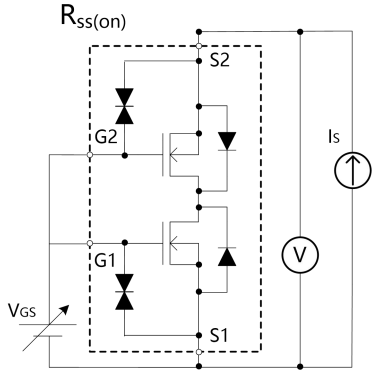
Test Circuit 4
g_{FS}



When FET1 is measured, Gate and Source of FET2 are short-circuited.

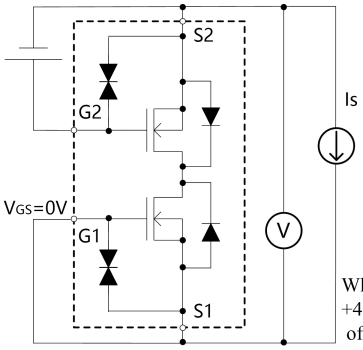
Test Circuit 5

$R_{ss(on)}$



Test Circuit 6

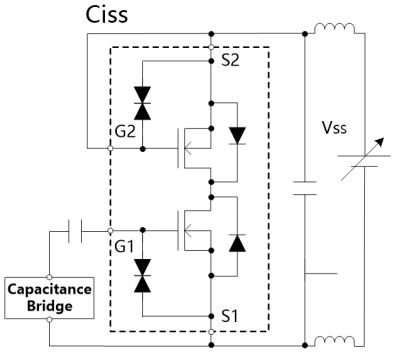
$V_{F(S-S)}$



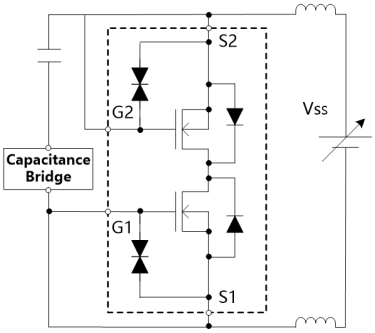
When FET1 is measured, +4.5V is added to V_{GS} of FET2.

Test Circuit 7

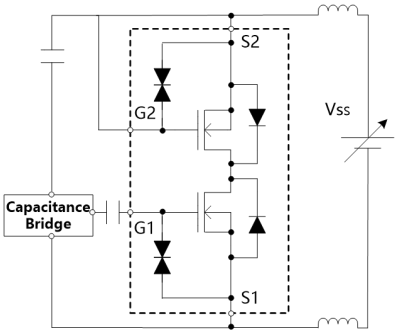
Ciss



Coss

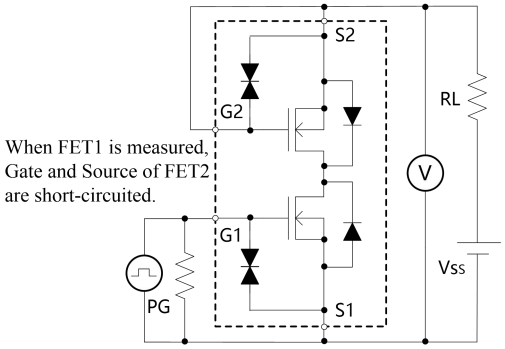


Crss



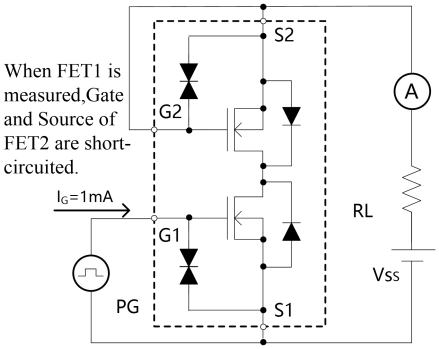
Test Circuit 8

$t_{d(on)}, t_r, t_{d(off)}, t_f$

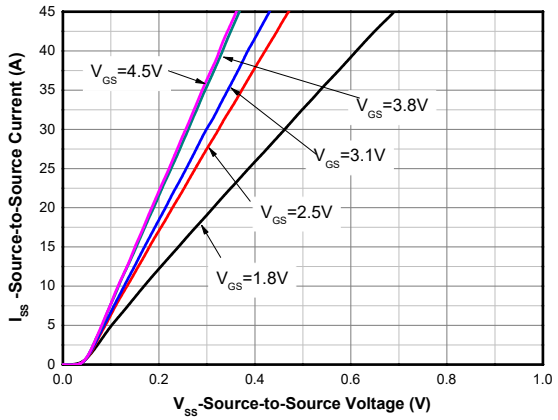


Test Circuit 9

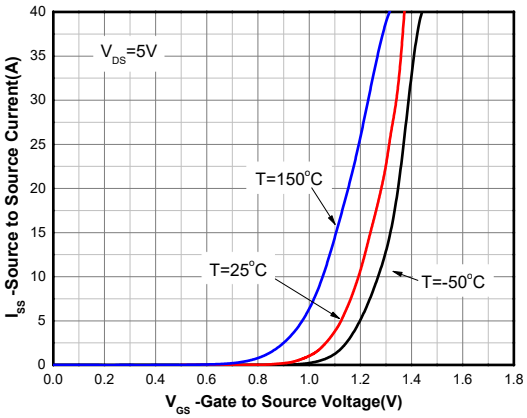
Qg



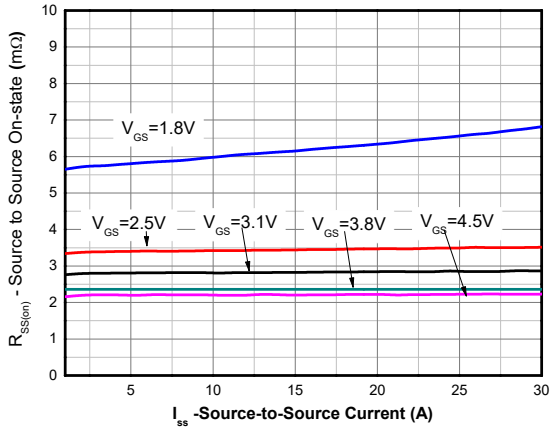
Typical Characteristics (Ta=25°C, unless otherwise noted)



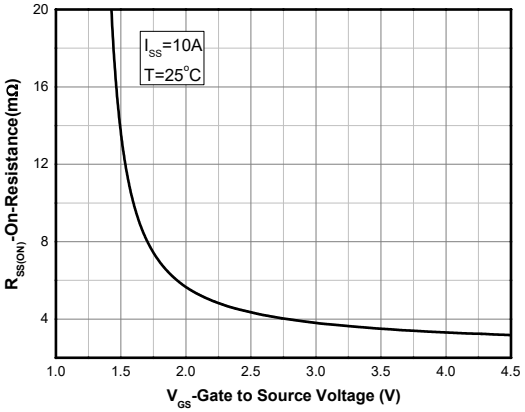
Output characteristics



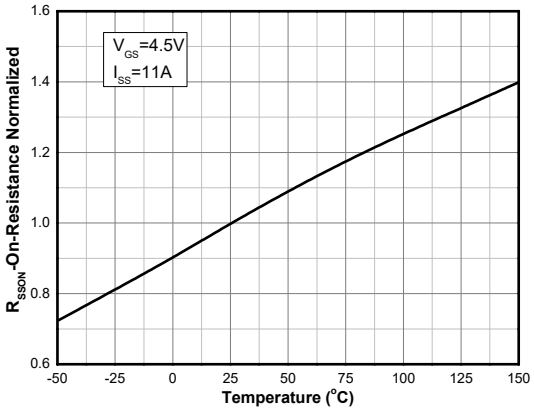
Transfer Characteristics



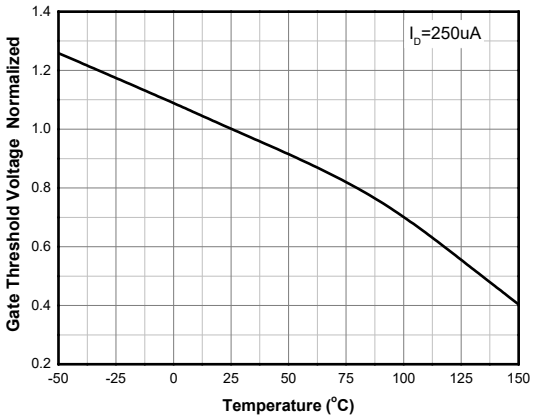
On-Resistance vs.Source Current



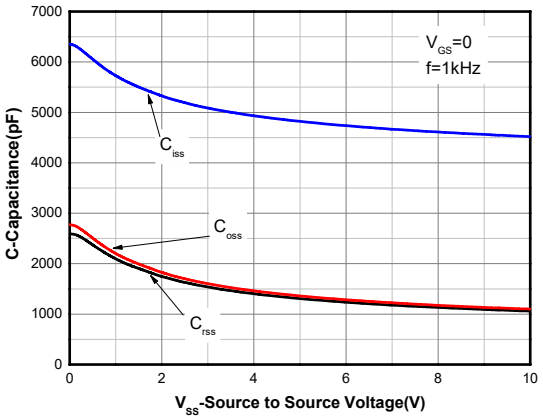
On-Resistance vs.Gate-to-Source Voltage



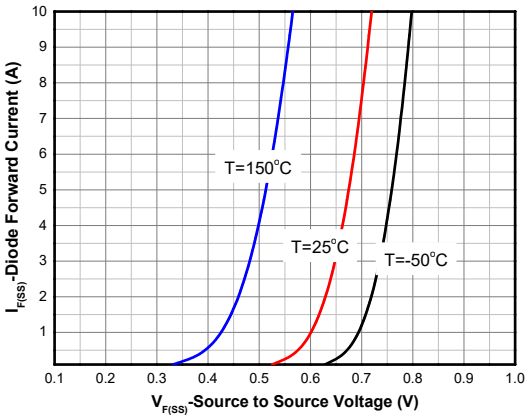
On-Resistance vs.Junction Temperature



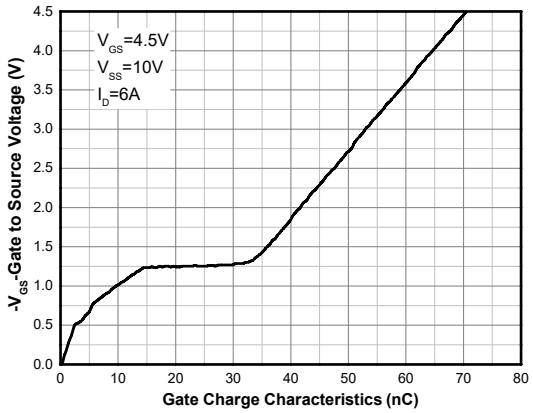
Threshold Voltage vs. Temperature



Capacitance



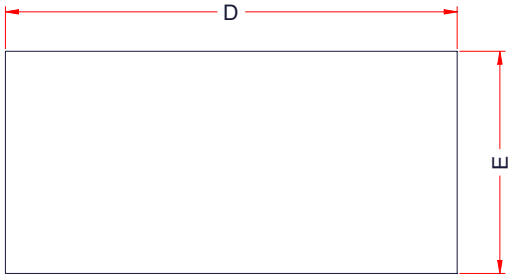
Body Diode Forward Voltage



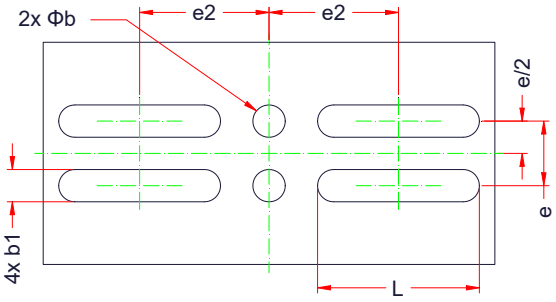
Gate Charge Characteristics

PACKAGE OUTLINE DIMENSIONS

CSP-6L



TOP VIEW

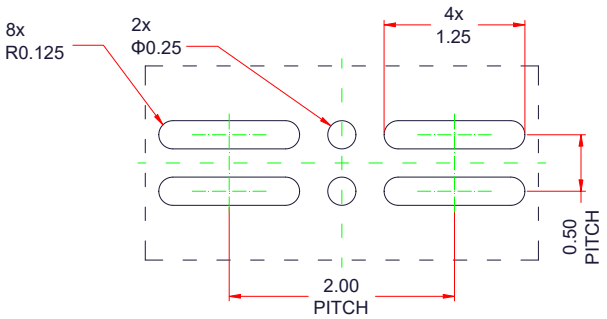


BOTTOM VIEW

SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.09	0.11	0.13
D	3.49	3.54	3.59
E	1.72	1.77	1.82
b		0.25 Typ	
b1		0.25 Typ	
e		0.50 Typ	
e2		1.00 Typ	
L		1.25 Typ	

Recommend PCB Layout (Unit: mm)

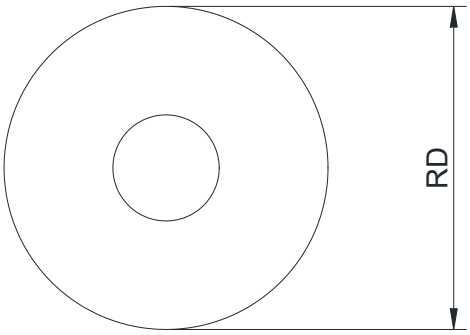


Notes:

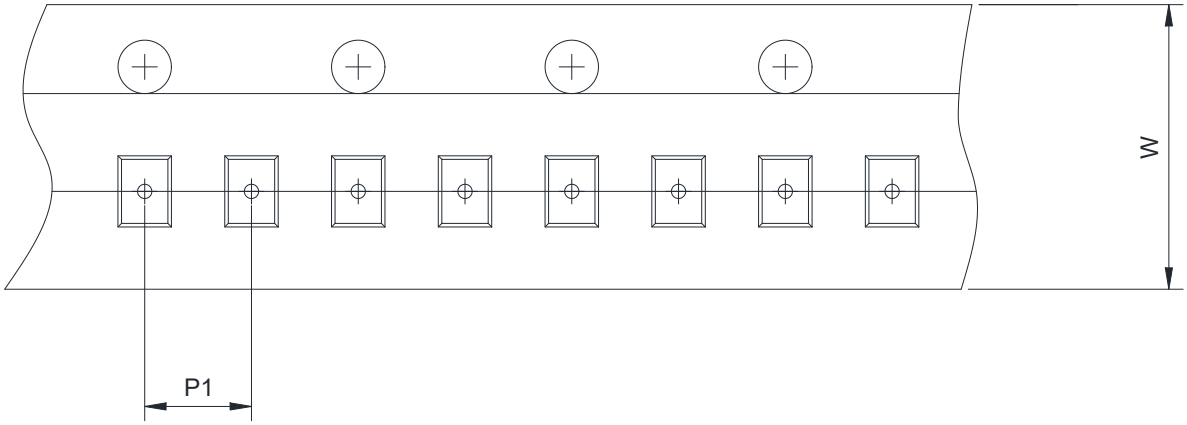
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

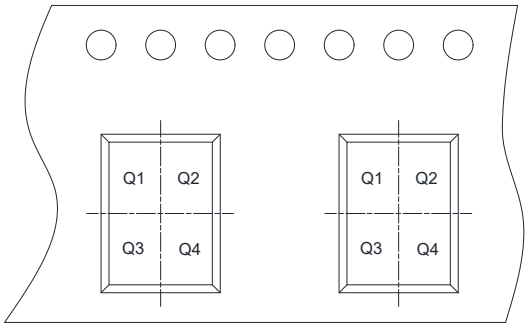
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☐ Q2	☐ Q3	☑ Q4