

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The NP52N06SLG is N-channel MOS FET designed for high current switching applications.

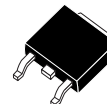
ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP52N06SLG-E1-AY	Pure Sn (Tin)	Tape	TO-252 (MP-3ZK)
NP52N06SLG-E2-AY		2500 p/reel	typ. 0.27 g

FEATURES

- Channel temperature 175 degree rating
- Low on-state resistance
 $R_{DS(on)} = 17.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 26 \text{ A)}$
- Logic level drive type

(TO-252)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 52	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 104	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	56	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current ^{Note2}	I_{AR}	20	A
Repetitive Avalanche Energy ^{Note2}	E_{AR}	40	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. $T_{ch} \leq 150^\circ\text{C}$, $V_{DD} = 30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	2.68	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

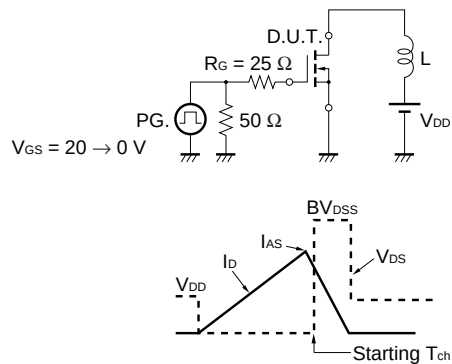
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

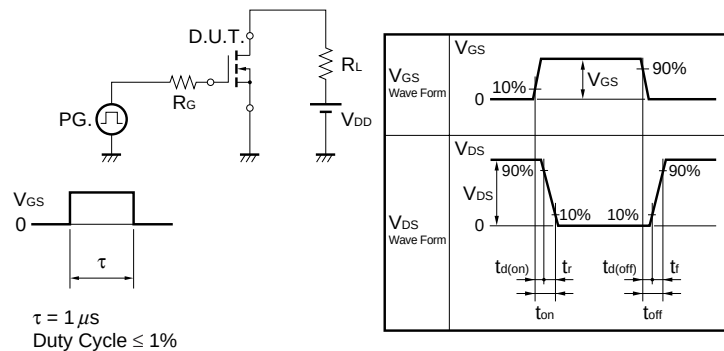
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 26 A	8	14.5		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 26 A		13.6	17.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 26 A		17.5	25	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		2100		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		150		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V		12		ns
Rise Time	t _r	I _D = 26 A		10		ns
Turn-off Delay Time	t _{d(off)}	V _{GS} = 10 V		47		ns
Fall Time	t _f	R _G = 0 Ω		9		ns
Total Gate Charge	Q _G	V _{DD} = 48 V		39		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		7.5		nC
Gate to Drain Charge	Q _{GD}	I _D = 52 A		12		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 52 A, V _{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 52 A, V _{GS} = 0 V		36		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		39		nC

Note Pulsed

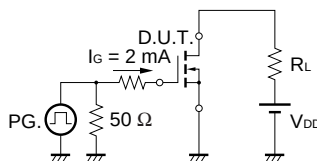
TEST CIRCUIT 1 AVALANCHE CAPABILITY



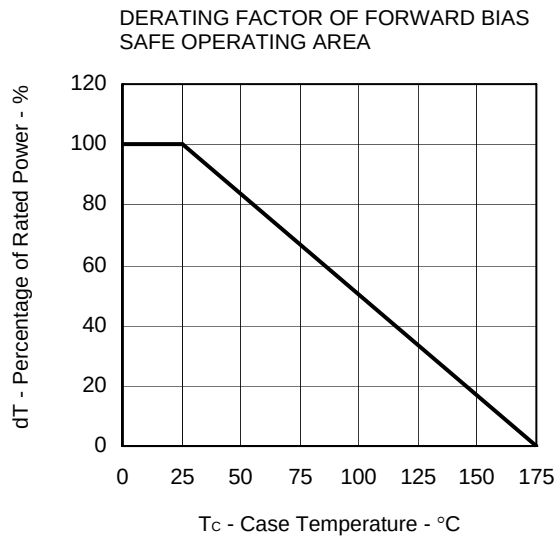
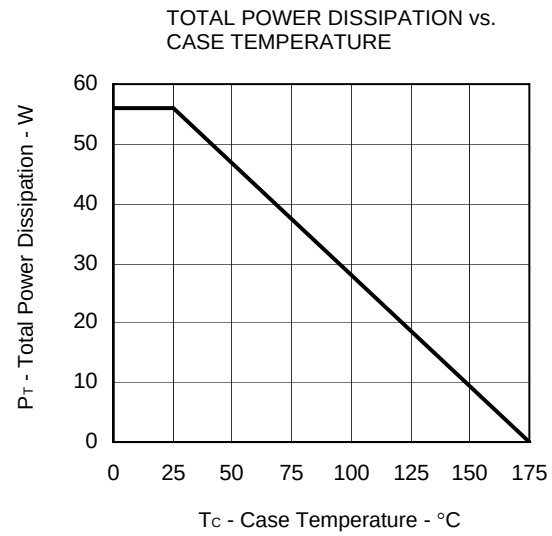
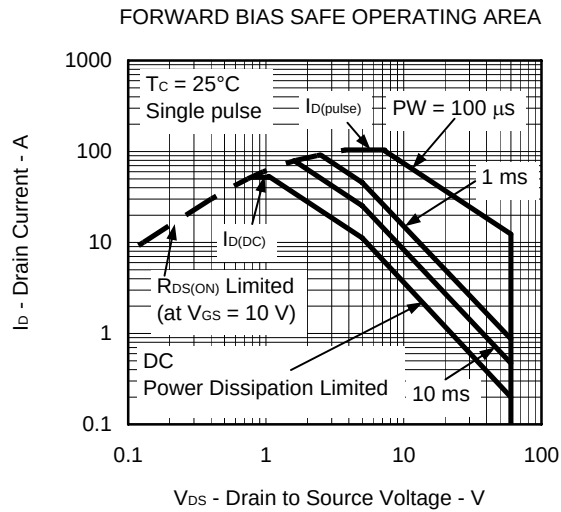
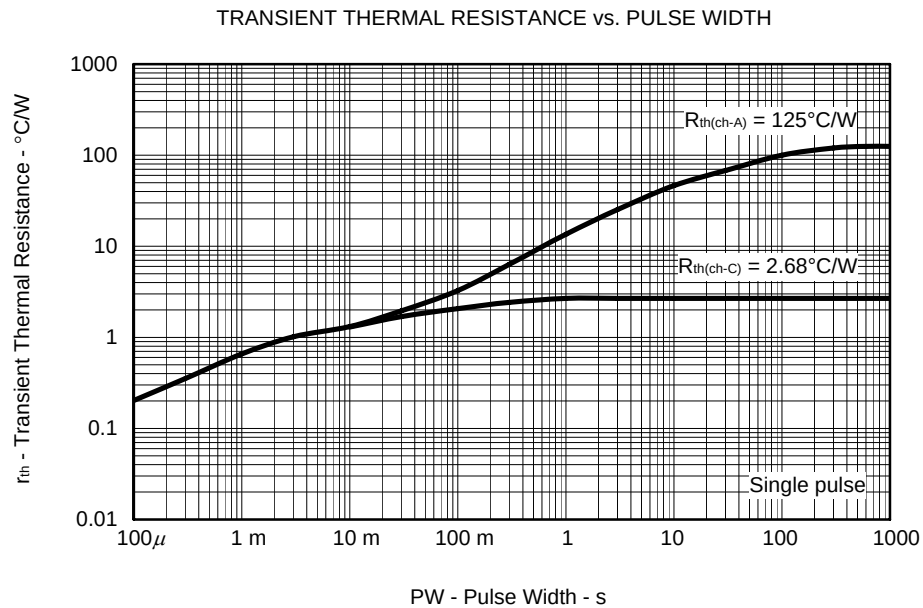
TEST CIRCUIT 2 SWITCHING TIME



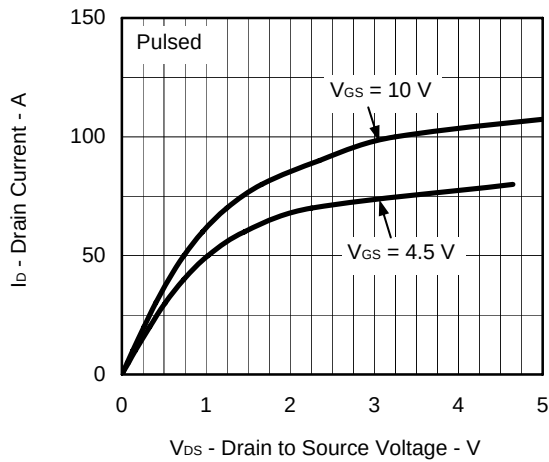
TEST CIRCUIT 3 GATE CHARGE



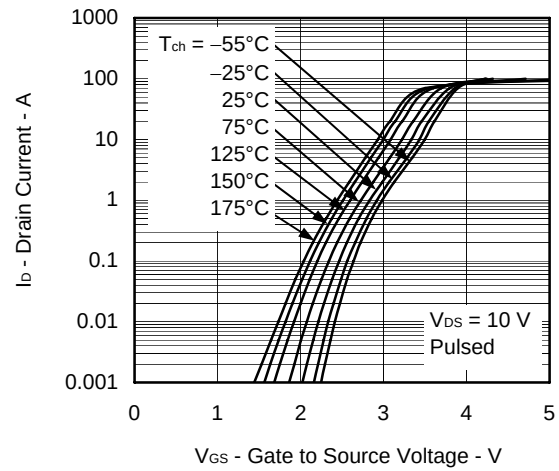
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



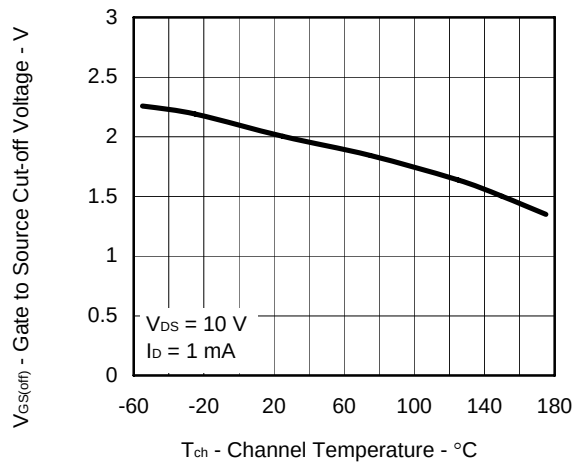
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



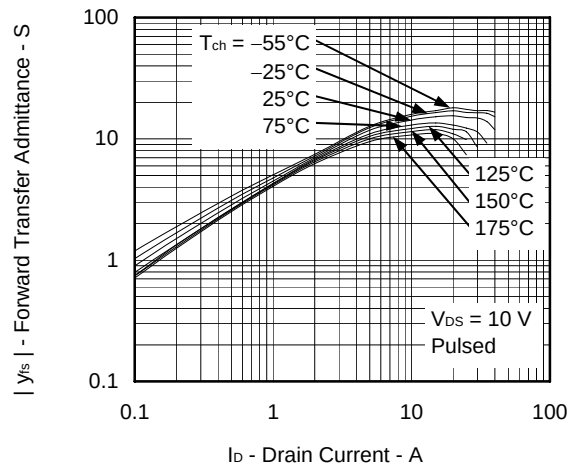
DRAIN CURRENT vs.
GATE TO SOURCE VOLTAGE



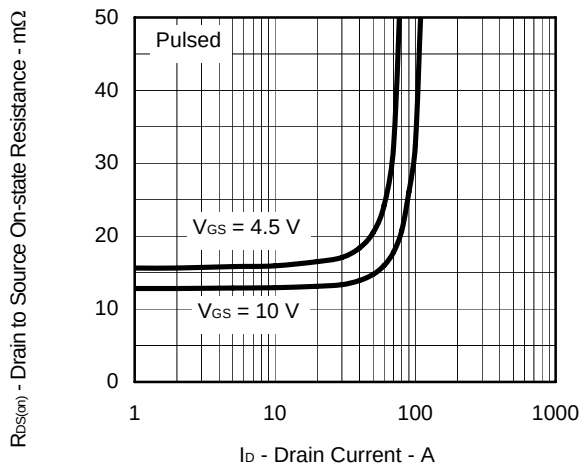
GATE TO SOURCE CUT-OFF VOLTAGE
vs. CHANNEL TEMPERATURE



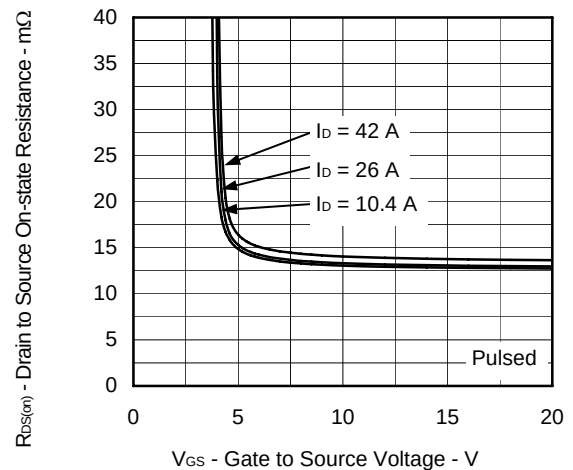
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



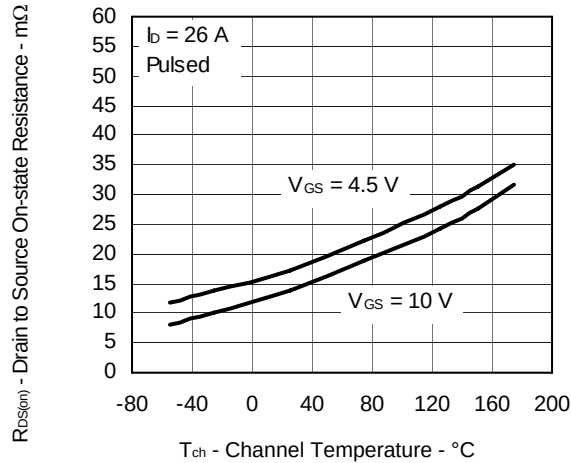
DRAIN TO SOURCE ON-STATE RESISTANCE
vs. DRAIN CURRENT



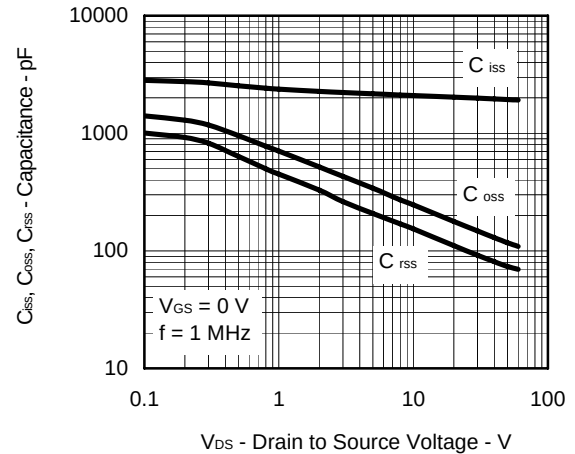
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



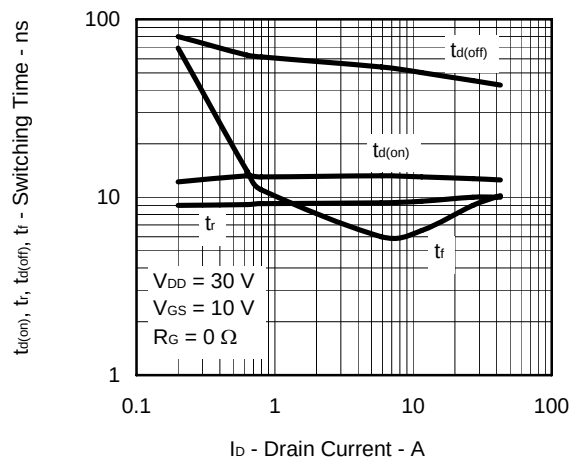
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



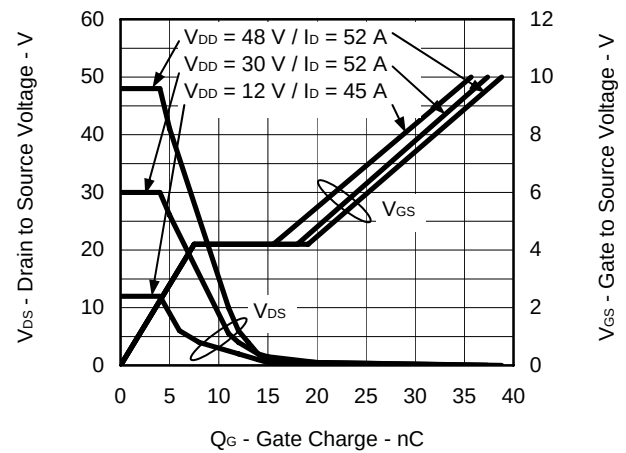
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



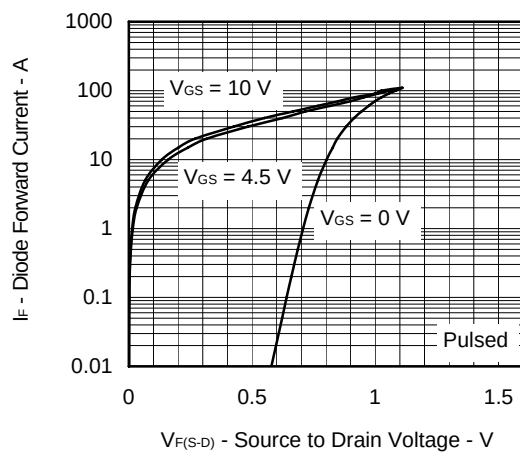
SWITCHING CHARACTERISTICS



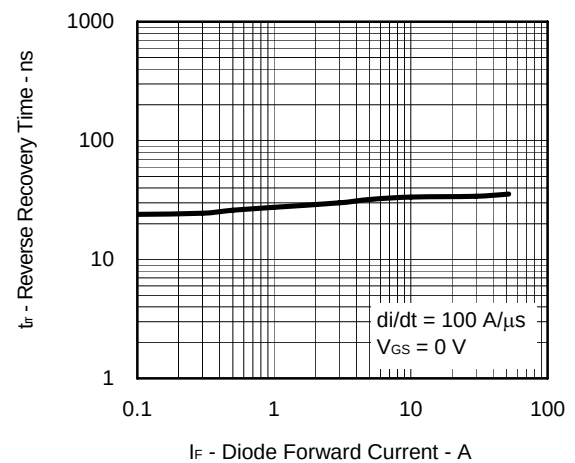
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



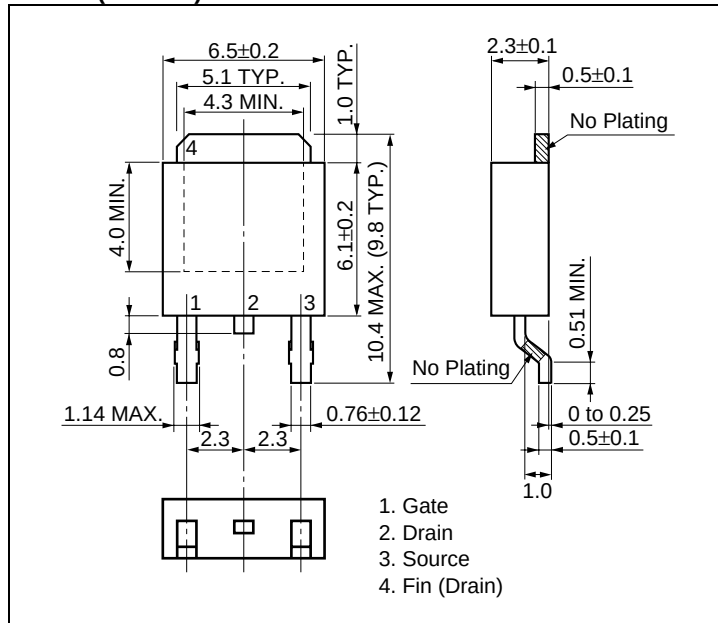
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



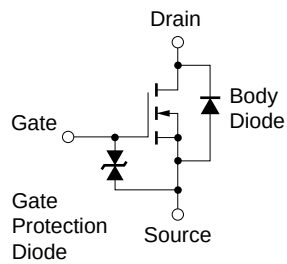
PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)

<R>



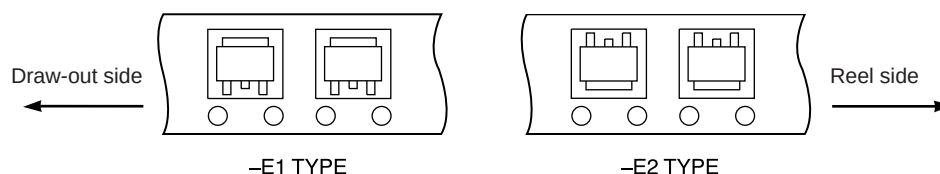
EQUIVALENT CIRCUIT



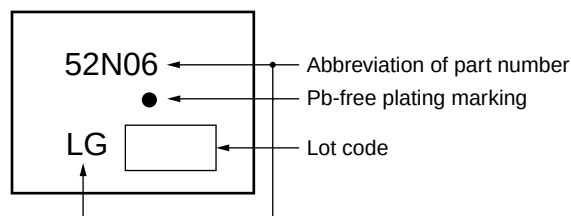
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP52N06SLG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).

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