

LP87702-Q1 Dual Buck Converter and 5-V Boost With Diagnostic Functions

1 Features

- AEC-Q100 Qualified for Automotive Applications:
 - Device Temperature Grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- Two High-Efficiency Step-Down DC/DC converters:
 - Maximum Output Current 3.5 A
 - 2-MHz, 3-MHz, or 4-MHz Switching Frequency
 - Auto PWM/PFM and Forced-PWM Operations
 - Output Voltage = 0.7 V to 3.36 V
- 5-V Boost Converter With Bypass-Mode Option:
 - Maximum Output Current 600 mA
- Two Inputs for External Voltage Monitoring
- Two Programmable Power-Good Signals
- Dedicated Reference Voltage for Diagnostics
- Window Watchdog With Reset Output
- External Clock Input to Synchronize Switching
- Spread-Spectrum Modulation
- Programmable Start-up and Shutdown Delays and Sequencing With Enable Signal
- Configurable General Purpose Outputs (GPOs)
- I²C-Compatible Interface Supporting Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes
- Interrupt Function With Programmable Masking
- Output Short-Circuit and Overload Protection
- Overtemperature Warning and Protection
- Overvoltage Protection (OVP) and Undervoltage Lockout (UVLO)

2 Applications

Automotive Radar, Automotive Camera, Automotive Sensor Fusion, Industrial Radar, Building Automation

3 Description

The LP87702-Q1 meets the power management requirements of the latest platforms, particularly in automotive radar and camera and industrial radar applications. The device contains two step-down DC/DC converters, a 5-V boost converter/bypass switch, two voltage monitoring inputs for external power supplies, and window watchdog. An I²C-compatible serial interface and enable signals control the device.

The automatic PWM/PFM (AUTO mode) operation gives high efficiency over a wide output current range for buck converters. The LP87702-Q1 uses remote voltage sensing for buck converters to compensate IR drop between the converter output and the point-of-load, thus improving the accuracy of the output voltage. In addition, the switching clock can be forced to PWM mode and also synchronized to an external clock for minimal disturbances.

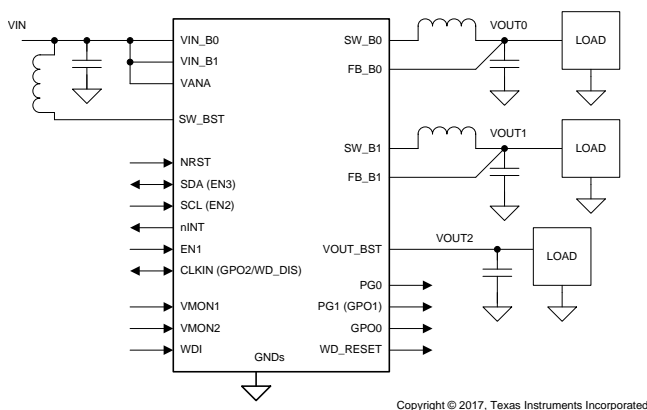
The LP8770 device has internal circuitry specifically designed to support current measurement, eliminating the need for an external resistor. Programmable start-up and shutdown sequences synchronized to the enable signal are supported, including general purpose digital outputs. During start-up and voltage change, the device controls the output slew rate for minimum output voltage overshoot and inrush current.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP87702-Q1	VQFN (32)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Buck Efficiency vs Output Current

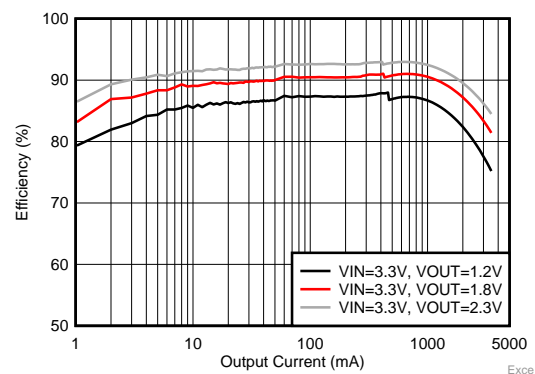


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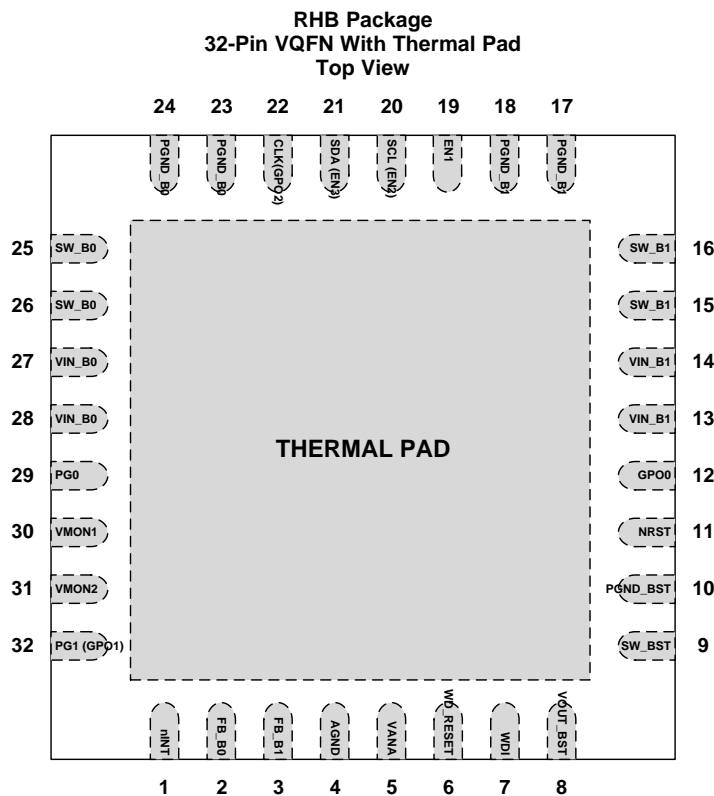
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2017) to Revision A	Page
• First release of production-data data sheet	1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	nINT	D/O	Open-drain interrupt output. Active LOW.
2	FB_B0	A	Output voltage feedback for Buck0.
3	FB_B1	A	Output voltage feedback for Buck1.
4	AGND	G	Ground.
5	VANA	P	Supply voltage for analog and digital blocks. Must be connected to same node with VIN_Bx.
6	WD_RESET	D/O	Reset output from window watchdog
7	WDI	D/I	Digital input signal for window watchdog
8	VOUT_BST	P/O	Boost output. Bypass switch output when this mode is selected.
9	SW_BST	P/I	Boost input. Bypass switch input when this mode is selected.
10	PGND_BST	P/G	Power ground for boost.
11	NRST	D/I	Reset signal for the device.
12	GPO0	D/O	General purpose digital output 0.
13, 14	VIN_B1	P/I	Input for Buck1. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
15, 16	SW_B1	P/O	Buck1 switch node.
17, 18	PGND_B1	P/G	Power Ground for Buck1.
19	EN1	D/I	Programmable Enable 1 signal.
20	SCL	D/I	Serial interface clock input for I2C access. Connect a pullup resistor. Alternative function is programmable enable 2 signal.
21	SDA	D/I/O	Serial interface data input and output for I2C access. Connect a pullup resistor. Alternative function is programmable enable 3 signal.
22	CLKIN	D/I/O	External clock input. Alternative function is general purpose digital output 2 (GPO2). Second alternative function is watchdog disable (WD_DIS)
23, 24	PGND_B0	P/G	Power ground for Buck0.
25, 26	SW_B0	P/O	Buck0 switch node.
27, 28	VIN_B0	P/I	Input for Buck0. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
29	PG0	D/O	Programmable power-good indication signal.
30	VMON1	A/I	Voltage monitoring input 1.
31	VMON2	A/I	Voltage monitoring input 2.
32	PG1	D/O	Programmable power-good indication signal. Alternative function is general purpose digital output 1 (GPO1).
Thermal pad	N/A	G	

A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
VIN_B0, VIN_B1, SW_BST, VANA	Voltage on input power connections	-0.3	6	V
SW_B0, SW_B1	Voltage on buck switch nodes	-0.3	(VIN_Bx + 0.3 V) with 6-V max	V
FB_B0, FB_B1	Voltage on buck voltage sense nodes	-0.3	(VANA + 0.3 V) with 6-V max	V
VOUT_BST	Voltage on boost output	-0.3	6	V
SCL (EN2), SDA (EN3), VMON1, VMON2	Voltage on voltage monitoring pins	-0.3	(VANA + 0.3 V) with 6-V max	V
NRST, EN1, nINT	Voltage on logic pins (input or output pins)	-0.3	6	V
PG0, PG1 (GPO1), GPO0, CLKIN (GPO2), WDI, WD_RESET	Voltage on logic pins (input or output pins)	-0.3	(VANA + 0.3 V) with 6-V max	V
T _{J-MAX}	Junction temperature	-40	150	°C
T _{stg}	Storage temperature	-65	150	°C
Maximum lead temperature (soldering, 10 sec.)			260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground.

6.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000	
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500
			Corner pins (1, 8, 9, 16, 17, 24, 25, 32)	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
INPUT VOLTAGE				
VIN_B0, VIN_B1, SW_BST, VANA	Voltage on input power connections	2.8	5.5	V
VMON1, VMON2	Voltage on voltage monitoring pins	0	5.5	V
NRST, EN1, EN2, EN3, nINT	Voltage on logic pins (input or output pins)	0	5.5	
PG0, PG1 (GPO1), GPO0, CLKIN (GPO2), WDI, WD_RESET	Voltage on logic pins (input or output pins)	0	VANA	V
SCL, SDA	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes	0	1.95	V
	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), and Fast+ (1 MHz) Modes	0	VANA with 3.6-V max	V
TEMPERATURE				
T _J	Junction temperature	-40	140	°C
T _A	Ambient temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		RHB (VQFN)	UNIT
		32 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	31.7	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	17.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	5.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	5.6	°C/W
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq 140^{\circ}\text{C}$, specified V_{VANA} , V_{VIN_Bx} , V_{VOUT_Bx} , V_{VOUT_BST} , and I_{OUT} range, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_Bx} = 3.3\text{ V}$, $V_{VOUT_BST} = 5\text{ V}$ and $V_{VOUT_Bx} = 1\text{ V}$, unless otherwise noted. ^{(1) (2)}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL COMPONENTS						
C _{IN_BUCK}	Input filtering capacitance for buck converters	Effective capacitance, connected from VIN_Bx to PGND_Bx	1.9	10		μF
C _{OUT_BUCK}	Output filtering capacitance for buck converters	Effective total capacitance. Maximum includes POL capacitance	15	22	100	μF
C _{OUT_BUCK_POL}	Point-of-load (POL) capacitance for buck converters	Optional POL capacitance		22		μF
C _{OUT_BST}	Output filtering capacitance for boost converter	Effective capacitance	10	22	40	μF
ESR _C	Input and output capacitor ESR	[1-10] MHz		2	10	mΩ
L _{BUCK}	Inductor for buck converters	Inductance of the inductor		0.47		μH
			-30%		30%	
L _{BST}	Inductor for boost converters	Inductance of the inductor, 2-MHz switching		1		μH
		Inductance of the inductor, 4-MHz switching		1		
		Inductance of the inductor	-30%		30%	
DCR _L	Inductor DCR			25		mΩ
BUCK CONVERTERS						
V _(VIN_Bx) , V _(VANA)	Input voltage range		2.8	3.3	5.5	V
V _{OUT_Bx}	Output voltage	Programmable voltage range	0.7	1	3.36	V
		Step size, $0.7\text{ V} \leq V_{OUT} < 0.73\text{ V}$		10		mV
		Step size, $0.73\text{ V} \leq V_{OUT} < 1.4\text{ V}$		5		
		Step size, $1.4\text{ V} \leq V_{OUT} \leq 3.36\text{ V}$		20		
I _{OUT_Bx}	Output current	Output current			3.5 ⁽³⁾	A
	Minimum voltage difference between V _(VIN_Bx) and V _{OUT_Bx} for electrical characteristics	V _(VIN_Bx) - V _{OUT} , I _{OUT_Bx} ≤ 2 A	0.8			V
		V _(VIN_Bx) - V _{OUT} , I _{OUT_Bx} > 2 A	1			

- (1) All voltage values are with respect to network ground.
- (2) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis.
- (3) The maximum output current can be limited by the forward current limit I_{LIM_FWD}. The maximum output current is also limited by the junction temperature and maximum average current over lifetime. The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length of the current pulse, efficiency, board and ambient temperature.

Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq 140^{\circ}\text{C}$, specified V_{VANA} , $V_{\text{VIN_Bx}}$, $V_{\text{VOUT_Bx}}$, $V_{\text{VOUT_BST}}$, and I_{OUT} range, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$, $V_{\text{VANA}} = V_{\text{VIN_Bx}} = 3.3\text{ V}$, $V_{\text{VOUT_BST}} = 5\text{ V}$ and $V_{\text{VOUT_Bx}} = 1\text{ V}$, unless otherwise noted. ⁽¹⁾ ⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	Force PWM mode, $V_{\text{OUT}} < 1.0\text{ V}$	-20		20	mV	
	Force PWM mode, $V_{\text{OUT}} \geq 1.0\text{ V}$	-2%		2%		
	PFM mode, $V_{\text{OUT}} < 1.0\text{ V}$, the average output voltage level is increased by max. 20 mV	-20		40	mV	
	PFM mode, $V_{\text{OUT}} \geq 1.0\text{ V}$, the average output voltage level is increased by max. 20 mV	-2%		2% + 20mV		
Ripple voltage	PWM mode, $V_{\text{OUT}} = 1.2\text{ V}$, $f_{\text{SW}} = 4\text{ MHz}$, $C_{\text{OUT}} = 22 + 22\text{ }\mu\text{F}$ (GCM31CR71A226KE02)		5		mV _{p-p}	
	PFM mode, $L = 0.47\text{ }\mu\text{H}$, $C_{\text{OUT}} = 22 + 22\text{ }\mu\text{F}$ (GCM31CR71A226KE02)		25			
DC _{LNR}	DC line regulation	$I_{\text{OUT}} = I_{\text{OUT(max)}}$		± 0.05	%/V	
DC _{LDR}	DC load regulation in PWM mode	$V_{\text{OUT_Bx}} = 1.0\text{ V}$, I_{OUT} from 0 to $I_{\text{OUT(max)}}$		0.3%		
T _{LDSR}	Transient load step response	$I_{\text{OUT}} = 0\text{ A}$ to 3 A , $T_R = T_F = 1\text{ }\mu\text{s}$, PWM mode, $V_{\text{VIN_Bx}} = 3.3\text{ V}$, $V_{\text{OUT_Bx}} = 1.2\text{ V}$, $C_{\text{OUT}} = 22 + 22\text{ }\mu\text{F}$, $L = 0.47\text{ }\mu\text{H}$, $f_{\text{SW}} = 4\text{ MHz}$		± 65	mV	
T _{LNSR}	Transient line response	$V_{\text{VIN_Bx}}$ stepping $3\text{ V} \leftrightarrow 3.5\text{ V}$, $T_R = T_F = 10\text{ }\mu\text{s}$, $I_{\text{OUT}} = I_{\text{OUT(max)}}$		± 20	mV	
I _{LIM FWD}	Forward current limit for both bucks (peak for every switching cycle)	Programmable range	1.5		4.5	A
		Step size		0.5		
		Accuracy, $V_{\text{VIN_Bx}} \geq 3\text{ V}$, $I_{\text{LIM}} = 4\text{ A}$	-5%	7.5%	20%	
		Accuracy, $2.8\text{ V} \leq V_{\text{VIN_Bx}} < 3\text{ V}$, $I_{\text{LIM}} = 4\text{ A}$	-20%	7.5%	20%	
I _{LIM NEG}	Negative current limit		1.6	2	3	A
R _{DSON} BUCK HS FET	On-resistance, high-side FET	Each phase, between VIN_Bx and SW_Bx pins ($I = 1.0\text{ A}$)		60	110	m Ω
R _{DSON} BUCK LS FET	On-resistance, low-side FET	Each phase, between SW_Bx and PGND_Bx pins ($I = 1.0\text{ A}$)		55	80	m Ω
f _{SW}	Switching frequency, PWM mode OTP programmable	2-MHz setting or $V_{\text{OUT_Bx}} < 0.8\text{ V}$	1.8	2	2.2	MHz
		3-MHz setting and $V_{\text{OUT_Bx}} \geq 0.8\text{ V}$	2.7	3	3.3	
		4-MHz setting and $V_{\text{OUT_Bx}} \geq 1.1\text{ V}$	3.6	4	4.4	
	Start-up time (soft start)	From ENx to $V_{\text{OUT_Bx}} = 0.35\text{ V}$ (slew-rate control begins)		120		μs
	Overshoot during start-up			50		mV
	Output voltage slew-rate ⁽⁴⁾	SLEW_RATEx[2:0] = 010, $V_{\text{VOUT_Bx}} \geq 0.7\text{ V}$	-15%	10	15%	mV/ μs
	Output voltage slew-rate ⁽⁴⁾	SLEW_RATEx[2:0] = 011, $V_{\text{VOUT_Bx}} \geq 0.7\text{ V}$	-15%	7.5	15%	mV/ μs
	Output voltage slew-rate ⁽⁴⁾	SLEW_RATEx[2:0] = 100, $V_{\text{VOUT_Bx}} \geq 0.7\text{ V}$	-15%	3.8	15%	mV/ μs
	Output voltage slew-rate ⁽⁴⁾	SLEW_RATEx[2:0] = 101, $V_{\text{VOUT_Bx}} \geq 0.7\text{ V}$	-15%	1.9	15%	mV/ μs
	Output voltage slew-rate ⁽⁴⁾	SLEW_RATEx[2:0] = 110, $V_{\text{VOUT_Bx}} \geq 0.7\text{ V}$	-15%	0.94	15%	mV/ μs
	Output voltage slew-rate ⁽⁴⁾	SLEW_RATEx[2:0] = 111, $V_{\text{VOUT_Bx}} \geq 0.7\text{ V}$	-15%	0.47	15%	mV/ μs

(4) The slew-rate can be limited by the current limit (forward or negative current limit), output capacitance and load current. Applies when internal oscillator is used.

Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq 140^{\circ}\text{C}$, specified V_{VANA} , V_{VIN_BX} , V_{VOUT_BX} , V_{VOUT_BST} , and I_{OUT} range, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_BX} = 3.3\text{ V}$, $V_{VOUT_BST} = 5\text{ V}$ and $V_{VOUT_BX} = 1\text{ V}$, unless otherwise noted. ^{(1) (2)}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PFM-PWM}$	PFM-to-PWM switch - current threshold ⁽⁵⁾			520		mA
$I_{PWM-PFM}$	PWM-to-PFM switch - current threshold ⁽⁵⁾			240		mA
	Output pull-down resistance	Converter disabled	75	125	175	Ω
BOOST CONVERTER						
V_{IN_BST}	Input voltage range for boost power inputs		2.8	3.3	4	V
	Input voltage range when bypass switch mode selected		4.5		5.5	V
V_{OUT_BST}	Output voltage, boost mode	BOOST_VSET = 00		4.9		V
		BOOST_VSET = 01		5.0		
		BOOST_VSET = 10		5.1		
		BOOST_VSET = 11		5.2		
I_{OUT_BST}	Output current	Both boost and bypass mode			0.6	A
I_{LIM_BST}	Output current limit	BOOST_ILIM = 00, $V_{IN_BST} < 3.6\text{ V}$	0.8	1	1.3	A
		BOOST_ILIM = 01, $V_{IN_BST} < 3.6\text{ V}$	1.1	1.4	1.9	
		BOOST_ILIM = 10, $V_{IN_BST} < 3.6\text{ V}$	1.5	1.9	2.3	
		BOOST_ILIM = 11, $V_{IN_BST} < 3.6\text{ V}$	2.2	2.8	3.4	
$V_{OUT_BST_DC}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature. Boost mode	Default output voltage	-3%		3%	
V_{DROP}	Voltage drop, bypass mode,	$I_{OUT} = 250\text{ mA}$			83	mV
	Ripple voltage, boost mode	22 μF effective output capacitance		20		mV _{p-p}
DC_{LDR}	DC load regulation, boost mode	$I_{OUT} = 1\text{ mA}$ to $I_{OUT(max)}$		0.3%		
T_{LDSR}	Transient load step response, boost mode	$I_{OUT} = 1\text{ mA}$ to 250 mA, $T_R = T_F = 1\text{ }\mu\text{s}$, 22 μF effective output capacitance, $V_{IN} > 3\text{ V}$	-220		220	mV
I_{SHORT}	Short circuit current limitation	During start-up, both boost and bypass mode. Short circuit current limit applies until $V_{OUT_BST} = V_{IN_BST}$		625		mA
$R_{DS(ON)}$ BST HS FET	On-resistance, high-side FET	Pin-to-pin, between SW_BST and VOUT_BST pins ($I = 250\text{ mA}$)		145	220	m Ω
$R_{DS(ON)}$ BST LS FET	On-resistance, low-side FET	Pin-to-pin, between SW_BST and PGND_BST pins ($I = 250\text{ mA}$)		90	175	m Ω
f_{SW}	Switching frequency, boost mode	2-MHz setting	1.8	2	2.2	MHz
		4-MHz setting	3.6	4	4.4	MHz
	Start-up time, boost mode	From enable to boost VOUT within 3% of target value. $C_{OUT_BST} = 22\text{ }\mu\text{F}$		450		μs
	Output pull-down resistance	Converter disabled		135		Ω

(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level.

Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq 140^{\circ}\text{C}$, specified V_{VANA} , V_{VIN_BX} , V_{VOUT_BX} , V_{VOUT_BST} , and I_{OUT} range, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_BX} = 3.3\text{ V}$, $V_{OUT_BST} = 5\text{ V}$ and $V_{OUT_BX} = 1\text{ V}$, unless otherwise noted. ^{(1) (2)}

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL CLOCK AND PLL					
External input clock ⁽⁶⁾	Nominal frequency	1		24	MHz
	Nominal frequency step size		1		
	Required accuracy from nominal frequency	-30%		10%	
External clock detection	Delay for detecting loss of external clock			1.8	μs
	Delay for detecting valid external clock			20	
Clock change delay (internal to external)	Delay from valid clock detection to use of external clock		600		μs
PLL output clock jitter	Cycle to cycle		300		ns, p-p
MONITORING FUNCTIONS					
VANA Voltage Monitoring	Voltage threshold, VANA_THRESHOLD = 0		3.3		V
	Voltage threshold, VANA_THRESHOLD = 1		5.0		
	Voltage window, VANA_WINDOW = 00	+/-3%	+/-4%	+/-5%	
	Voltage window, VANA_WINDOW = 01	+/-4%	+/-5%	+/-6%	
	Voltage window, VANA_WINDOW = 10 or 11	+/-9%	+/-10%	+/-11%	
VMON1 and VMON2 Voltage Monitoring Thresholds	VMONx_THRESHOLD = 000		0.65		V
	VMONx_THRESHOLD = 001		0.8		
	VMONx_THRESHOLD = 010		1.0		
	VMONx_THRESHOLD = 011		1.1		
	VMONx_THRESHOLD = 100		1.2		
	VMONx_THRESHOLD = 101		1.3		
	VMONx_THRESHOLD = 110		1.8		
	VMONx_THRESHOLD = 111		1.8		
VMON1 and VMON2 Voltage Monitoring Windows	VMONx_WINDOW = 00	+/-1%	+/-2%	+/-3%	
	VMONx_WINDOW = 01	+/-2%	+/-3%	+/-4%	
	VMONx_WINDOW = 10	+/-3%	+/-4%	+/-5%	
	VMONx_WINDOW = 11	+/-5%	+/-6%	+/-7%	
Buck0 and Buck1 Voltage Monitoring Windows	BUCKx_WINDOW = 00	+/-20	+/-30	+/-40	mV
	BUCKx_WINDOW = 01	+/-37	+/-50	+/-63	
	BUCKx_WINDOW = 10	+/-57	+/-70	+/-83	
	BUCKx_WINDOW = 11	+/-77	+/-90	+/-103	
Boost Voltage Monitoring	BOOST_WINDOW = 00	+/-0.6%	+/-2%	+/-3.4%	
	BOOST_WINDOW = 01	+/-2.6%	+/-4%	+/-5.4%	
	BOOST_WINDOW = 10	+/-4.6%	+/-6%	+/-7.4%	
	BOOST_WINDOW = 11	+/-6.6%	+/-8%	+/-9.4%	
Deglitch time	VANA, VMONx and BOOST monitoring	12		17	μs
	BUCKx monitoring	6		9	
PROTECTION FUNCTIONS					
Thermal warning	Temperature rising, TDIE_WARN_LEVEL = 0	115	125	135	°C
	Temperature rising, TDIE_WARN_LEVEL = 1	130	140	150	
	Hysteresis		20		

(6) The external clock frequency must be selected so that buck switching frequency is above 1.7 MHz.

Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq 140^{\circ}\text{C}$, specified V_{VANA} , V_{VIN_Bx} , V_{VOUT_Bx} , V_{VOUT_BST} , and I_{OUT} range, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_Bx} = 3.3\text{ V}$, $V_{VOUT_BST} = 5\text{ V}$ and $V_{VOUT_Bx} = 1\text{ V}$, unless otherwise noted. ⁽¹⁾ ⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown	Temperature rising	140	150	160	°C
	Hysteresis		20		
VANA _{OVP} VANA Overvoltage	Voltage rising, VANA_OVP_SEL = 0	5.6	5.8	6.1	V
	Voltage falling, VANA_OVP_SEL = 0	5.45	5.73	5.96	
	Voltage rising, VANA_OVP_SEL = 1	4.1	4.3	4.6	
	Voltage falling, VANA_OVP_SEL = 1	3.95	4.23	4.46	
	Hysteresis		40		mV
VANA _{UVL} _O VANA Undervoltage Lockout	Voltage rising	2.51	2.63	2.75	V
	Voltage falling	2.5	2.6	2.7	
BUCKx short circuit detection	Threshold	0.32	0.35	0.45	V
Bypass short circuit current limit			270	420	mA
LOAD CURRENT MEASUREMENT FOR BUCK CONVERTERS					
Current measurement range	Maximum code			10.22	A
Resolution	LSB		20		mA
Measurement accuracy	$I_{OUT} > 1\text{ A}$		<10%		
Measurement time	Auto mode (automatically changing to PWM mode for the measurement)		50		µs
	PWM mode		4		
CURRENT CONSUMPTION					
Shutdown current consumption	NRST = 0		1		µA
Standby current consumption, converters disabled	NRST = 1		9		µA
Active current consumption, one buck converter enabled in Auto mode, internal RC oscillator	$I_{OUT_Bx} = 0\text{ mA}$, not switching		55		µA
Active current consumption, two buck converters enabled in Auto mode, internal RC oscillator	$I_{OUT_Bx} = 0\text{ mA}$, not switching		90		µA
Active current consumption during PWM operation, one buck converter enabled	$I_{OUT_Bx} = 0\text{ mA}$		15		mA
Active current consumption during PWM operation, two buck converters enabled	$I_{OUT_Bx} = 0\text{ mA}$		27		mA
Active current consumption, Boost converter in PWM operation	$I_{OUT_BST} = 0\text{ mA}$, $f_{SW} = 4\text{ MHz}$		18		mA
PLL and clock detector current consumption	Additional current consumption when enabled, 2 MHz external clock		2		mA

Electrical Characteristics (continued)

Limits apply over the junction temperature range $-40^{\circ}\text{C} \leq T_J \leq 140^{\circ}\text{C}$, specified V_{VANA} , V_{VIN_Bx} , V_{VOUT_Bx} , V_{VOUT_BST} , and I_{OUT} range, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$, $V_{VANA} = V_{VIN_Bx} = 3.3\text{ V}$, $V_{VOUT_BST} = 5\text{ V}$ and $V_{VOUT_Bx} = 1\text{ V}$, unless otherwise noted. ⁽¹⁾ ⁽²⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT SIGNALS SCL, SDA, NRST, EN1, EN2, EN3, CLKIN, WDI						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.2			
V_{HYS}	Hysteresis of Schmitt Trigger inputs		10	80	200	mV
	ENx, CLKIN, WDI pull-down resistance	ENx_PD = 1, CLKIN_PD = 1, WDI_PD = 1		500		k Ω
	NRST pull-down resistance	Always enabled		500		k Ω
DIGITAL OUTPUT SIGNALS nINT, SDA						
V_{OL}	Output low level	SDA: $I_{SOURCE} = 20\text{ mA}$			0.5	V
		nINT: $I_{SOURCE} = 2\text{ mA}$			0.4	
R_P	External pull-up resistor for nINT	To VIO Supply		10		k Ω
DIGITAL OUTPUT SIGNALS PGOOD, PG1, GPO0, GPO1, GPO2, WD_RESET						
V_{OL}	Output low level	$I_{SOURCE} = 2\text{ mA}$			0.4	V
V_{OH}	Output high level, configured to push-pull	$I_{SINK} = 2\text{ mA}$	$V_{VANA} - 0.4$		V_{VANA}	
V_{PU}	Supply voltage for external pull-up resistor, configured to open-drain				V_{VANA}	
R_{PU}	External pull-up resistor, configured to open-drain			10		k Ω
ALL DIGITAL INPUTS						
I_{LEAK}	Input current	All logic inputs except NRST, over pin voltage range, when PD not enabled	-1		1	μA
		NRST, over pin voltage range. Other logic inputs when PD enabled.	-1		20	μA

6.6 I²C Serial Bus Timing Parameters

See ⁽¹⁾ .		MIN	MAX	UNIT	
f_{SCL}	Serial clock frequency	Standard mode		100	kHz
		Fast mode		400	
		Fast mode +		1	MHz
		High-speed mode, $C_b = 100\text{ pF}$		3.4	
		High-speed mode, $C_b = 400\text{ pF}$		1.7	
t_{LOW}	SCL low time	Standard mode	4.7		μs
		Fast mode	1.3		
		Fast mode +	0.5		
		High-speed mode, $C_b = 100\text{ pF}$	160		ns
		High-speed mode, $C_b = 400\text{ pF}$	320		

(1) C_b refers to the capacitance of one bus line. C_b is expressed in pF units.

I²C Serial Bus Timing Parameters (continued)

See ⁽¹⁾ .		MIN	MAX	UNIT	
t _{HIGH}	SCL high time	Standard mode	4	μs	
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode, C _b = 100 pF	60	ns	
		High-speed mode, C _b = 400 pF	120		
t _{SU;DAT}	Data setup time	Standard mode	250	ns	
		Fast mode	100		
		Fast mode +	50		
		High-speed mode	10		
t _{HD;DAT}	Data hold time	Standard mode	0.01	3.45	μs
		Fast mode	0.01	0.9	
		Fast mode +	0.01		
		High-speed mode, C _b = 100 pF	10	70	ns
		High-speed mode, C _b = 400 pF	10	150	
t _{SU;STA}	Setup time for a start or a repeated start condition	Standard mode	4.7	μs	
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
t _{HD;STA}	Hold time for a start or a repeated start condition	Standard mode	4	μs	
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
t _{BUF}	Bus free time between a stop and start condition	Standard Mode	4.7	μs	
		Fast Mode	1.3		
		Fast mode +	0.5		
t _{SU;STO}	Setup time for a stop condition	Standard Mode	4	μs	
		Fast Mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160	ns	
t _{rDA}	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20+0.1 C _b	300	
		Fast mode +		120	
		High-speed mode, C _b = 100 pF	10	80	
		High-speed mode, C _b = 400 pF	20	160	
t _{fDA}	Fall time of SDA signal	Standard mode		250	ns
		Fast mode	20+0.1 C _b	250	
		Fast mode +	20+0.1 C _b	120	
		High-speed mode, C _b = 100 pF	10	80	
		High-speed mode, C _b = 400 pF	20	160	
t _{rCL}	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20+0.1 C _b	300	
		Fast mode +		120	
		High-speed mode, C _b = 100 pF	10	40	
		High-speed mode, C _b = 400 pF	20	80	

I²C Serial Bus Timing Parameters (continued)

See (1).		MIN	MAX	UNIT	
t _{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	Standard mode	1000	ns	
		Fast mode	20+0.1 C _b		300
		Fast mode +			120
		High-speed mode, C _b = 100 pF	10		80
		High-speed mode, C _b = 400 pF	20		160
t _{rCL}	Fall time of a SCL signal	Standard mode	300	ns	
		Fast mode	20+0.1 C _b		300
		Fast mode +	20+0.1 C _b		120
		High-speed mode, C _b = 100 pF	10		40
		High-speed mode, C _b = 400 pF	20		80
C _b	Capacitive load for each bus line (SCL and SDA)		400	pF	
t _{SP}	Pulse width of spike suppressed (Spikes shorter than indicated width are suppressed)	Fast mode, Fast mode +	50	ns	
		High-speed mode	10		

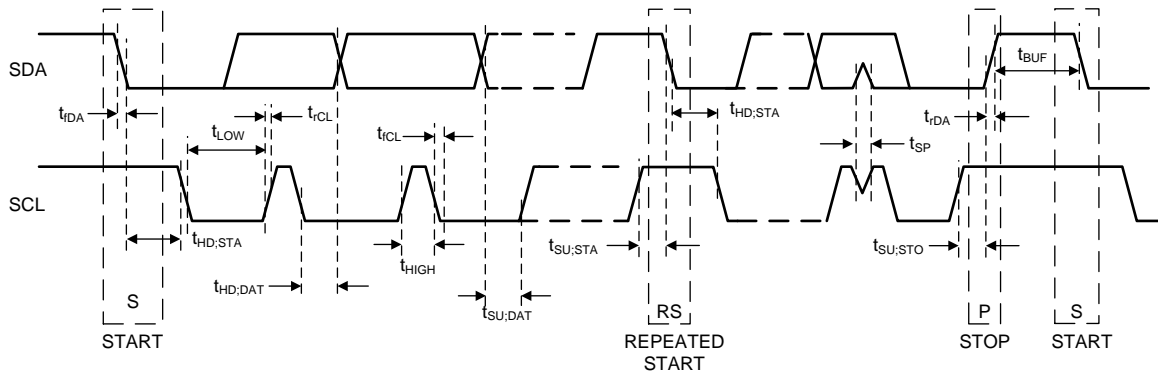
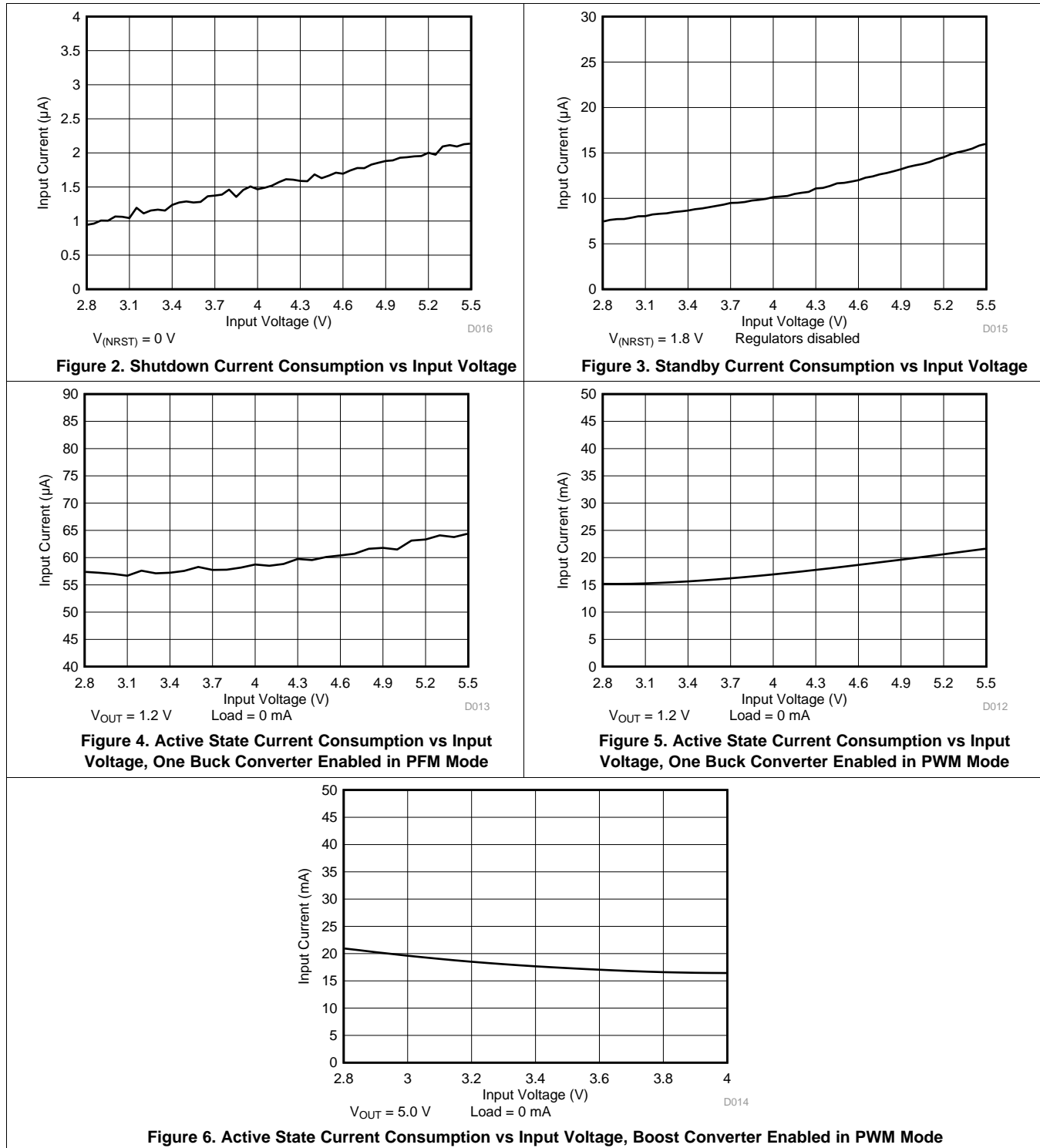


Figure 1. I²C Timing

6.7 Typical Characteristics

Unless otherwise specified: $V_{IN} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, f_{SW} -setting 4 MHz, $L_0 = L_1 = 0.47\ \mu\text{H}$ (TOKO DFE252012PD-R47M), $L_2 = 1\ \mu\text{H}$ (TFM252012ALMA1R0), $C_{OUT_BUCK} = 22\ \mu\text{F}$, and $C_{POL_BUCK} = 22\ \mu\text{F}$, $C_{OUT_BOOST} = 22\ \mu\text{F}$. Measurements are done using connections in the [Figure 81](#).



7 Detailed Description

7.1 Overview

The LP87702-Q1 is a high-efficiency, high-performance power supply IC with two step-down DC/DC converters (Buck0 and Buck1) and boost converter for automotive and industrial applications. [Table 1](#) lists the output characteristics of the various converters. Boost has an alternate bypass switch mode. Selection between boost and bypass modes is defined in OTP and is fixed.

Table 1. Supply Specification

SUPPLY	OUTPUT		
	V _{OUT} RANGE (V)	RESOLUTION (mV)	I _{MAX} MAXIMUM OUTPUT CURRENT (mA)
Boost	4.9 to 5.2	100	600
Buck0	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3500
Buck1	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3500

The LP87702-Q1 converters support switching clock synchronization to an external clock connected to CLKIN input. The external clock can be from 1 MHz to 24 MHz with 1-MHz steps. Alternatively, optional spread spectrum mode can be enabled to reduce EMI.

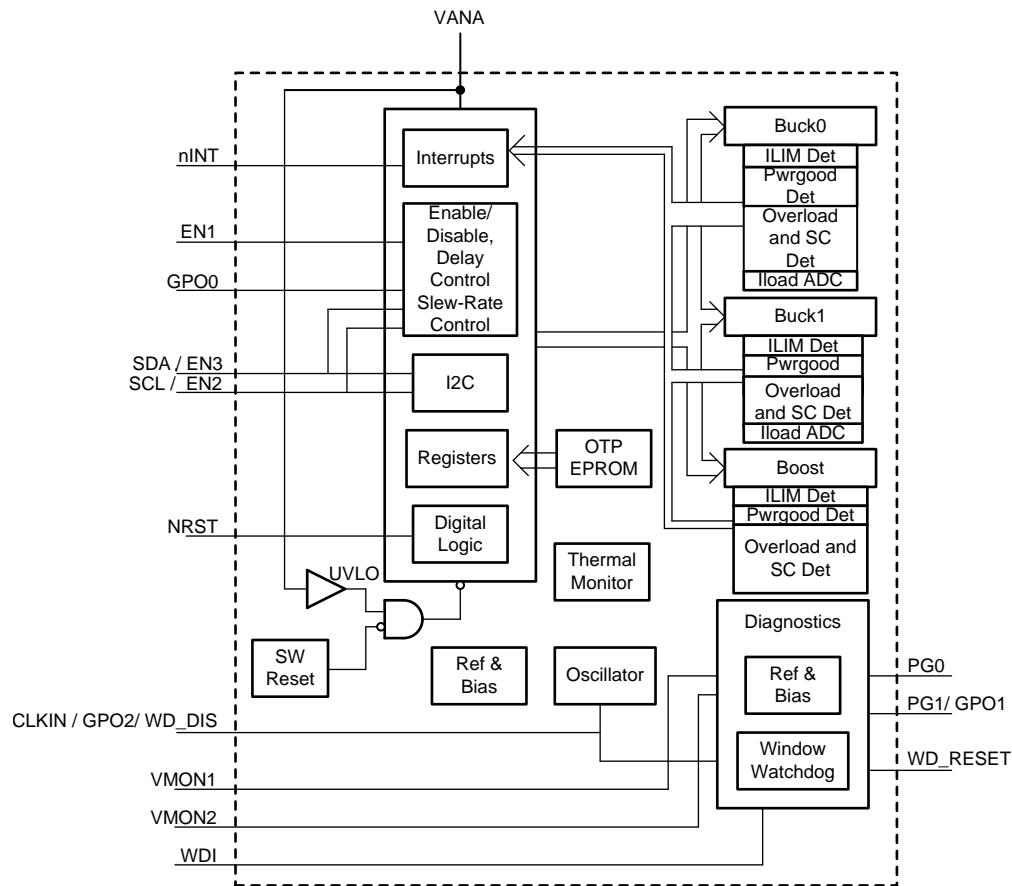
LP87702-Q1 features include diagnostics, monitoring and protections for both device internal and system level operation:

- Soft start
- Input undervoltage lockout
- Programmable undervoltage or window (over- and undervoltage) monitoring for the input (from VANA pin)
- Programmable undervoltage or window (over- and undervoltage) monitoring for the buck and boost converter outputs
- Two inputs (VMONx) with programmable undervoltage or window (over- and undervoltage) thresholds, for monitoring external rails in the system
- One dedicated power-good output (PG0) to which selected monitoring signals can be combined
- Second programmable power-good output (PG1), multiplexed with general purpose output (GPO1)
- Power good flags with maskable interrupt
- Programmable window watchdog
- Buck and boost converter overload detection
- Thermal warning with two selectable thresholds
- Thermal shutdown

LP87702-Q1 control interface:

- Up to three enable inputs (EN1, EN2 and EN3) with programmable power-up/power-down sequence control
- Optional I2C (multiplexed with EN2 and EN3 inputs)
- Interrupt signal (nINT) to host
- Reset input (NRST)
- One dedicated general purpose output (GPO0)
- Watchdog disable WD_DIS, multiplexed with CLKIN/GPO2

7.2 Functional Block Diagram



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7.3 Feature Descriptions

7.3.1 Step-Down DC/DC Converters

7.3.1.1 Overview

The LP87702-Q1 includes two high-efficiency step-down DC/DC converters. The buck converters deliver 0.7-V to 3.36-V regulated voltage rails from 2.8-V to 5.5-V input-supply voltage. The converters are designed for flexibility; most of the functions are programmable, thus optimizing the converter operation for each application:

- DVS support with programmable slew rate
- Automatic mode control based on the loading (PWM or PFM mode)
- Forced PWM mode option
- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Programmable output voltage monitoring with maskable interrupt and selectable connection PG0 and/or PG1
- Average output current sensing (for PFM entry and load current measurement)

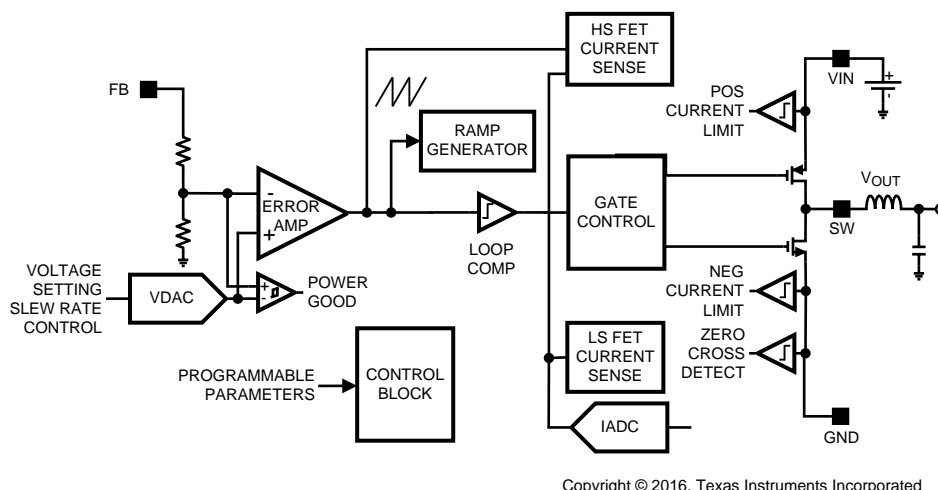
Feature Descriptions (continued)

Some of the key parameters that can be programmed via registers (with default values set by OTP bits):

- Output voltage
- Forced PWM operation
- Switch current limit
- Output voltage slew rate
- Enable and disable delays with ENx pin control

There are two modes of operation for the buck converters, depending on the output current required: pulse width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 520 mA or higher. Lighter output current loads will cause the converter to automatically switch into PFM mode for reduced current consumption when forced PWM mode is disabled. The forced PWM mode can be selected to maintain fixed switching frequency at all load currents. When buck is disabled, buck output is isolated from the input voltage rail. Output has an optional pulldown resistor.

A block diagram of a single buck converter is shown in [Figure 7](#).



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Figure 7. Detailed Block Diagram Showing One Buck Converter

7.3.1.2 Transition Between PWM and PFM Modes

The LP87702-Q1 buck converter operates in PWM mode at load current of about 520 mA or higher. At lighter load current levels the device automatically switches into PFM mode for reduced current consumption when forced PWM mode is disabled (AUTO mode operation). By combining the PFM and the PWM modes a high efficiency is achieved over a wide output-load current range.

7.3.1.3 Buck Converter Load Current Measurement

Buck load current can be monitored via I²C registers. The monitored buck converter is selected with the LOAD_CURRENT_BUCK_SELECT bit in SEL_I_LOAD register. A write to this selection register starts a current measurement sequence. The converter is forced to PWM mode during the measurement. The measurement sequence is 50 μs long at maximum. LP87702-Q1 can be configured to give out an I_MEAS_INT interrupt in INT_TOP_1 register after the load current measurement sequence is finished. Load current measurement interrupt can be masked with I_MEAS_MASK bit in TOP_MASK_1 register. The measurement result can be read from I_LOAD_1 and I_LOAD_2 registers. The Buck converter load current measurement result is 9-bit wide, with 8 LSB bits stored in I_LOAD_1 register and 1 MSB bit stored in I_LOAD_2 register. The single bit resolution is 20 mA, with a maximum load current value of 10.22A.

Feature Descriptions (continued)

7.3.2 Boost Converter

The LP87702-Q1 device integrates a boost converter with programmable output voltage from 4.9V to 5.2V in 0.1V steps, and input voltage range from 2.8V to 4V. The boost converter has flexibility to support wide range of application conditions:

- Forced PWM operation
- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Programmable output voltage monitoring with maskable interrupt and selectable connection to PG0 and/or PG1

Following parameters can be programmed via registers, with default values set by OTP bits unless otherwise noted:

- Output voltage level (BOOST_VSET)
- Switch current limit (BOOST_ILIM)
- Enable and disable delays when ENx pin control is used (BOOST_DELAY register)
- Output pulldown resistor enable/disable when boost is disabled (BOOST_RDIS_EN bit, discharge is enabled by default)
- Output voltage monitoring enable/disable and monitoring window thresholds

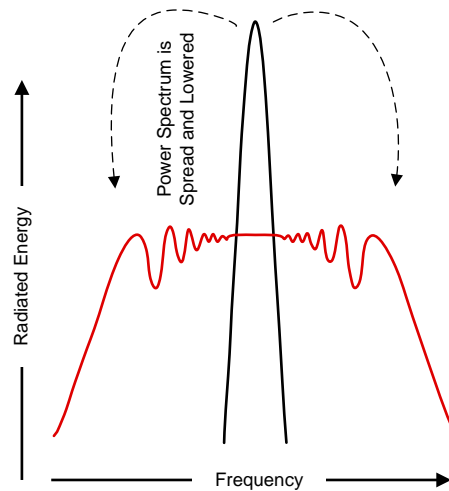
The boost converter operates in forced PWM mode with fixed switching frequency across all load currents. When boost is disabled, boost output is isolated from the input voltage rail.

Boost converter supports an alternative operating mode as a bypass/load switch, with input voltage range from 4.5V to 5.5V. Operating mode is selected in OTP and is fixed, changing the mode on-the-fly is not supported.

7.3.3 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP87702-Q1 device supports spread-spectrum switching frequency modulation mode that is register controlled. This mode minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies between $0.85 \times f_{SW}$ and f_{SW} , where f_{SW} is switching frequency selected in the OTP. Spread spectrum modulation reduces conducted and radiated emissions by the converter and associated passive components and PCB traces (see [Figure 8](#)). This feature is available only when internal RC oscillator is used (EN_PLL is 0 in PLL_CTRL register) and it is enabled with the EN_SPREAD_SPEC bit in CONFIG register, and it affects both buck converters and the boost converter.

Feature Descriptions (continued)



Where a fixed frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP87702-Q1 spreads that energy over a large bandwidth.

Figure 8. Spread Spectrum Modulation

7.3.4 Sync Clock Functionality

The LP87702-Q1 device contains a CLKIN input to synchronize buck and boost converters' switching clock with the external clock. The block diagram of the clocking and PLL module is shown in [Figure 9](#). Depending on the EN_PLL bit in PLL_CTRL register and the external clock availability, the external clock is selected and interrupt is generated as shown in [Table 2](#). The interrupt can be masked with SYNC_CLK_MASK bit in TOP_MASK_1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits in PLL_CTRL register and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%/+10%) for valid clock detection.

The SYNC_CLK_INT interrupt in INT_TOP_1 register is also generated in cases the external clock is expected but it is not available. These cases are Startup (Read OTP-to-standby transition) when EN_PLL = 1 and buck or boost converter is enabled (standby-to-active transition) when EN_PLL = 1.

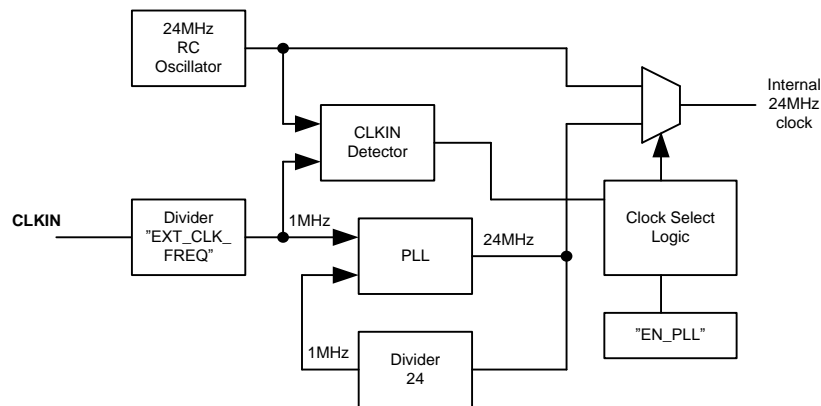


Figure 9. Clock and PLL Module

Feature Descriptions (continued)
Table 2. PLL Operation

DEVICE OPERATION MODE	EN_PLL	PLL AND CLOCK DETECTOR STATE	INTERRUPT FOR EXTERNAL CLOCK	CLOCK
STANDBY	0	Disabled	No	Internal RC
ACTIVE	0	Disabled	No	Internal RC
STANDBY	1	Enabled	When external clock disappears or appears	Automatic change to internal RC oscillator when External clock is not available
ACTIVE	1	Enabled	When external clock disappears or appears	Automatic change to internal RC oscillator when External clock is not available

7.3.5 Power-Up

The power-up sequence for the LP87702-Q1 is as follows:

- VANA (and VIN_Bx) reach minimum recommended levels ($V_{VANA} > VANA_{UVLO}$).
- Driving NRST input high initiates OTP read and enables the system I/O interface. Minimum delay from NRST reset input rising edge to I2C write or read access is 1.2ms.
- Device enters STANDBY mode. Watchdog operation starts.
- The host can change the default register setting by I²C if needed.
- The converters can be enabled/disabled and the GPOx signals can be controlled by ENx pins and by I²C interface.

7.3.6 Buck and Boost Control
7.3.6.1 Enabling and Disabling Converters

The buck converters can be enabled when the device is in STANDBY or ACTIVE state. There are two ways to enable and disable the buck converters:

- Using BUCKx_EN bit in BUCKx_CTRL_1 register (BUCKx_EN_PIN_CTRL bit is 00 in BUCKx_CTRL_1 register)
- Using ENx control pin (BUCKx_EN bit is 1 in BUCKx_CTRL_1 register **AND** BUCKx_EN_PIN_CTRL bit is not 00 in BUCKx_CTRL_1 register)

Similarly there are two ways to enable and disable the boost converter:

- Using BOOST_EN bit in BOOST_CTRL register (BOOST_EN_PIN_CTRL bit is 0 in BOOST_CTRL register)
- Using ENx control pin (BOOST_EN bit is 1 in BOOST_CTRL register **AND** BOOST_EN_PIN_CTRL bit is not 00 in BOOST_CTRL register)

If the ENx control pin is used to enable and disable then the delay from the control signal rising edge to start-up is set by BUCKx_STARTUP_DELAY[3:0] bits in BUCKx_DELAY register and BOOST_STARTUP_DELAY[3:0] bits in BOOST_DELAY register. The delay from falling edge of control signal to shutdown is set by BUCKx_SHUTDOWN_DELAY[3:0] bits in BUCKx_DELAY register and BOOST_SHUTDOWN_DELAY[3:0] bits in BOOST_DELAY register. The delays are valid only when ENx pin control is used, not when converters are enabled by I²C write to BUCKx_EN and BOOST_EN bits.

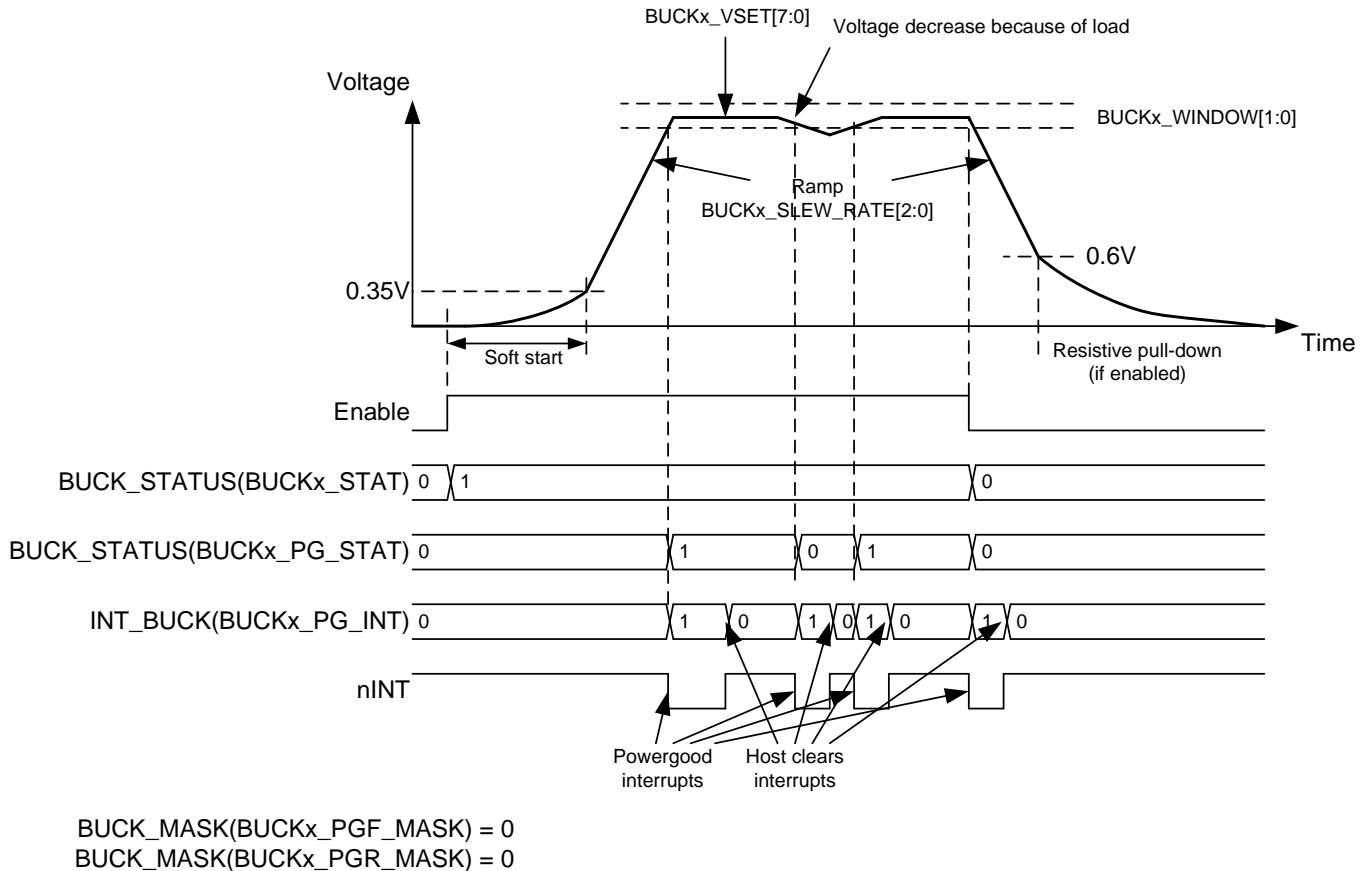
The control of the converters (with 0-ms delays) is shown in [Table 3](#).

Table 3. Converter Control

	BUCKx_EN / BOOST_EN	BUCKx_EN_PIN_C TRL / BOOST_EN_PIN_C TRL	EN1 PIN	EN2 PIN	EN3 PIN	BUCKx OUTPUT VOLTAGE / BOOST OUTPUT VOLTAGE
Enable/disable control with BUCKx_EN/BOOST_EN bit	0	Don't Care	Don't Care	Don't Care	Don't Care	Disabled
	1	00	Don't Care	Don't Care	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable/disable control with EN1 pin	1	01	Low	Don't Care	Don't Care	Disabled
	1	01	High	Don't Care	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable/disable control with EN2 pin	1	10	Don't Care	Low	Don't Care	Disabled
	1	10	Don't Care	High	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable/disable control with EN3 pin	1	11	Don't Care	Don't Care	Low	Disabled
	1	11	Don't Care	Don't Care	High	BUCKx_VSET[7:0] / BOOST_VSET[1:0]

BUCKx converter is enabled by an ENx pin or by I²C write access as shown in [Figure 10](#). The soft-start circuit limits the in-rush current during start-up. Output voltage increase rate is typically 30 mV/μsec during soft start. When the output voltage rises to 0.35-V level, the output voltage becomes slew-rate controlled. If there is a short circuit at the output and the output voltage does not increase above a 0.35-V level in 1 ms, the converter is disabled, and interrupt is set. When the output voltage rises above the undervoltage power-good threshold level the BUCKx_PG_INT interrupt flag in INT_BUCK register is set.

Power-good thresholds are defined by BUCKx_WINDOW bits. A PGOOD_WINDOW bit in PGOOD_CTRL register sets the detection method for the valid buck output voltage, either undervoltage detection or undervoltage and overvoltage detection. The powergood interrupt flag when reaching valid output voltage can be masked using BUCKx_PGR_MASK bit in BUCK_MASK register. The power-good interrupt flag can be also generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by BUCKx_PGF_MASK bit in BUCK_MASK register. When window monitoring (under and overvoltage monitoring) is selected, mask bits apply when voltage is crossing either threshold. A BUCKx_PG_STAT bit in BUCK_STAT register shows always the validity of the output voltage; '1' means valid, and '0' means invalid output voltage.


Figure 10. Buck Converter Enable and Disable

The boost converter is enabled by an ENx pin or by I²C write access as shown in Figure 11. The soft-start circuit limits the in-rush current during start-up. Output voltage increase rate is less than 100 mV/μsec during soft start. If there is a short circuit at the output and the output voltage does not reach input voltage level in 1 ms, the converter is disabled, and interrupt is set. When the output voltage reaches the power-good threshold level the BOOST_PG_INT interrupt flag in INT_BOOST register is set.

Power-good thresholds are defined by BOOST_WINDOW bits. A PGOOD_WINDOW bit in PGOOD_CTRL register sets the detection method for the valid boost output voltage, either undervoltage detection or undervoltage and overvoltage detection. The power-good interrupt flag when reaching valid output voltage can be masked using BOOST_PGR_MASK bit in BOOST_MASK register. The power-good interrupt flag can be also generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by BOOST_PGF_MASK bit in BOOST_MASK register. A BOOST_PG_STAT bit in BOOST_STAT register shows always the validity of the output voltage; '1' means valid and '0' means invalid output voltage.

The ENx input pins have integrated pull-down resistors. The pull-down resistors are enabled by default and host can disable those with ENx_PD bits in CONFIG register.

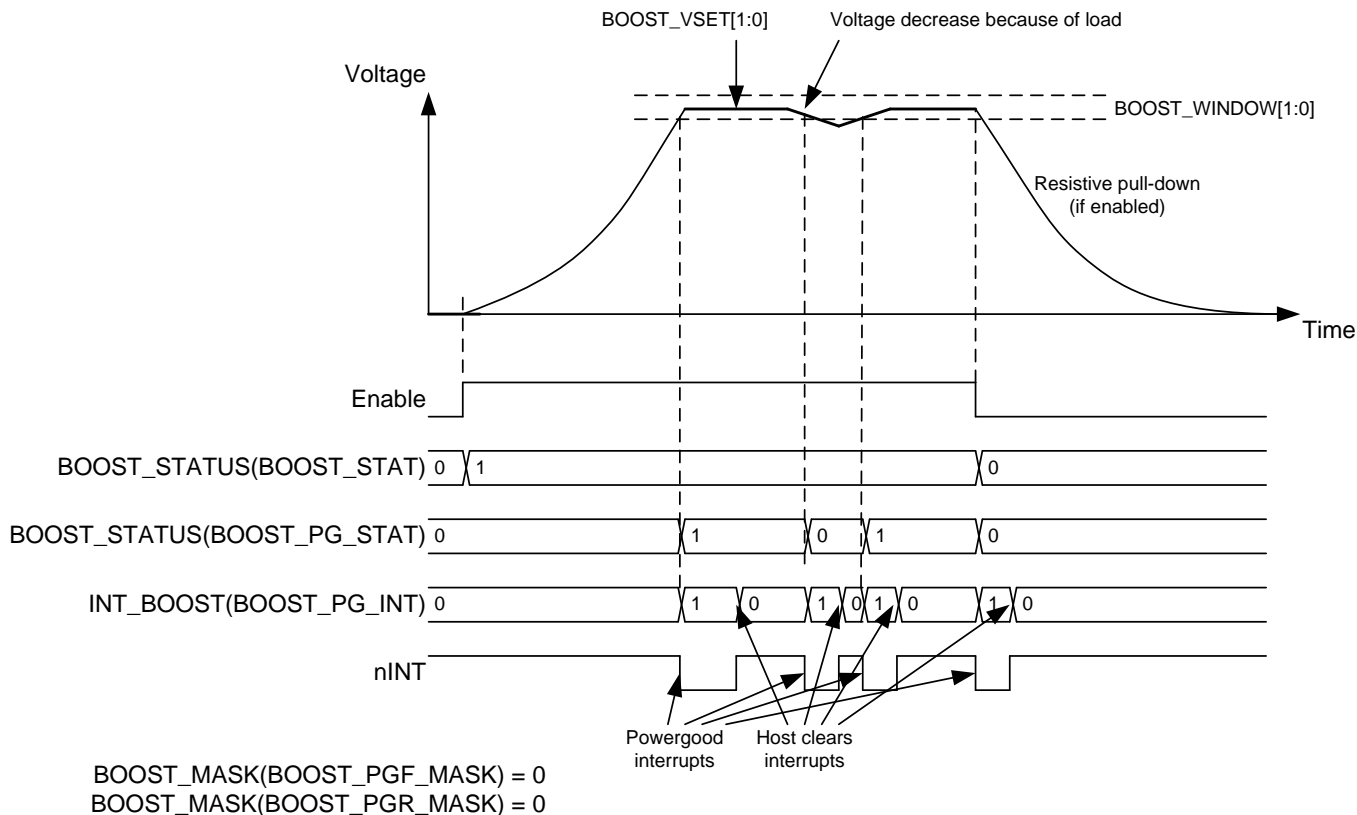
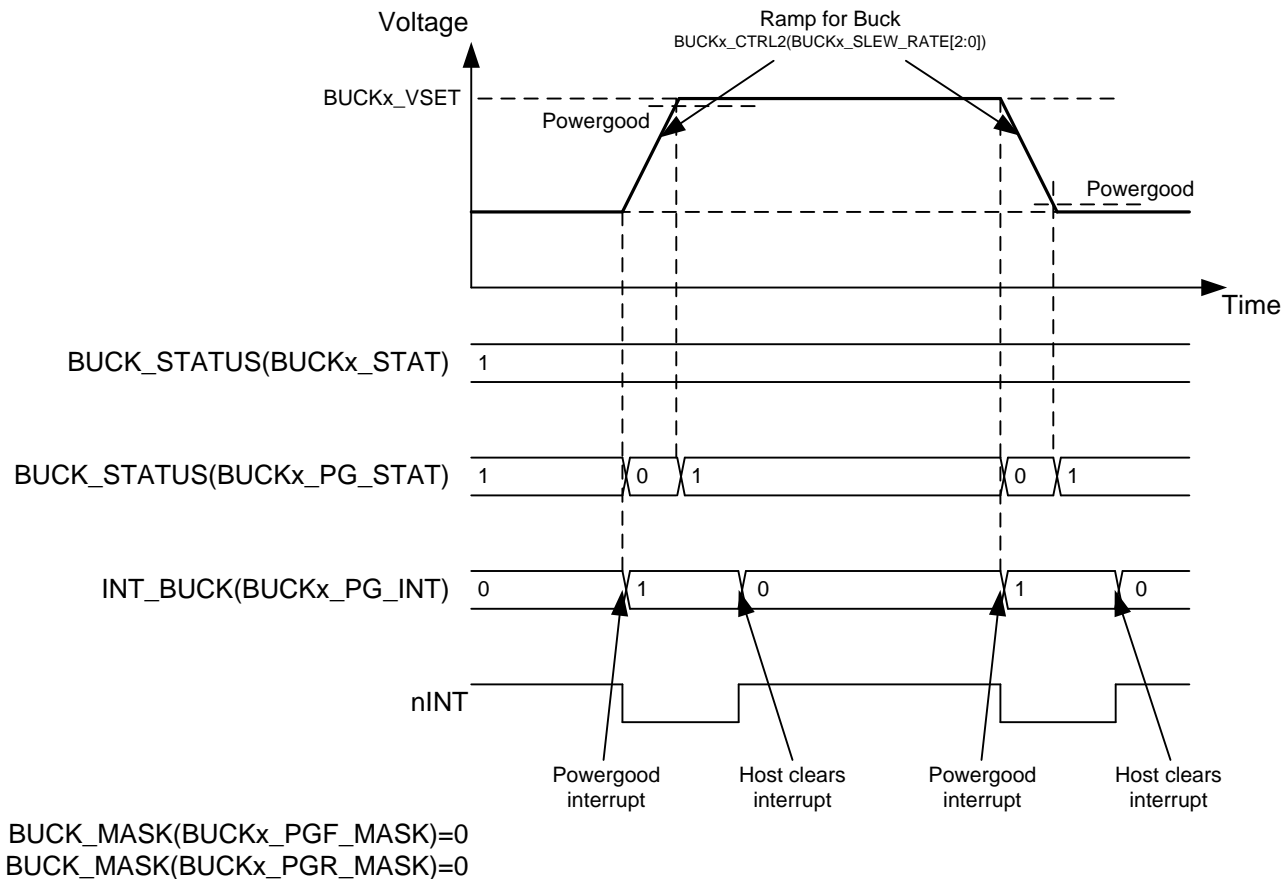


Figure 11. Boost Converter Enable and Disable

7.3.6.2 Changing Buck Output Voltage

The output voltage of BUCKx converter can be changed by writing to the BUCKx_VOUT register. The voltage change for buck converter is always slew-rate controlled, and the slew-rate is defined by the BUCKx_SLEW_RATE[2:0] bits in BUCKx_CTRL_2 register. During voltage change the forced PWM mode is used automatically. When the programmed output voltage is achieved, the mode becomes the one defined by load current, and the BUCKx_FPWM bit.

The voltage change and power-good interrupts are shown in [Figure 12](#).


Figure 12. Buck Output Voltage Change

7.3.7 Enable and Disable Sequences

The LP87702-Q1 device supports programmable start-up and shutdown sequencing. An enable control signal is used to initiate the start-up sequence and to turn off the device according to the programmed shutdown sequence. Up to three enable inputs are available: EN1 is a dedicated enable input and EN2, EN3 are multiplexed with I2C interface. The buck converter is selected for sequence control with:

- BUCKx_CTRL_1(BUCKx_EN) = 1
- BUCKx_CTRL_1(BUCKx_EN_PIN_CTRL) = 0x1 or 0x2 or 0x3, for EN1 or EN2 or EN3 control, respectively
- BUCKx_VOUT.(BUCKx_VSET[7:0]) = Required voltage when EN pin is high
- The delay from rising edge of EN pin to the converter enable is set by BUCKx_DELAY(BUCKx_STARTUP_DELAY[3:0]) bits and
- The delay from falling edge of EN pin to the converter disable is set by BUCKx_DELAY(BUCKx_SHUTDOWN_DELAY[3:0])

In the same way the boost converter is selected for delayed control with:

- BOOST_CTRL(BOOST_EN) = 1
- BOOST_CTRL(BOOST_EN_PIN_CTRL) = 0x1 or 0x2 or 0x3, for EN1 or EN2 or EN3 control, respectively
- BOOST_CTRL(BOOST_VSET[2:0]) = Required voltage when EN pin is high
- The delay from rising edge of EN pin to the converter enable is set by BOOST_DELAY(BOOST_STARTUP_DELAY[3:0]) bits and
- The delay from falling edge of EN pin to the converter disable is set by BOOST_DELAY(BOOST_SHUTDOWN_DELAY[3:0])

An example of start-up and shutdown sequences for buck converters are shown in Figure 13. The start-up and shutdown delays for Buck0 converter are 1 ms and 4 ms and for Buck1 converter 3 ms and 1 ms. The delay settings are used only for enable/disable control with EN signal.

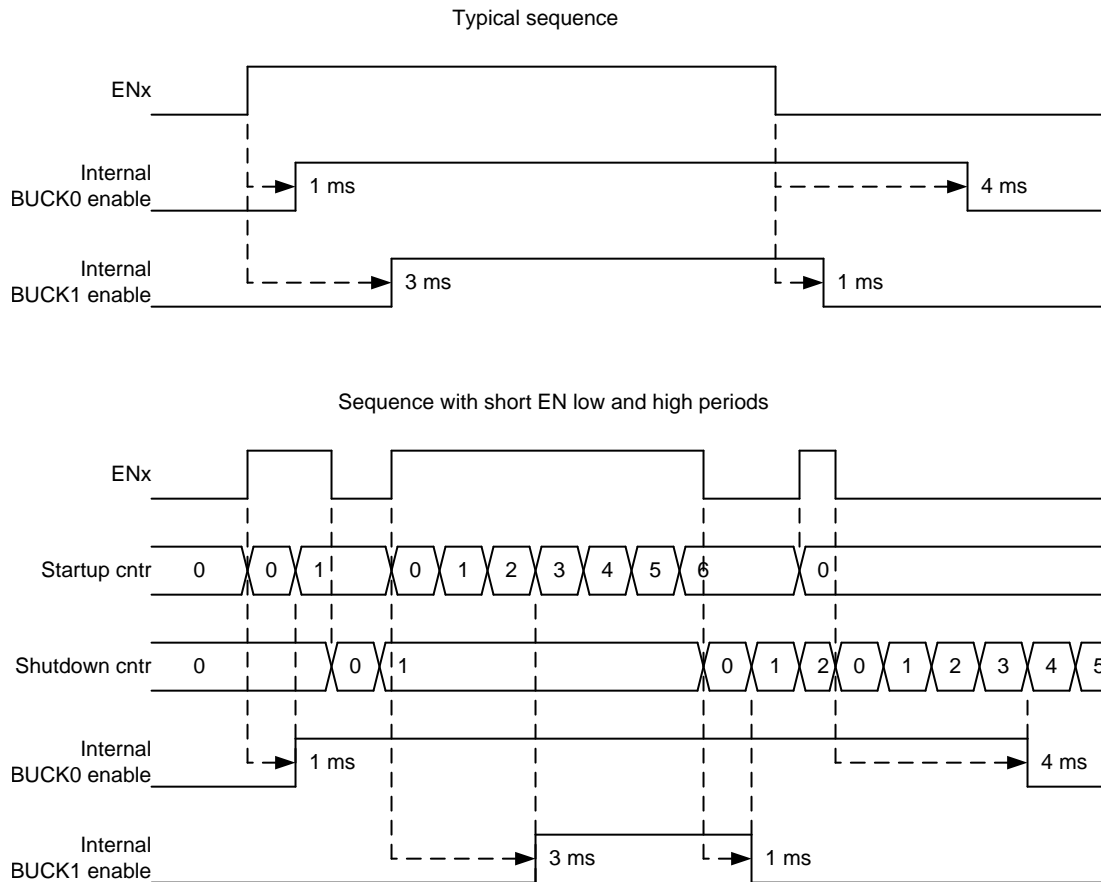


Figure 13. Start-up and Shutdown Sequencing Example

7.3.8 Window Watchdog

Operation of the LP87702-Q1 watchdog is shown in Figure 14 for an example when ENx pin is used for controlling power sequence and ENx pin is active.

WDI is the watchdog function input pin and WD_RESET is the reset output. WDI pin needs to be pulsed within a certain timing window to avoid watchdog expiration. Watchdog expiration always causes a reset pulse at WD_RESET output, otherwise device behavior after watchdog expiration is programmable. WD_RESET output polarity and mode, push-pull or open drain, are also programmable.

Watchdog default settings are read from OTP during device start-up. Default settings in WD_CTRL_1 and WD_CTRL_2 register can be over-written via I2C (as long as WD_LOCK bit is not set to 1). Writing WD_LOCK = 1 in WD_CTRL_2 register locks watchdog settings until NRST input is driven low, power cycle or register reset by SW_RESET.

Long open, close and open window periods are independently programmable as shown in Table 4. When long open or open window expires before WDI input is received, watchdog enters WD Reset state. Also when WDI is received during close window, watchdog enters WD Reset. Long open period can be extended by a I2C write to WD_CTRL_1 or WD_CTRL_2 register; register access initializes the long open counter and the long open period restarts (except in Stop mode).

LP87702-Q1 behavior after WD expiration is programmable :

- When WD_RESET_CNTR_SEL = 00, system restart is disabled and converters are maintained ON. WD_RESET pin is active for 10 ms. Watchdog returns to Long Open mode.
- When WD_RESET_CNTR_SEL = 01 (restart after first reset pulse), LP87702-Q1 performs shutdown

sequence followed by start-up sequence so the converters are disabled and re-enabled according to the OTP programmed sequences. During start-up, device reloads OTP defaults when `WD_EN_OTP_READ = 1`. Settings valid before shutdown are maintained when `WD_EN_OTP_READ = 0`. `WD_RESET` output pin is active for a period of (10 ms + maximum shutdown delay). Maximum shutdown delay can be selected as 7.5 ms (`SHUTDOWN_DELAY_SEL = 0`) or 15 ms (`SHUTDOWN_DELAY_SEL = 1`). After the restart watchdog returns to Long Open mode.

- Status bit `WD_SYSTEM_RESTART_FLAG` is set to indicate that system restart has happened. Status can be cleared by writing "1" to `WD_CLR_SYSTEM_RESTART_FLAG`. `WD_RESET_CNTR_SEL` can be set to 10 or 11 to select restart after 2 or 4 WD expirations, respectively. Current status of reset counter is available in `WD_RESET_CNTR_STATUS`. Reset counter can be cleared by writing `WD_CLR_RESET_CNTR` to 1.
- Watchdog can also be programmed to perform shutdown sequence and enter STOP mode after the first WD expiration. In STOP mode converters are OFF. `WD_RESET` output pin is activated for a period of (10 ms + maximum shutdown delay), in STOP mode `WD_RESET` is inactive. NRST, power cycle, register reset `SW_RESET`, writing `WD_CLR_SYSTEM_RESTART_FLAG = 1` or writing `WD_SYSTEM_RESTART_FLAG_MODE = 0` is required to recover. This WD operating mode is selected by setting OTP bit `WD_SYS_RESTART_FLAG_MODE = 1`.

Watchdog settings in `WD_CTRL_1` and `WD_CTRL_2` registers are locked by setting `WD_LOCK` bit. `WD_SYSTEM_RESTART_FLAG` and `WD_RESET_CNTR_STATUS` can be cleared even if `WD_LOCK = 1`.

Description above is for a case where ENx pin is used for controlling power sequence and ENx pin is active. Depending on OTP settings and ENx pin state watchdog behavior can be slightly different:

- When ENx pin is used for controlling power sequence and ENx pin is not active, shutdown sequence can not be performed. `WD_RESET` pulse length is fixed 31 ms.
- When ENx pins are not used for power sequence control and all converters and GPOs enabled via I2C, there is no OTP defined power sequence. WD expiration does not cause converter disable/enable sequence even when OTP settings for watchdog are such that restart is enabled. In this case `WD_RESET` pulse is 11 ms.

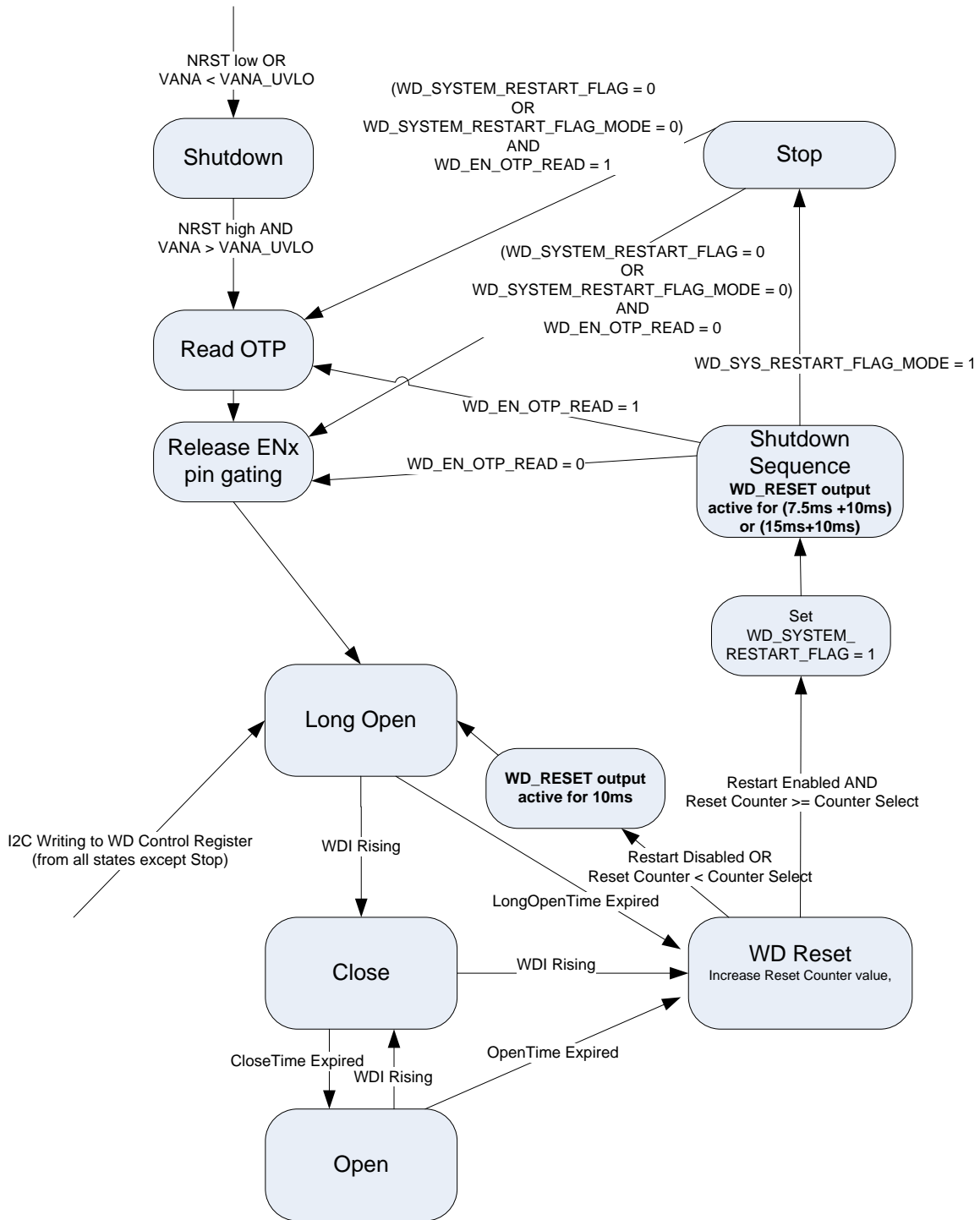


Figure 14. Watchdog Operation

Table 4. Watchdog Window Periods

CONTROL BIT	DEFAULT	VALUES
WD_LONG_OPEN_TIME	OTP	00 - 200 ms 01 - 600 ms 10 - 2000 ms 11 - 5000 ms
WD_CLOSE_TIME	OTP	00 - 10 ms 01 - 20 ms 10 - 50 ms 11 - 100 ms
WD_OPEN_TIME	OTP	00 - 20 ms 01 - 100 ms 10 - 200 ms 11 - 600 ms

LP87702-Q1 supports option to disable watchdog. WD_DIS pin function is multiplexed with CLKIN/GPIO2 functions. Watchdog disable option can be selected by setting register bit WD_DIS_CTRL = 1. When WD_DIS_CTRL = 1, WD is disabled if CLKIN/GPIO2/WD_DIS pin is HIGH and enabled if CLKIN/GPIO2/WD_DIS pin is LOW. If WD_DIS_CTRL is toggled to disable and re-enable WD, WD starts from Long Open window after re-enabling.

Default for WD_DIS_CTRL is set in OTP. WD_DIS_CTRL value can be changed via I2C until WD settings are locked. When WD_LOCK is set to 1, WD is enabled regardless of WD_DIS_CTRL value. WD_DIS_CTRL bit is protected by write lock. Three consecutive codes have to be written to WD_DIS_UNLOCK_CODE to open WD_DIS_CTRL for write access.

7.3.9 Device Reset Scenarios

There are four reset methods implemented on the LP87702-Q1:

- Software reset with SW_RESET bit in RESET register
- NRST input signal low
- Undervoltage lockout (UVLO) reset from VANA supply
- Watchdog expiration (depending on watchdog settings)

A SW reset occurs when SW_RESET bit is set to 1. The bit is automatically cleared after writing. This event disables all the converters immediately, drives GPO signals low, resets all the register bits to the default values and OTP bits are loaded (see [Figure 20](#)). I²C interface is not reset during software reset. The host must wait at least 1.2 ms after writing SW reset until making a new I2C read or write to the device.

If VANA supply voltage falls below UVLO threshold level or NRST signal is set low then all the converters are disabled immediately, GPOx signals are driven low and all the register bits are reset to the default values. When the VANA supply voltage rises above UVLO threshold level and NRST signal rises above threshold level, OTP bits are loaded to the registers and a start-up is initiated according to the register settings. The host must wait at least 1.2 ms before reading or writing to I2C interface.

Depending on watchdog settings, watchdog expiration can reset the device to OTP default values.

7.3.10 Diagnostics and Protection Features

The LP87702-Q1 provides four levels of protection features:

- Information of input and output voltages. Non-valid voltage sets interrupt or PGx signal
 - Validity of the output voltage of BUCK or BOOST converters
 - Validity of VANA, VMON1 and VMON2 input voltages
- Warnings causing interrupt
 - Peak current limit detection in BUCK or BOOST converters
 - Thermal warning
- Protection events which are disabling the converters
 - Short-circuit and overload protection for BUCK and BOOST converters
 - Input overvoltage protection (VANA_{OVP})
 - Watchdog expiration (optional, depends on watchdog settings)

- Thermal shutdown
- Protection events which are causing the device to shutdown
 - Undervoltage lockout ($VANA_{UVLO}$)
- Protections not causing interrupt or converter disable
 - Negative current limit detection in BUCK or BOOST converters

7.3.10.1 Voltage Monitorings

The LP87702-Q1 device has programmable voltage monitoring for the BUCKx and BOOST converter output voltages and for VANA, VMON1 and VMON2 inputs. Monitoring of each signal is independently enabled in PGOOD_CTRL register. Voltage monitoring can be under-voltage monitoring only (PGOOD_WINDOW = 0) or overvoltage and undervoltage monitoring (PGOOD_WINDOW = 1). This selection is common for all enabled monitorings. Enabled monitoring signals are combined to generate power-good (PG0, PG1) and/or interrupts as described in [Power-Good Information to Interrupt and PG0 and PG1 Pins](#). Monitoring comparators have a dedicated reference and bias block, which is independent of the main reference and bias block.

Nominal level for the output voltage of BUCKx converter is set with BUCKx_VSET in BUCKx_VOUT register. Overvoltage and undervoltage detection levels, with respect to nominal level, are selected with BUCKx_WINDOW as ± 30 mV, ± 50 mV, ± 70 mV or ± 90 mV. Nominal level for the output voltage of BOOST converter is set with BOOST_VSET in BOOST_CTRL register. Available levels are 4.9 V, 5 V, 5.1 V and 5.2 V. Overvoltage and undervoltage detection levels, with respect to nominal level, are selected with BOOST_WINDOW as $\pm 2\%$, $\pm 4\%$, $\pm 6\%$ or $\pm 8\%$. Converter monitoring window selection bits are in PGOOD_LEVEL_3 register.

Input voltage of LP87702-Q1 is monitored at VANA pin. Nominal level can be selected as 3.3 V or 5 V with VANA_THRESHOLD bit. Overvoltage and undervoltage detection levels are selected with VANA_WINDOW as $\pm 4\%$, $\pm 5\%$ or $\pm 10\%$ (nominal). VANA_THRESHOLD and VANA_WINDOW are set in PGOOD_LEVEL_2 register.

VMON1 and VMON2 inputs can be used for monitoring external rails in the system. VMONx settings are defined in PGOOD_LEVEL_1 and PGOOD_LEVEL_2 registers. Nominal value for the input level of VMONx is selected with VMONx_THRESHOLD, between 0.65 V to 1.8 V. Higher voltage levels or levels not directly supported can be monitored using an external resistor divider. In this case VMONx_THRESHOLD must be set as 0.65V to have high-impedance input and the resistor divider must scale the monitored level down to 0.65 V at VMONx pin. Overvoltage and undervoltage detection levels are selected with VMONx_WINDOW as $\pm 2\%$, $\pm 3\%$, $\pm 4\%$ or $\pm 6\%$.

For more details on the accuracy of the monitoring windows and deglitch filtering see [Specifications](#).

7.3.10.2 Interrupts

The LP87702-Q1 sets the flag bits indicating what protection or warning conditions have occurred, and the nINT pin is pulled low. nINT output pin is driven high after all flag bits and pending interrupts are cleared.

Fault detection is indicated by RESET_REG_INT interrupt flag bit set in INT_TOP_2 register after start-up event.

Table 5. Summary of Interrupt Signals

EVENT	SAFE STATE	INTERRUPT BIT	INTERRUPT MASK	STATUS BIT	RECOVERY/INTERRUPT CLEAR
Buck current limit triggered (20- μ s debounce)	No effect	BUCKx_INT = 1 BUCKx_ILIM_INT = 1	BUCKx_ILIM_MASK	BUCKx_ILIM_STAT	Write 1 to BUCKx_ILIM_INT bit Interrupt is not cleared if current limit is active
Boost current limit triggered	No effect	BOOST_INT = 1 BOOST_ILIM_INT = 1	BOOST_ILIM_MASK	BOOST_ILIM_STAT	Write 1 to BOOST_ILIM_INT bit Interrupt is not cleared if current limit is active
Buck short circuit ($V_{OUT} < 0.35V$ at 1 ms after enable) or Overload (V_{OUT} decreasing below 0.35 V during operation, 1 ms debounce)	Converter disable	BUCKx_INT = 1 BUCKx_SC_INT = 1	N/A	N/A	Write 1 to BUCKx_SC_INT bit
Boost short circuit	Converter disable	BOOST_INT = 1 BOOST_SC_INT = 1	N/A	N/A	Write 1 to BOOST_SC_INT bit
Thermal warning	No effect	TDIE_WARN_INT = 1	TDIE_WARN_MASK	TDIE_WARN_STAT	Write 1 to TDIE_WARN_INT bit Interrupt is not cleared if temperature is above thermal warning level
Thermal shutdown	All converters disabled immediately and GPOx set to low	TDIE_SD_INT = 1	N/A	TDIE_SD_STAT	Write 1 to TDIE_SD_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
VANA overvoltage ($VANA_{OVP}$)	All converters disabled immediately and GPOx set to low	OVP_INT	N/A	OVP_STAT	Write 1 to OVP_INT bit Interrupt is not cleared if VANA voltage is above $VANA_{OVP}$ level
Buck power-good, output voltage becomes valid	No effect	BUCK_INT = 1 BUCKx_PG_INT = 1	BUCKx_PGR_MASK	BUCKx_PG_STAT	Write 1 to BUCKx_PG_INT bit
Buck power-good, output voltage becomes invalid	No effect	BUCK_INT = 1 BUCKx_PG_INT = 1	BUCKx_PGF_MASK	BUCKx_PG_STAT	Write 1 to BUCKx_PG_INT bit
Boost power-good, output voltage becomes valid	No effect	BOOST_INT = 1 BOOST_PG_INT = 1	BOOST_PGR_MASK	BOOST_PG_STAT	Write 1 to BOOST_PG_INT bit
Boost power-good, output voltage becomes invalid	No effect	BOOST_INT = 1 BOOST_PG_INT = 1	BOOST_PGF_MASK	BOOST_PG_STAT	Write 1 to BOOST_PG_INT bit
VMON1 power-good, input voltage becomes valid	No effect	DIAG_INT = 1 VMON1_PG_INT = 1	VMON1_PGR_MASK	VMON1_PG_STAT	Write 1 to VMON1_PG_INT bit
VMON1 power-good, input voltage becomes invalid	No effect	DIAG_INT = 1 VMON1_PG_INT = 1	VMON1_PGF_MASK	VMON1_PG_STAT	Write 1 to VMON1_PG_INT bit
VMON2 power-good, input voltage becomes valid	No effect	DIAG_INT = 1 VMON2_PG_INT = 1	VMON2_PGR_MASK	VMON2_PG_STAT	Write 1 to VMON2_PG_INT bit
VMON2 power-good, input voltage becomes invalid	No effect	DIAG_INT = 1 VMON2_PG_INT = 1	VMON2_PGF_MASK	VMON2_PG_STAT	Write 1 to VMON2_PG_INT bit
VANA power-good, input voltage becomes valid	No effect	DIAG_INT = 1 VANA_PG_INT = 1	VANA_PGR_MASK	VANA_PG_STAT	Write 1 to VANA_PG_INT bit
VANA power-good, input voltage becomes invalid	No effect	DIAG_INT = 1 VANA_PG_INT = 1	VANA_PGF_MASK	VANA_PG_STAT	Write 1 to VANA_PG_INT bit
External clock appears or disappears	No effect to converters	SYNC_CLK_INT ⁽¹⁾	SYNC_CLK_MASK	SYNC_CLK_STAT	Write 1 to SYNC_CLK_INT bit
Load current measurement ready	No effect	I_MEAS_INT = 1	I_MEAS_MASK	N/A	Write 1 to I_MEAS_INT bit
Supply voltage $VANA_{UVLO}$ triggered (VANA falling)	Immediate shutdown, registers reset to default values	N/A	N/A	N/A	N/A
Supply voltage $VANA_{UVLO}$ triggered (VANA rising)	Start-up, registers reset to default values and OTP bits loaded	RESET_REG_INT = 1	RESET_REG_MASK	N/A	Write 1 to RESET_REG_INT bit
Software requested reset	Immediate shutdown followed by powerup, registers reset to default values	RESET_REG_INT = 1	RESET_REG_MASK	N/A	Write 1 to RESET_REG_INT bit

(1) Interrupt generated during Clock Detector operation and in case Clock is not available when Clock Detector is enabled.

7.3.10.3 Power-Good Information to Interrupt and PG0 and PG1 Pins

LP87702-Q1 supports both interrupt based indication of power-good levels for various voltage settings and using two power-good signals, PG0 and PG1. The selection of monitored signals is independent for the interrupt (nINT) and PG0, PG1 signals. Each signal can include:

- The output voltage of one or both BUCKx converters
- The output voltage of the BOOST converter
- Input voltage of VANA
- Input voltage of VMON1 and/or VMON2
- Thermal warning

The block diagram for power-good connections to PG0 and PG1 pins and interrupt is shown in [Figure 15](#).

Monitored signals are enabled in PGOOD_CTRL register. Converter output voltage monitoring (not current limit monitoring) can be selected for the indication. Monitoring is enabled by EN_PGOOD_BUCKx and EN_PGOOD_BOOST bits. When a converter is disabled, the monitoring is automatically masked to prevent it forcing PGx inactive or causing an interrupt. Also monitoring of VANA, VMON1 and VMON2 inputs can be independently enabled via PGOOD_CTRL register. The type of voltage monitoring for PGx signals and nINT is selected by PGOOD_WINDOW bit. If the bit is 0, only undervoltage is monitored and if the bit is 1 both undervoltage and overvoltage are monitored. For voltage monitoring thresholds see [Voltage Monitorings](#).

Monitoring interrupts from all the output rails, input rails and thermal warning are combined to nINT pin. Dedicated mask bits are used to select which interrupts control the state of nINT pin. See [Table 5](#) for summary of interrupts, mask bits and interrupt clearing.

Similarly, enabled monitoring signals from all the output rails, input rails and thermal warning are combined to PG0 and PG1 output pins. Register bits SEL_PGx_x in PG0_CTRL and PG1_CTRL select which of the signals control the state of PG0 and PG1, respectively. The polarity and the output type (push-pull or open-drain) of PG0 and PG1 are selected by PGx_POL and PGx_OD bits in PG_CTRL register.

PGx is only *active* or *asserted* when all monitored input voltages and all output voltages of monitored and enabled converters are within specified tolerance of set target value.

PGx is *inactive* or *de-asserted* if any of the monitored input voltages or output voltages of monitored and enabled converters are outside specified tolerance of set target value.

When PGx_RISE_DELAY = 1, PGx is set as *active* or *asserted* with 11 ms delay from the point of time where all enabled power resource output voltages are within specified tolerance for each requested/programmed output voltage.

Thermal shutdown and VANA overvoltage protection events force PGx to default state (assuming PGx polarity set in OTP is active high, PGx are drive low).

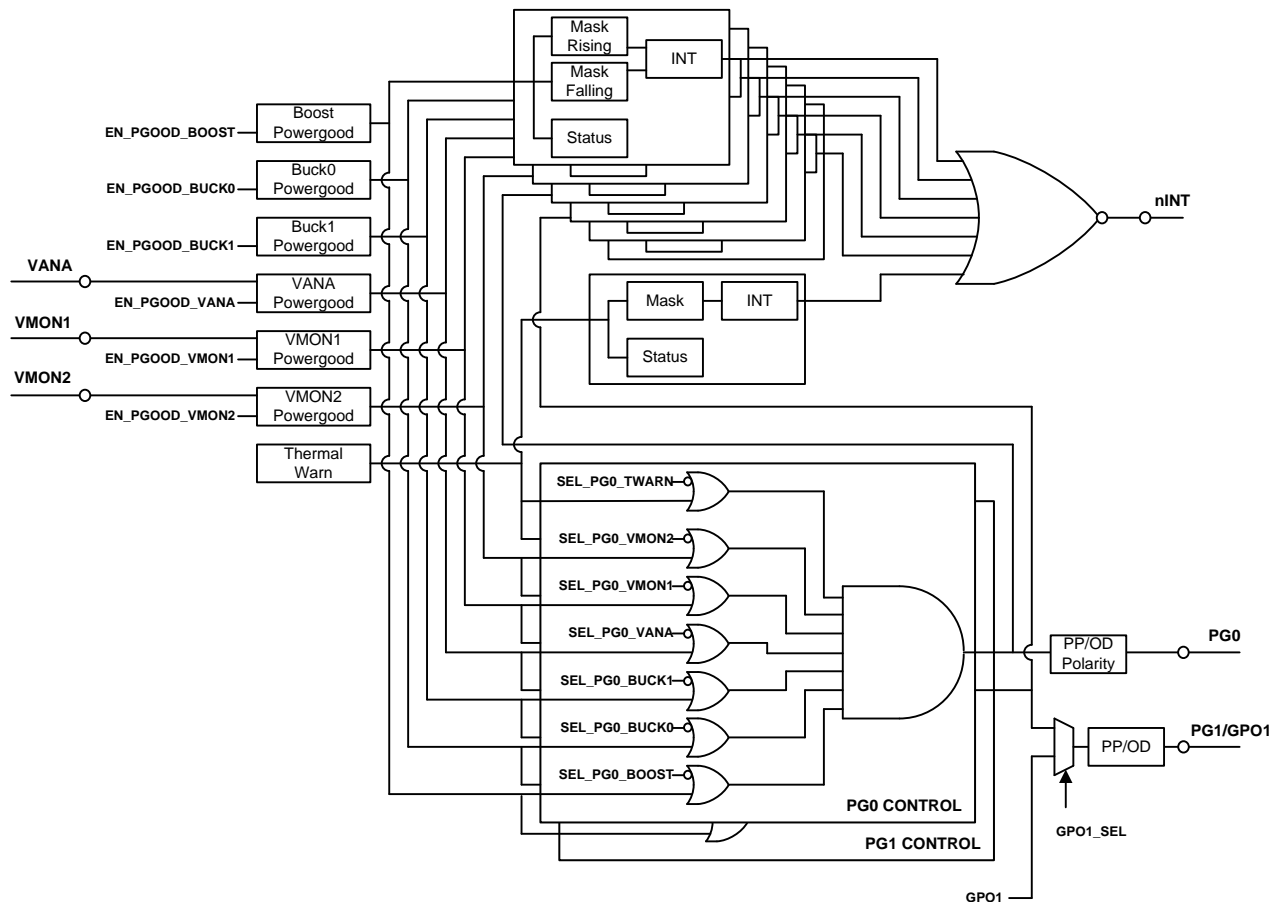


Figure 15. Block Diagram of Power-Good Connections

LP87702-Q1 power-good detection has two operating modes, selected in OTP: gated (that is, *unusual*) or continuous (that is, *invalid*) mode of operation. These modes are described in [PGx Pin Gated \(Unusual\) Mode](#) and in [PGx pin Operation in Continuous Mode](#).

7.3.10.3.1 PGx Pin Gated (Unusual) Mode

In this mode the PGx signal detects unexpected or unusual situations. Mode is selected by setting PGx_MODE bit to 0 in PG_CTRL register.

For the gated mode of operation, PGx behaves as follows:

- PGx is set to active or asserted state upon exiting OTP configuration as an initial default state.
- For each enabled rail PGx status is suspended or unchanged during an 800- μ s gated time period from the enable activation, thereby *gating-off* the status indication.
- During normal power-up sequencing and requested voltage changes, PGx state typically remains *active* or *asserted* for normal conditions.
- During an abnormal power-up sequencing and requested voltage changes, PGx status could change to *inactive* or *de-asserted* after an 800- μ s gated time period if any output voltage is outside of regulation range.
- Using the gated mode of operation could allow the PGx signal to initiate an immediate power shutdown sequence if the PGx signal is wired-OR with signal connected to EN input. This type of circuit configuration provides a smart PORz function for processor that eliminates the need for additional components to generate PORz upon start-up and to monitor voltage levels of key voltage domains.

PGx signal is set inactive if the output voltage of a monitored buck or boost converter is invalid or the output voltage is not valid at 800 μ s from the enable of the converter. This should be considered when selecting the BUCKx_SLEW_RATE setting. To avoid PGx triggering at start-up keep the sum of soft start time and slew rate controlled part of voltage ramp below 800 μ s. In addition when invalid input voltage at VANA, VMON1 or VMON2 pin is detected PGx is inactive.

Detected fault sets the corresponding fault bit in PG0_FAULT or in PG1_FAULT register. The detected fault must be cleared to continue the PGx monitoring. The over-voltage and thermal faults are cleared by writing 1 to the corresponding interrupt bits in INT_TOP_1 register. Converter, VMONx and VANA faults are cleared by writing 1 to the corresponding register bit in INT_BUCK, INT_BOOST and INT_DIAG register, respectively. An example of PGx pin operation in gated mode is shown in Figure 16 and the different use cases for PGx signal operation are summarized in Table 6.

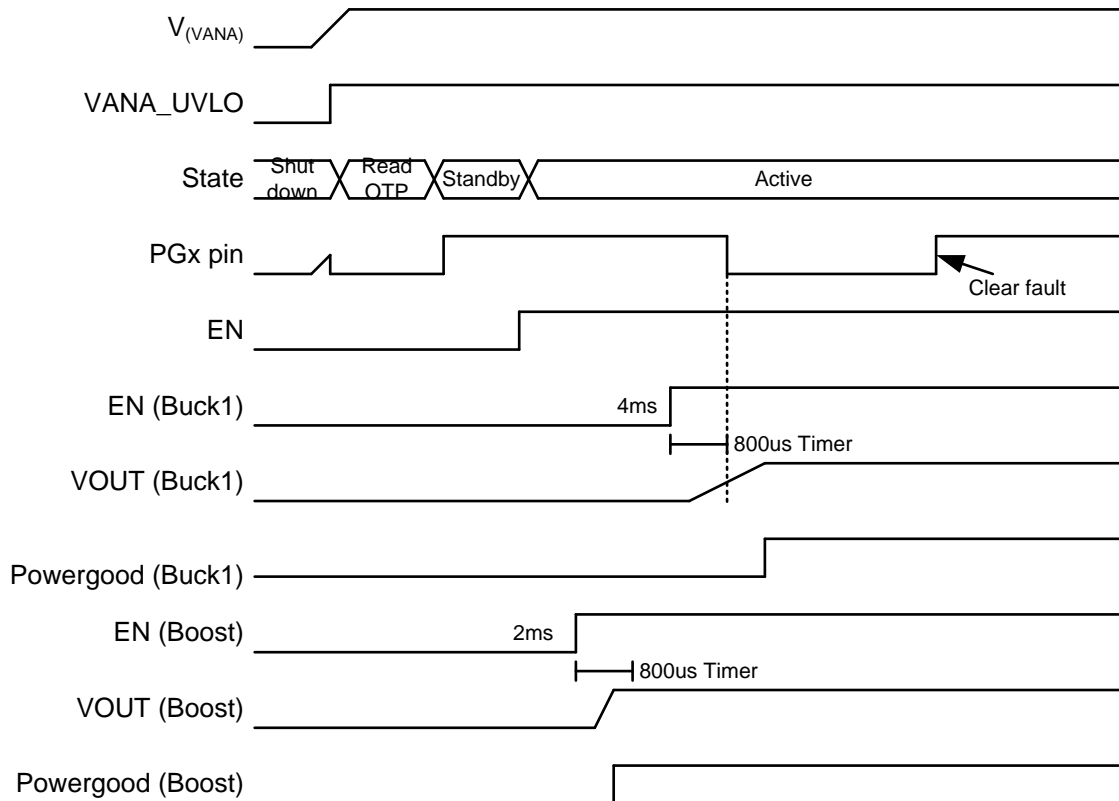


Figure 16. PGx Pin Operation in Gated Mode.

7.3.10.3.2 PGx pin Operation in Continuous Mode

In this mode the PGx signal shows the validity of the requested voltages continuously. Mode is selected by setting PGx_MODE bit to 1 in PG_CTRL register.

For the continuous mode of operation, PGx behaves as follows:

- PGx is set to *active* or *asserted* state upon exiting OTP configuration as an initial default state.
- PGx is set to *inactive* or *de-asserted* as soon as converter is enabled.
- PGx status begins indicating output voltage regulation status immediately and continuously.
- During power-up sequencing and requested voltage changes, PGx will toggle between *inactive* or *deasserted* while output voltages are outside of regulation ranges and active or asserted when inside of regulation ranges.

When invalid output voltage of monitored converter is detected, corresponding bit in PG0_FAULT or PG1_FAULT register is set to 1 and PGx signal becomes inactive. The PG0_FAULT and PG1_FAULT register bits are latched and maintain the fault information until host clears the fault bit by writing 1 to the bit. The PGx signal indicates also interrupts from VANA, VMON1 and VMON2 inputs and thermal warning and shutdown. All are cleared by clearing the interrupt bits.

When converter voltage is transitioning from one target voltage to another, the PGx signal is set inactive.

When PGx signal becomes inactive, the source for the fault can be read from PGx_FAULT register. If the invalid output voltage becomes valid again the PGx signal becomes active. Thus the PGx signal shows all the time if the monitored output voltages are valid. An example of PGx pin operation in continuous mode is shown in Figure 17.

The PGx signal can be also configured so that it maintains inactive state even when the monitored outputs are valid but there are PG_FAULT_x bits pending clearance. This type of operation is selected by setting PGOOD_FAULT_GATES_PGx bit to 1.

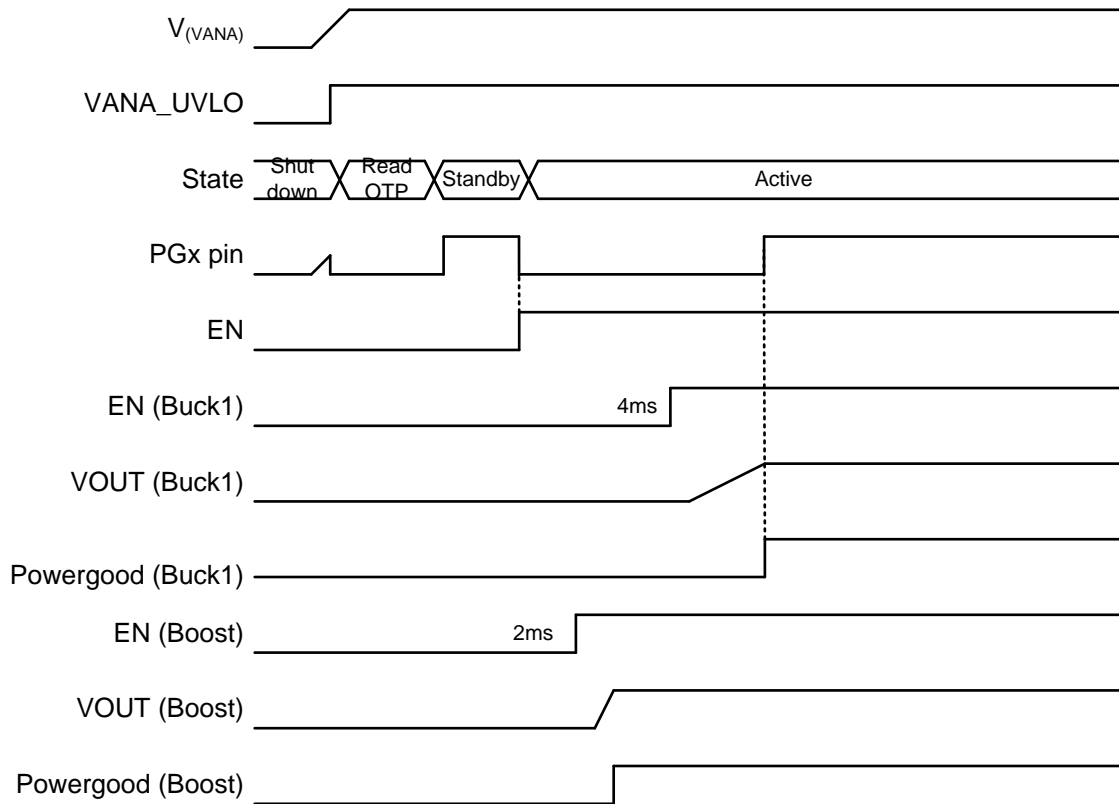


Figure 17. PGx Pin Operation in Continuous Mode

7.3.10.3.3 Summary of PG0, PG1 Gated and Continuous Operating Modes

Table 6 summarizes the PGx behavior in different application scenarios, for the gated and continuous operating modes.

Table 6. PGx Operation

STATUS / USE CASE	CONDITION	PGx SIGNAL ⁽¹⁾⁽²⁾	
		GATED MODE PGx_MODE = 0	CONTINUOUS MODE PGx_MODE = 1
Device start-up	Until device state is STANDBY	Low	Low
Converter not selected for PGx monitoring	EN_PGOOD_x = 0	OK	OK
Converter selected for PGx monitoring and disabled by host	BUCKx_EN / BOOST_EN = 0 OR (Pin ctrl AND EN = 0)	OK	OK
Converter start-up delay ongoing	EN = 1	OK	NOK
Converter start-up until valid output voltage reached	Valid output voltage reached in 800 μ s	OK	NOK
Converter start-up until valid output voltage reached	Valid output voltage not reached at 800 μ s	NOK	NOK
Output voltage within window limits after start-up	Must be inside limits longer than debounce time	OK	OK
Output voltage spikes (over/undervoltage)	If spikes are outside voltage monitoring threshold(s) longer than debounce time	NOK	NOK
Voltage setting change, output voltage ramp		OK (if new voltage reached in 800 μ s) NOK after 800 μ s (if new voltage not reached at 800 μ s)	NOK
Output voltage within window limits after voltage change	Must be inside limits longer than debounce time	OK	OK
Converter shutdown delay ongoing		OK	OK
Buck converter disabled by host, slew-rate controlled ramp down ongoing		OK	OK
Converter disabled by host, pulldown resistor active (if selected)		OK	OK
Converter short-circuit interrupt pending (converter selected for PGx monitoring)	Faulty converter disabled by short-circuit detection BUCKx_SC_INT / BOOST_SC_INT = 1	NOK	NOK
Thermal shutdown interrupt pending	Converters disabled by thermal shutdown detection TDIE_SD_INT = 1	NOK	NOK
Input (VANA) overvoltage interrupt pending	Converters disabled by overvoltage detection OVP_INT = 1	NOK	NOK
Supply voltage below VANA _{UVLO}		Low	Low

(1) NOK (Not OK) means faulty situation. PGx pin is inactive if at least one NOK situation is detected.

(2) PGx pin is generated from PG_FAULT register bits and INT_TOP_1 register bits TDIE_SD_INT, OVP_INT and INT_TOP_2(RESET_REG_INT) bit.

7.3.10.4 Warning Interrupts for System Level Diagnostics

7.3.10.4.1 Output Power Limit

The buck converters have programmable output peak current limits. The limits are individually programmed for both converters with BUCKx_ILIM[2:0] bits. If the load current is increased so that the current limit is triggered, the converter continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 20 μ s, the LP87702-Q1 device sets the BUCKx_ILIM_INT bit and pulls the nINT pin low. The host processor can read BUCKx_ILIM_STAT bits to see if the converter is still in peak current regulation mode.

If the load is so high that the output voltage decreases below a 350-mV level, the LP87702-Q1 device disables the converter and sets the BUCKx_SC_INT bit. In addition the BUCKx_SC_STAT bit is set to 0. The interrupt is cleared when the host processor writes 1 to BUCKx_SC_INT bit. The Buck overload situation is shown in Figure 18.

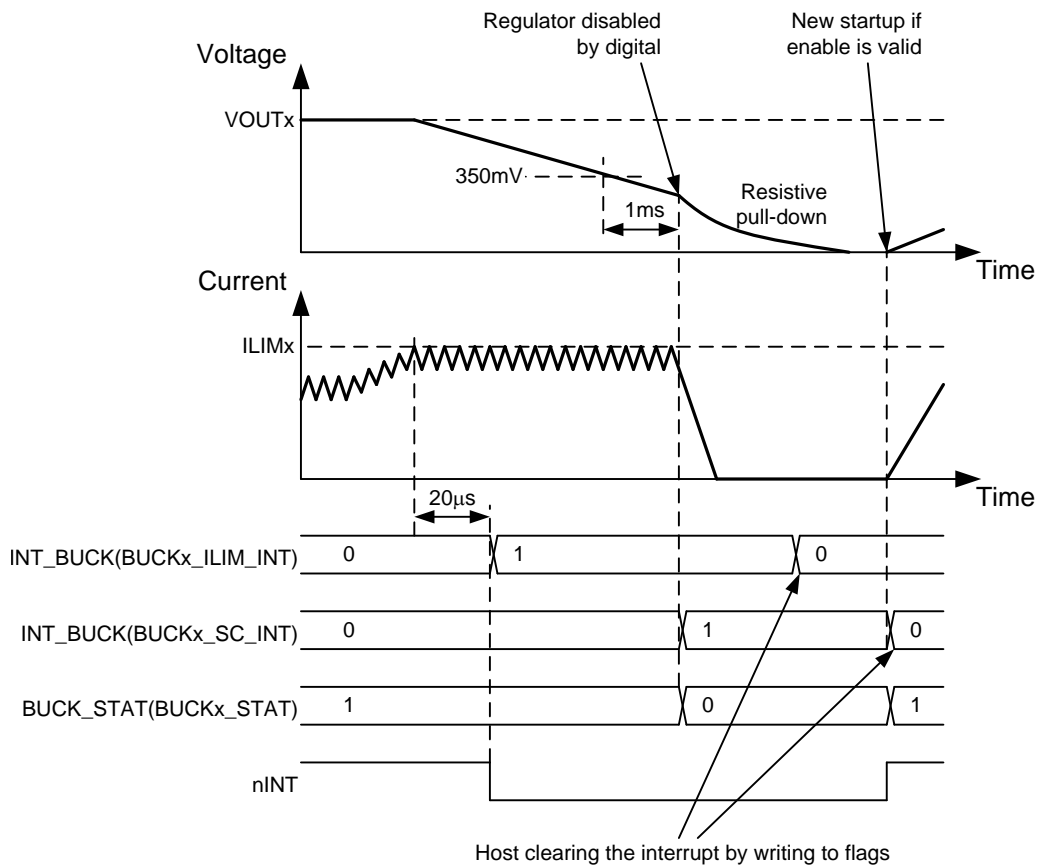


Figure 18. Buck Overload Situation

The boost converter has programmable output peak current limits. The limits are set with BOOST_ILIM bits. If the load current is increased so that the current limit is triggered, the converter continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 64 μ s, the LP87702-Q1 device sets the BOOST_ILIM_INT bit and pulls the nINT pin low. The host processor can read BOOST_ILIM_STAT bits to see if the converter is still in peak current regulation mode.

If the load is so high that the output voltage decreases 150mV (typical) below input voltage level converter is disabled after 1 ms. If the output voltage decreases to 2.5 V, boost is disabled immediately. Interrupt BOOST_SC_INT bit is set when boost is disabled. In addition the BOOST_SC_STAT bit is set to 0. The interrupt is cleared when the host processor writes 1 to BOOST_SC_INT bit. The Boost overload situation is shown in Figure 19.

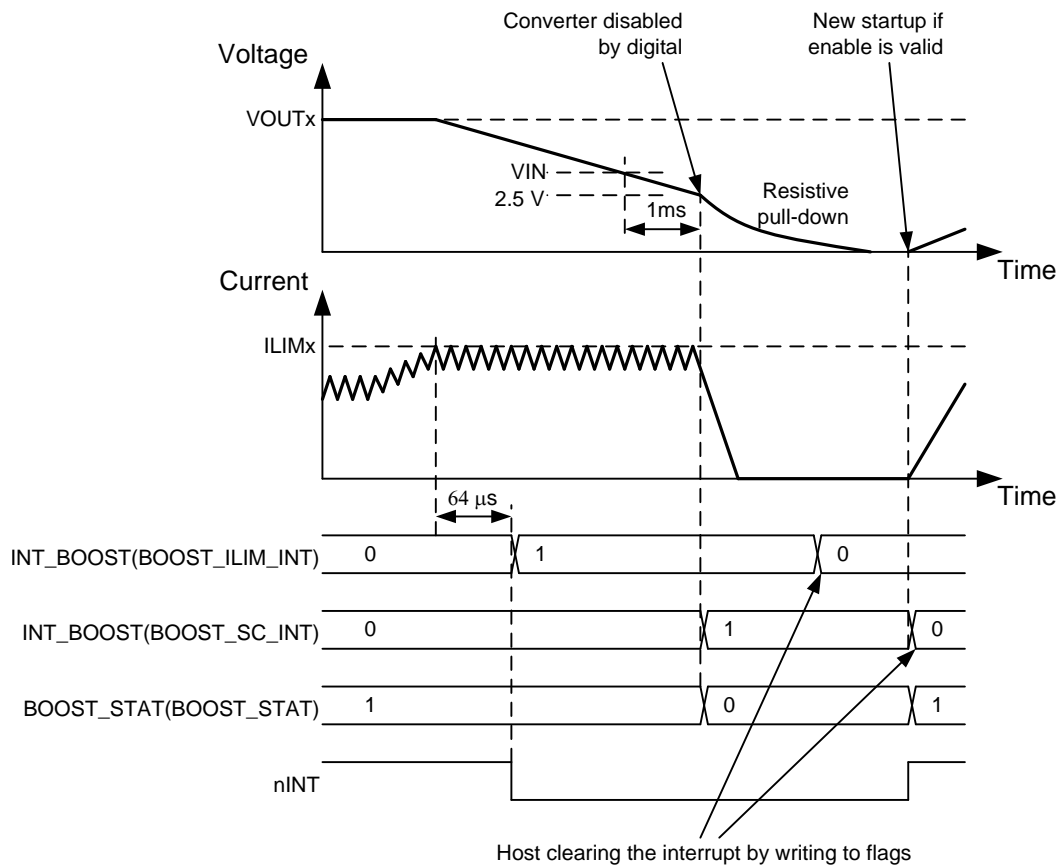


Figure 19. Boost Overload Situation

The buck converters have a fixed current limit for negative output peak current (I_{LIM_NEG}). When negative coil current increases it is limited below I_{LIM_NEG} , converter continues to operate and no interrupt is generated. Operation of the negative peak current limit of the boost converter is similar and limit value is 1.4 A (typical).

7.3.10.4.2 Thermal Warning

The LP87702-Q1 device includes a protection feature against over-temperature by setting an interrupt for host processor. The threshold level of the thermal warning is selected with TDIE_WARN_LEVEL bit.

If the LP87702-Q1 device temperature increases above thermal warning level the device sets TDIE_WARN_INT bit and pulls nINT pin low. The status of the thermal warning can be read from TDIE_WARN_STAT bit and the interrupt is cleared by writing 1 to TDIE_WARN_INT bit. The thermal warning interrupt can be masked by setting TDIE_WARN_MASK bit to 1.

7.3.10.5 Protections Causing Converter Disable

If the converter is disabled because of protection or fault (short-circuit protection, thermal shutdown, overvoltage protection, or undervoltage lockout), the output power FETs are set to high-impedance mode, and the output pulldown resistor is enabled (if enabled with BUCKx_RDIS_EN and BOOST_RDIS_EN bits). The turnoff time of the output voltage is defined by the output capacitance, load current, and the resistance of the integrated pulldown resistor. The pulldown resistors are active as long as VANA voltage is above approximately 1.2-V level.

7.3.10.5.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the LP87702-Q1 to protect itself and external components against short circuit at the output or against overload during start-up. During start-up, short-circuit at buck converter output is detected when the output voltage is below 350mV (typical) 1 ms after the buck converter is enabled. For boost the fault threshold is 150mV (typical) below input voltage level. Boost converter is disabled if the output voltage is below the threshold level 1 ms after the boost converter is enabled.

In a similar way the overload situation is protected during normal operation. If the feedback-pin voltage of the buck converter falls below 0.35 V and remains below the threshold level for 1 ms the buck converter is disabled. If the output voltage of the boost converter decreases 150 mV below input voltage level, converter is disabled after 1 ms. If the output voltage decreases to 2.5 V, boost is disabled immediately.

In the Buck converter short-circuit and overload situations the BUCKx_SC_INT and the BUCK_INT bits are set to 1, the BUCKx_STAT bit is set to 0 and the nINT signal is pulled low. In the boost converter short-circuit and overload situations the BOOST_SC_INT and the BOOST_INT bits are set to 1, the BOOST_STAT bit is set to 0 and the nINT signal is pulled low. The host processor clears the interrupt by writing 1 to the BUCKx_SC_INT or BOOST_SC_INT bit. Upon clearing the interrupt the converter makes a new start-up attempt if the converter is in enabled state.

7.3.10.5.2 Overvoltage Protection

The LP87702-Q1 device monitors the input voltage from VANA pin in standby and active operation modes. If the input voltage rises above $VANA_{OVP}$ voltage level, all the converters are disabled immediately (without switching ramp, no shutdown delays), pulldown resistors discharge the output voltages (BUCKx_RDIS_EN = 1 and BOOST_RDIS_EN = 1), GPOs are set to logic low level, nINT signal is pulled low, OVP_INT bit is set to 1 and BUCKx_STAT and BOOST_STAT bits are set to 0. The host processor clears the interrupt by writing 1 to the OVP_INT bit. If the input voltage is above over-voltage detection level the interrupt is not cleared. The host can read the status of the overvoltage from the OVP_STAT bit. Converters cannot be enabled as long as the input voltage is above over-voltage detection level or the overvoltage interrupt is pending.

7.3.10.5.3 Thermal Shutdown

The LP87702-Q1 has an overtemperature protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the converters are disabled immediately (without switching ramp, no shutdown delays), the TDIE_SD_INT bit is set to 1, the nINT signal is pulled low, and the device enters STANDBY. nINT is cleared by writing 1 to the TDIE_SD_INT bit. If the temperature is above thermal shutdown level the interrupt is not cleared. The host can read the status of the thermal shutdown from the TDIE_SD_STAT bit. Converters cannot be enabled as long as the junction temperature is above thermal shutdown level or the thermal shutdown interrupt is pending.

7.3.10.6 Protections Causing Device Power Down

7.3.10.6.1 Undervoltage Lockout

When the input voltage falls below $VANA_{UVLO}$ at the VANA pin, the buck and boost converters are disabled immediately (without switching ramp, no shutdown delays), and the output capacitor is discharged using the pulldown resistor, and the LP87702-Q1 device enters SHUTDOWN. When $V_{(VANA)}$ voltage is above $VANA_{UVLO}$ threshold level, the device powers up to STANDBY state.

If the reset interrupt is unmasked by default (RESET_REG_MASK = 0 in TOP_MASK_2 register) the RESET_REG_INT interrupt in INT_TOP_2 register indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the RESET_REG_INT bit. If the host processor reads the RESET_REG_INT flag after detecting an nINT low signal, it knows that the input supply voltage has been below $VANA_{UVLO}$ level (or the host has requested reset with RESET(SW_RESET) bit), and the registers are reset to default values.

7.3.11 OTP Error Correction

LP87702-Q1 supports OTP bit error detection and 1-bit error correction per five registers. ECC_STATUS register bit SED is set if a single bit error was detected and corrected. In case two bit errors have been detected in any bank of five registers, DED bit is set.

7.3.12 Operation of GPO Signals

The LP87702-Q1 device supports up to 3 general purpose output (GPO) signals. The GPO1 signal is multiplexed with PG1 signal and the GPO2 signal is multiplexed with CLKIN and WD_DIS signals. The selection between signal use are set with GPO1_SEL and GPO2_SEL bits in GPO_CONTROL_2 register.

The type of the output, either push-pull with $V_{(VANA)}$ level or open drain, are set with GPO0_OD and GPO1_PG1_OD bits in GPO_CONTROL_1 register and GPO2_OD bit in GPO_CONTROL_2 register

The logic level of the GPOx pins are is set by GPO0_OUT and GPO1_OUT bits in GPO_CONTROL_1 register and GPO2_OUT bit in GPO_CONTROL_2 register.

The control of the GPOs can be included to start-up and shutdown sequences. The GPO control for a sequence with ENx pin is selected by GPOx_EN_PIN_CTRL bits. The delays during start-up and shutdown are set by bits in GPOx_DELAY registers.

7.3.13 Digital Signal Filtering

The digital signals have a debounce filtering. The signal/supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

Table 7. Digital Signal Filtering

EVENT	SIGNAL/SUPPLY	RISING EDGE	FALLING EDGE
		LENGTH	LENGTH
Enable/Disable for BUCKx, BOOST or GPOx	ENx	3 μ s ⁽¹⁾	3 μ s ⁽¹⁾
VANA undervoltage lockout	VANA	Immediate (VANA voltage rising)	Immediate (VANA voltage falling)
VANA overvoltage	VANA	1 μ s (VANA voltage rising)	1 μ s (VANA voltage falling)
Thermal warning	TDIE_WARN_INT	20 μ s	20 μ s
Thermal shutdown	TDIE_SD_INT	20 μ s	20 μ s
Current limit, BUCKx		20 μ s	20 μ s
Current limit, BOOST		64 μ s	64 μ s
Overload	FB_B0, FB_B1, VOUT_BST	1 ms	N/V
PGx pin and power-good interrupt (voltage monitoring)	PG0, PG1 / FB_B0, FB_B1	6 μ s	6 μ s
PGx pin and power-good interrupt (voltage monitoring)	PG0, PG1 / VOUT_BST, VANA, VMON1, VMON2	15 μ s	15 μ s

(1) No glitch filtering, only synchronization.

7.4 Device Functional Modes

7.4.1 Modes of Operation

SHUTDOWN: The $V_{(VANA)}$ voltage is below $VANA_{UVLO}$ threshold level or NRST signal is low. All switch, reference, control and bias circuitry of the LP87702-Q1 device are turned off.

READ OTP: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level and NRST signal is high. The converters are disabled and the reference and bias circuitry of the LP87702-Q1 are enabled. The OTP bits are loaded to registers. I2C access is not allowed during OTP read. This applies also to watchdog (see [Window Watchdog](#)).

STANDBY: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level and NRST signal is high. All registers can be read or written by the host processor via the system serial interface. Watchdog is active and WDI input is expected to toggle to avoid watchdog expiration. The converters are disabled and the reference, control and bias circuitry of the LP87702-Q1 are enabled. The converters can be enabled if needed.

ACTIVE: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level and NRST signal is high. At least one converter is enabled. All registers can be read or written by the host processor via the system serial interface. Watchdog is active and WDI input is expected to toggle to avoid watchdog expiration.

The operating modes and transitions between the modes are shown in [Figure 20](#). For the window watchdog detailed operation see [Window Watchdog](#).

Device Functional Modes (continued)

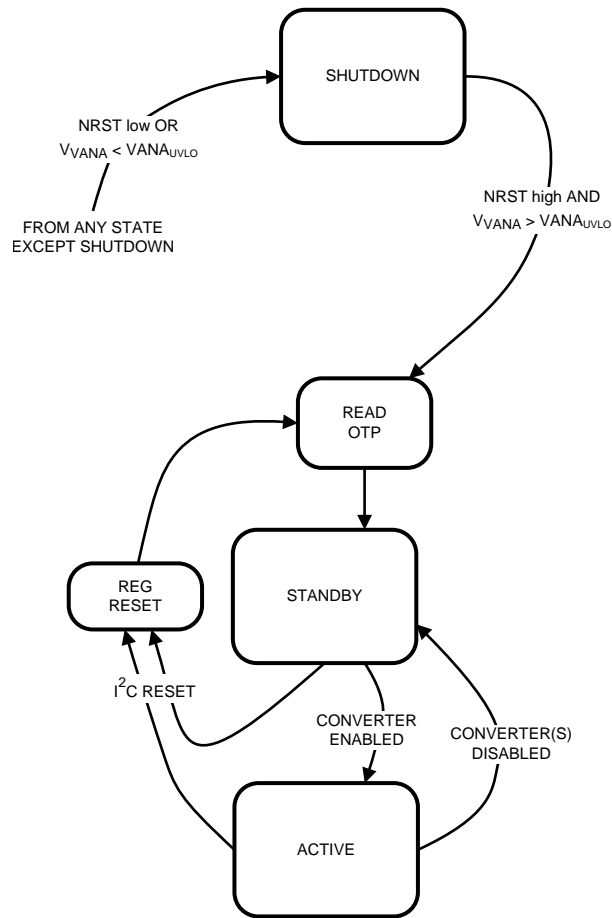


Figure 20. Device Operation Modes.

7.5 Programming

7.5.1 I²C-Compatible Interface

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the ICs connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pull-up resistor placed somewhere on the line and remain HIGH even when the bus is idle. The LP87702-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz).

7.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

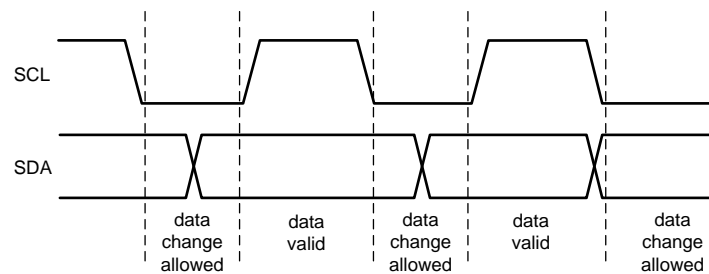


Figure 21. Data Validity Diagram

7.5.1.2 Start and Stop Conditions

The LP87702-Q1 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

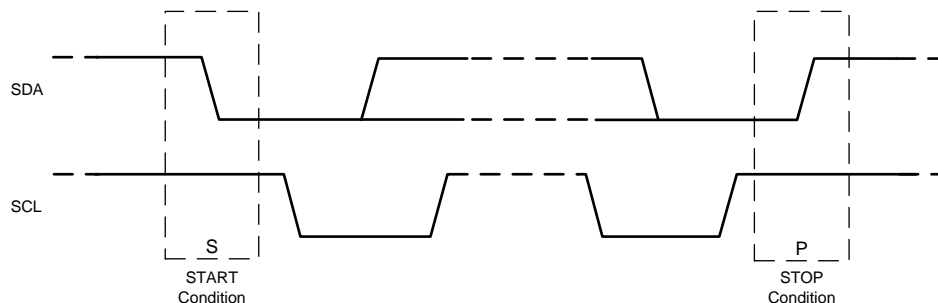
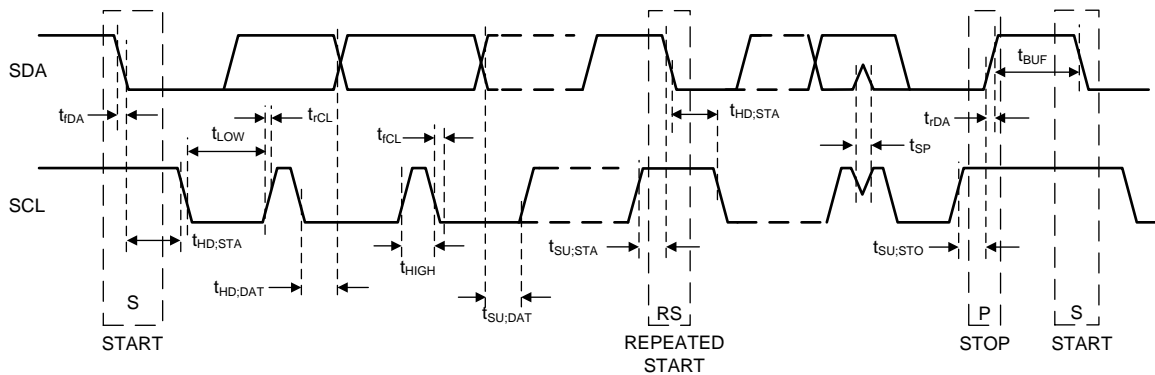


Figure 22. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. [Figure 23](#) shows the SDA and SCL signal timing for the I²C-Compatible Bus. See the [Figure 1](#) for timing values.

Programming (continued)

Figure 23. I²C-Compatible Timing
7.5.1.3 Transferring Data

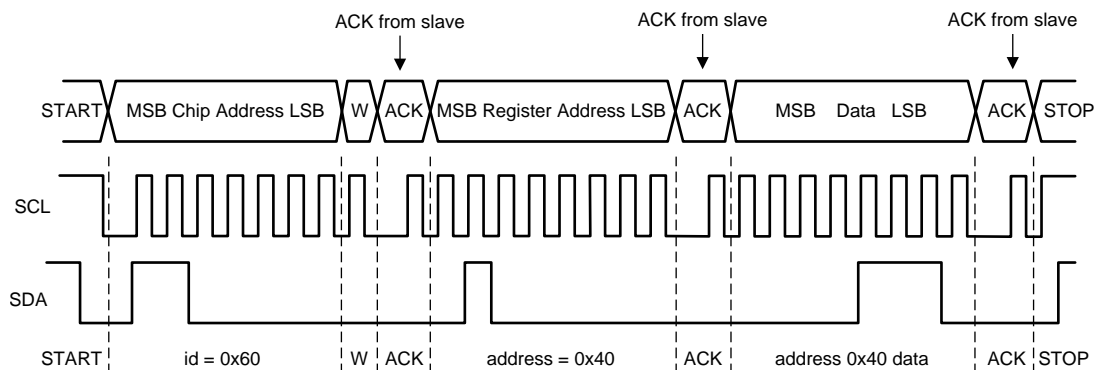
Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP87702-Q1 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP87702-Q1 generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

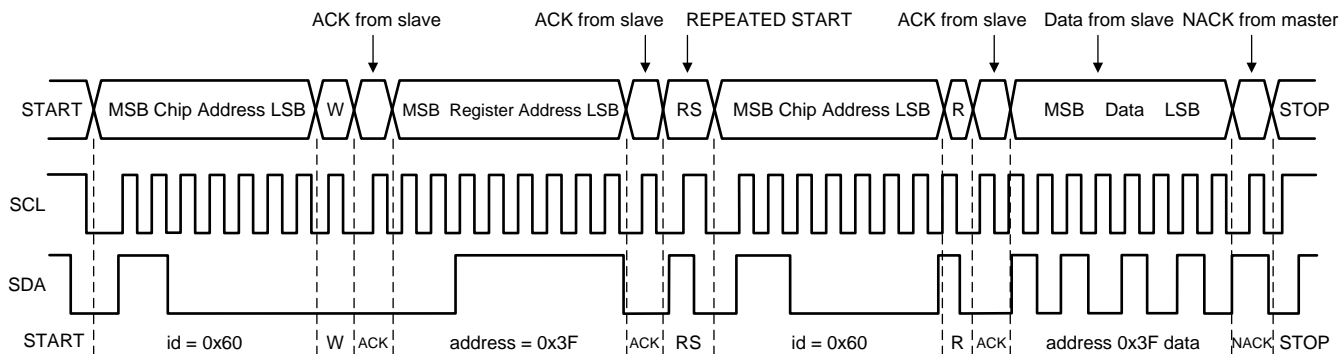
NOTE

If the $V_{(VANA)}$ voltage is below $VANA_{UVLO}$ threshold level during I²C communication the LP87702-Q1 device does not drive SDA line. The ACK signal and data transfer to the master is disabled at that time.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.


Figure 24. Write Cycle (w = write; SDA = 0), id = Device Address = 60Hex for LP87702-Q1

Programming (continued)

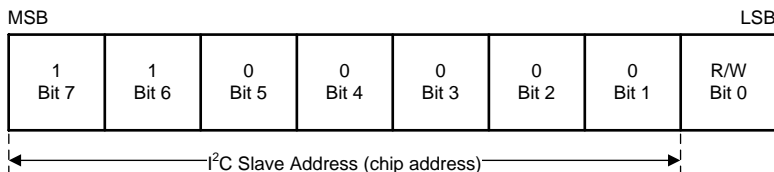


When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 25. Read Cycle (r = read; SDA = 1), id = Device Address = 60Hex for LP87702-Q1

7.5.1.4 I²C-Compatible Chip Address

The device address for the LP87702-Q1 is 0x60. After the START condition, the I²C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.



A. Here device address is 1100000Bin = 60Hex.

Figure 26. Device Address

7.5.1.5 Auto Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP87702-Q1, the internal address index counter will be incremented by one and the next register will be written. Table 8 below shows writing sequence to two consecutive registers. Note that auto increment feature does not work for read.

Table 8. Auto-Increment Example

MASTER ACTION	START	DEVICE ADDRESS S = 60H	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
LP87702-Q1				ACK		ACK		ACK		ACK	

7.6 Register Maps

7.6.1 Register Descriptions

The LP87702-Q1 is controlled by a set of registers through the system serial interface port. This register map describes the default values for bits which are not read from OTP memory. The asterisk (*) marking indicates register bits which are updated from OTP memory during READ OTP state. OTP values for each orderable part number are described in a separate technical reference manual TRM.

7.6.1.1 LP8770_map Registers

Table 9 lists the memory-mapped registers for the LP8770_map registers. All register offset addresses not listed in Table 9 should be considered as reserved locations and the register contents should not be modified.

Table 9. LP8770_MAP Registers

Offset	Acronym	Register Name	Section
0h	DEV_REV		DEV_REV Register (Offset = 0h) [reset = 0h]
1h	OTP_CODE		OTP_CODE Register (Offset = 1h) [reset = 0h]
2h	BUCK0_CTRL_1		BUCK0_CTRL_1 Register (Offset = 2h) [reset = 8h]
3h	BUCK0_CTRL_2		BUCK0_CTRL_2 Register (Offset = 3h) [reset = 1Ah]
4h	BUCK1_CTRL_1		BUCK1_CTRL_1 Register (Offset = 4h) [reset = 8h]
5h	BUCK1_CTRL_2		BUCK1_CTRL_2 Register (Offset = 5h) [reset = 1Ah]
6h	BUCK0_VOUT		BUCK0_VOUT Register (Offset = 6h) [reset = 0h]
7h	BUCK1_VOUT		BUCK1_VOUT Register (Offset = 7h) [reset = 0h]
8h	BOOST_CTRL		BOOST_CTRL Register (Offset = 8h) [reset = 8h]
9h	BUCK0_DELAY		BUCK0_DELAY Register (Offset = 9h) [reset = 0h]
Ah	BUCK1_DELAY		BUCK1_DELAY Register (Offset = Ah) [reset = 0h]
Bh	BOOST_DELAY		BOOST_DELAY Register (Offset = Bh) [reset = 0h]
Ch	GPO0_DELAY		GPO0_DELAY Register (Offset = Ch) [reset = 0h]
Dh	GPO1_DELAY		GPO1_DELAY Register (Offset = Dh) [reset = 0h]
Eh	GPO2_DELAY		GPO2_DELAY Register (Offset = Eh) [reset = 0h]
Fh	GPO_CONTROL_1		GPO_CONTROL_1 Register (Offset = Fh) [reset = AAh]
10h	GPO_CONTROL_2		GPO_CONTROL_2 Register (Offset = 10h) [reset = Ah]
11h	CONFIG		CONFIG Register (Offset = 11h) [reset = 3Ch]
12h	PLL_CTRL		PLL_CTRL Register (Offset = 12h) [reset = 2h]
13h	PGOOD_CTRL		PGOOD_CTRL Register (Offset = 13h) [reset = 0h]
14h	PGOOD_LEVEL_1		PGOOD_LEVEL_1 Register (Offset = 14h) [reset = 0h]

Table 9. LP8770_MAP Registers (continued)

Offset	Acronym	Register Name	Section
15h	PGOOD_LEVEL_2		PGOOD_LEVEL_2 Register (Offset = 15h) [reset = 0h]
16h	PGOOD_LEVEL_3		PGOOD_LEVEL_3 Register (Offset = 16h) [reset = 0h]
17h	PG_CTRL		PG_CTRL Register (Offset = 17h) [reset = 2h]
18h	PG0_CTRL		PG0_CTRL Register (Offset = 18h) [reset = 0h]
19h	PG0_FAULT		PG0_FAULT Register (Offset = 19h) [reset = 0h]
1Ah	PG1_CTRL		PG1_CTRL Register (Offset = 1Ah) [reset = 0h]
1Bh	PG1_FAULT		PG1_FAULT Register (Offset = 1Bh) [reset = 0h]
1Ch	WD_CTRL_1		WD_CTRL_1 Register (Offset = 1Ch) [reset = 0h]
1Dh	WD_CTRL_2		WD_CTRL_2 Register (Offset = 1Dh) [reset = 1h]
1Eh	WD_STATUS		WD_STATUS Register (Offset = 1Eh) [reset = 0h]
1Fh	RESET		RESET Register (Offset = 1Fh) [reset = 0h]
20h	INT_TOP_1		INT_TOP_1 Register (Offset = 20h) [reset = 0h]
21h	INT_TOP_2		INT_TOP_2 Register (Offset = 21h) [reset = 0h]
22h	INT_BUCK		INT_BUCK Register (Offset = 22h) [reset = 0h]
23h	INT_BOOST		INT_BOOST Register (Offset = 23h) [reset = 0h]
24h	INT_DIAG		INT_DIAG Register (Offset = 24h) [reset = 0h]
25h	TOP_STATUS		TOP_STATUS Register (Offset = 25h) [reset = 0h]
26h	BUCK_STATUS		BUCK_STATUS Register (Offset = 26h) [reset = 0h]
27h	BOOST_STATUS		BOOST_STATUS Register (Offset = 27h) [reset = 0h]
28h	DIAG_STATUS		DIAG_STATUS Register (Offset = 28h) [reset = 0h]
29h	TOP_MASK_1		TOP_MASK_1 Register (Offset = 29h) [reset = 0h]
2Ah	TOP_MASK_2		TOP_MASK_2 Register (Offset = 2Ah) [reset = 1h]
2Bh	BUCK_MASK		BUCK_MASK Register (Offset = 2Bh) [reset = 0h]
2Ch	BOOST_MASK		BOOST_MASK Register (Offset = 2Ch) [reset = 0h]
2Dh	DIAG_MASK		DIAG_MASK Register (Offset = 2Dh) [reset = 0h]
2Eh	SEL_I_LOAD		SEL_I_LOAD Register (Offset = 2Eh) [reset = 0h]
2Fh	I_LOAD_2		I_LOAD_2 Register (Offset = 2Fh) [reset = 0h]
30h	I_LOAD_1		I_LOAD_1 Register (Offset = 30h) [reset = 0h]

Table 9. LP8770_MAP Registers (continued)

Offset	Acronym	Register Name	Section
31h	FREQ_SEL		FREQ_SEL Register (Offset = 31h) [reset = 0h]
32h	BOOST_ILIM_CTRL		BOOST_ILIM_CTRL Register (Offset = 32h) [reset = 0h]
33h	ECC_STATUS		ECC_STATUS Register (Offset = 33h) [reset = 0h]
34h	WD_DIS_CTRL_CODE		WD_DIS_CTRL_CODE Register (Offset = 34h) [reset = 0h]
35h	WD_DIS_CONTROL		WD_DIS_CONTROL Register (Offset = 35h) [reset = 0h]

Complex bit access types are encoded to fit into small table cells. [Table 10](#) shows the codes that are used for access types in this section.

Table 10. LP8770_map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

7.6.1.1.1 DEV_REV Register (Offset = 0h) [reset = 0h]

DEV_REV is shown in [Figure 27](#) and described in [Table 11](#).

Return to [Summary Table](#).

Figure 27. DEV_REV Register

7	6	5	4	3	2	1	0
RESERVED		DEVICE_ID			RESERVED		
R-0h		R-0h			R-0h		

Table 11. DEV_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-3	DEVICE_ID	R	0h	Device specific ID code. (Default from OTP memory)

Table 11. DEV_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	RESERVED	R	0h	Reserved

7.6.1.1.2 OTP_CODE Register (Offset = 1h) [reset = 0h]

OTP_CODE is shown in [Figure 28](#) and described in [Table 12](#).

Return to [Summary Table](#).

Figure 28. OTP_CODE Register

7	6	5	4	3	2	1	0
OTP_ID						OTP_REV	
R-0h						R-0h	

Table 12. OTP_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	OTP_ID	R	0h	Identification Code of the OTP EPROM. (Default from OTP memory)
1-0	OTP_REV	R	0h	Version number of the OTP ID. (Default from OTP memory)

7.6.1.1.3 BUCK0_CTRL_1 Register (Offset = 2h) [reset = 8h]

BUCK0_CTRL_1 is shown in [Figure 29](#) and described in [Table 13](#).

Return to [Summary Table](#).

Figure 29. BUCK0_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED	BUCK0_FPWM	BUCK0_RDIS_EN	BUCK0_EN_PIN_CTRL		BUCK0_EN
R/W-0h		R-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h

Table 13. BUCK0_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	RESERVED	R	0h	Reserved
4	BUCK0_FPWM	R/W	0h	Forces the BUCK0 converter to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation. (Default from OTP memory)
3	BUCK0_RDIS_EN	R/W	1h	Enable output discharge resistor when BUCK0 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.
2-1	BUCK0_EN_PIN_CTRL	R/W	0h	Enable/disable control for BUCK0: 0x0 - only BUCK0_EN bit controls BUCK0 0x1 - BUCK0_EN bit AND EN1 pin control BUCK0 0x2 - BUCK0_EN bit AND EN2 pin control BUCK0 0x3 - BUCK0_EN bit AND EN3 pin control BUCK0 (Default from OTP memory)

Table 13. BUCK0_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BUCK0_EN	R/W	0h	Enable BUCK0 converter: 0 - BUCK0 converter is disabled 1 - BUCK0 converter is enabled. (Default from OTP memory)

7.6.1.1.4 BUCK0_CTRL_2 Register (Offset = 3h) [reset = 1Ah]

BUCK0_CTRL_2 is shown in [Figure 30](#) and described in [Table 14](#).

Return to [Summary Table](#).

Figure 30. BUCK0_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK0_ILIM			BUCK0_SLEW_RATE		
R/W-0h		R/W-3h			R/W-2h		

Table 14. BUCK0_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK0_ILIM	R/W	3h	Sets the switch peak current limit of BUCK0. Can be programmed at any time during operation: 0x0 - 1.5 A 0x1 - 2.0 A 0x2 - 2.5 A 0x3 - 3.0 A 0x4 - 3.5 A 0x5 - 4.0 A 0x6 - 4.5 A 0x7 - Reserved (Default from OTP memory)
2-0	BUCK0_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK0 converter (rising and falling edges): 0x0 - Reserved 0x1 - Reserved 0x2 - 10 mV/μs 0x3 - 7.5 mV/μs 0x4 - 3.8 mV/μs 0x5 - 1.9 mV/μs 0x6 - 0.94 mV/μs 0x7 - 0.47 mV/μs (Default from OTP memory)

7.6.1.1.5 BUCK1_CTRL_1 Register (Offset = 4h) [reset = 8h]

BUCK1_CTRL_1 is shown in [Figure 31](#) and described in [Table 15](#).

Return to [Summary Table](#).

Figure 31. BUCK1_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK1_FPWM	BUCK1_RDIS_EN	BUCK1_EN_PIN_CTRL		BUCK1_EN
R/W-0h			R/W-0h	R/W-1h	R/W-0h		R/W-0h

Table 15. BUCK1_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	BUCK1_FPWM	R/W	0h	Forces the BUCK1 converter to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation. (Default from OTP memory)
3	BUCK1_RDIS_EN	R/W	1h	Enable output discharge resistor when BUCK1 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.
2-1	BUCK1_EN_PIN_CTRL	R/W	0h	Enable/disable control for BUCK1: 0x0 - only BUCK1_EN bit controls BUCK1 0x1 - BUCK1_EN bit AND EN1 pin control BUCK1 0x2 - BUCK1_EN bit AND EN2 pin control BUCK1 0x3 - BUCK1_EN bit AND EN3 pin control BUCK1 (Default from OTP memory)
0	BUCK1_EN	R/W	0h	Enable BUCK1 converter: 0 - BUCK1 converter is disabled 1 - BUCK1 converter is enabled. (Default from OTP memory)

7.6.1.1.6 BUCK1_CTRL_2 Register (Offset = 5h) [reset = 1Ah]

BUCK1_CTRL_2 is shown in [Figure 32](#) and described in [Table 16](#).

Return to [Summary Table](#).

Figure 32. BUCK1_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_ILIM			BUCK1_SLEW_RATE		
R/W-0h		R/W-3h			R/W-2h		

Table 16. BUCK1_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK1_ILIM	R/W	3h	Sets the switch peak current limit of BUCK1. Can be programmed at any time during operation: 0x0 - 1.5 A 0x1 - 2.0 A 0x2 - 2.5 A 0x3 - 3.0 A 0x4 - 3.5 A 0x5 - 4.0 A 0x6 - 4.5 A 0x7 - Reserved (Default from OTP memory)
2-0	BUCK1_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK1 converter (rising and falling edges): 0x0 - Reserved 0x1 - Reserved 0x2 - 10 mV/μs 0x3 - 7.5 mV/μs 0x4 - 3.8 mV/μs 0x5 - 1.9 mV/μs 0x6 - 0.94 mV/μs 0x7 - 0.47 mV/μs (Default from OTP memory)

7.6.1.1.7 BUCK0_VOUT Register (Offset = 6h) [reset = 0h]

BUCK0_VOUT is shown in [Figure 33](#) and described in [Table 17](#).

Return to [Summary Table](#).

Figure 33. BUCK0_VOUT Register

7	6	5	4	3	2	1	0
BUCK0_VSET							
R/W-0h							

Table 17. BUCK0_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK0_VSET	R/W	0h	Output voltage of BUCK0 converter: 0x00 ... 0x13, Reserved, DO NOT USE 0.7 V - 0.73 V, 10 mV steps 0x14 - 0.7V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V (Default from OTP memory)

7.6.1.1.8 BUCK1_VOUT Register (Offset = 7h) [reset = 0h]

BUCK1_VOUT is shown in [Figure 34](#) and described in [Table 18](#).

Return to [Summary Table](#).

Figure 34. BUCK1_VOUT Register

7	6	5	4	3	2	1	0
BUCK1_VSET							
R/W-0h							

Table 18. BUCK1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK1_VSET	R/W	0h	Output voltage of BUCK1 converter 0x00 ... 0x13, Reserved, DO NOT USE 0.7 V - 0.73 V, 10 mV steps 0x14 - 0.7V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V (Default from OTP memory)

7.6.1.1.9 BOOST_CTRL Register (Offset = 8h) [reset = 8h]

 BOOST_CTRL is shown in [Figure 35](#) and described in [Table 19](#).

 Return to [Summary Table](#).

Figure 35. BOOST_CTRL Register

7	6	5	4	3	2	1	0
BOOST_VSET		RESERVED	BOOST_FPWM	BOOST_RDIS_EN	BOOST_EN_PIN_CTRL		BOOST_EN
R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h

Table 19. BOOST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BOOST_VSET	R/W	0h	Output voltage of Boost: 0x0 - 4.9V 0x1 - 5.0V 0x2 - 5.1V 0x3 - 5.2V (Default from OTP memory)
5	RESERVED	R/W	0h	
4	RESERVED	R/W	1h	
3	BOOST_RDIS_EN	R/W	1h	Enable output discharge resistor when BOOST is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.
2-1	BOOST_EN_PIN_CTRL	R/W	0h	Enable/disable control for Boost: 0x0 - only BOOST_EN bit controls Boost 0x1 - BOOST_EN bit AND EN1 pin control Boost 0x2 - BOOST_EN bit AND EN2 pin control Boost 0x3 - BOOST_EN bit AND EN3 pin control Boost (Default from OTP memory)
0	BOOST_EN	R/W	0h	Enable Boost converter: 0 - Boost converter is disabled 1 - Boost converter is enabled. (Default from OTP memory)

7.6.1.1.10 BUCK0_DELAY Register (Offset = 9h) [reset = 0h]

 BUCK0_DELAY is shown in [Figure 36](#) and described in [Table 20](#).

 Return to [Summary Table](#).

Figure 36. BUCK0_DELAY Register

7	6	5	4	3	2	1	0
BUCK0_SHUTDOWN_DELAY				BUCK0_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 20. BUCK0_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK0_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of BUCK0 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

Table 20. BUCK0_DELAY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	BUCK0_STARTUP_DELAY	R/W	0h	Startup delay of BUCK0 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.11 BUCK1_DELAY Register (Offset = Ah) [reset = 0h]

BUCK1_DELAY is shown in [Figure 37](#) and described in [Table 21](#).

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Figure 37. BUCK1_DELAY Register

7	6	5	4	3	2	1	0
BUCK1_SHUTDOWN_DELAY				BUCK1_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 21. BUCK1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK1_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of BUCK1 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BUCK1_STARTUP_DELAY	R/W	0h	Startup delay of BUCK1 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.12 BOOST_DELAY Register (Offset = Bh) [reset = 0h]

BOOST_DELAY is shown in [Figure 38](#) and described in [Table 22](#).

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Figure 38. BOOST_DELAY Register

7	6	5	4	3	2	1	0
BOOST_SHUTDOWN_DELAY				BOOST_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 22. BOOST_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BOOST_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of Boost from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

Table 22. BOOST_DELAY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	BOOST_STARTUP_DELAY	R/W	0h	Startup delay of Boost from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.13 GPO0_DELAY Register (Offset = Ch) [reset = 0h]

GPO0_DELAY is shown in [Figure 39](#) and described in [Table 23](#).

Return to [Summary Table](#).

Figure 39. GPO0_DELAY Register

7	6	5	4	3	2	1	0
GPO0_SHUTDOWN_DELAY				GPO0_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 23. GPO0_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO0_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO0 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO0_STARTUP_DELAY	R/W	0h	Startup delay of GPO0 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.14 GPO1_DELAY Register (Offset = Dh) [reset = 0h]

GPO1_DELAY is shown in [Figure 40](#) and described in [Table 24](#).

Return to [Summary Table](#).

Figure 40. GPO1_DELAY Register

7	6	5	4	3	2	1	0
GPO1_SHUTDOWN_DELAY				GPO1_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 24. GPO1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO1_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO1 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

Table 24. GPO1_DELAY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	GPO1_STARTUP_DELAY	R/W	0h	Startup delay of GPO1 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.15 GPO2_DELAY Register (Offset = Eh) [reset = 0h]

GPO2_DELAY is shown in [Figure 41](#) and described in [Table 25](#).

Return to [Summary Table](#).

Figure 41. GPO2_DELAY Register

7	6	5	4	3	2	1	0
GPO2_SHUTDOWN_DELAY				GPO2_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 25. GPO2_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO2_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO2 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO2_STARTUP_DELAY	R/W	0h	Startup delay of GPO2 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.16 GPO_CONTROL_1 Register (Offset = Fh) [reset = AAh]

GPO_CONTROL_1 is shown in [Figure 42](#) and described in [Table 26](#).

Return to [Summary Table](#).

Figure 42. GPO_CONTROL_1 Register

7	6	5	4	3	2	1	0
GPO1_PG1_OD	GPO1_EN_PIN_CTRL		GPO1_OUT	GPO0_OD	GPO0_EN_PIN_CTRL		GPO0_OUT
R/W-1h	R/W-1h		R/W-0h	R/W-1h	R/W-1h		R/W-0h

Table 26. GPO_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPO1_PG1_OD	R/W	1h	GPO1 / PG1 signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)

Table 26. GPO_CONTROL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	GPO1_EN_PIN_CTRL	R/W	1h	Control for GPO1 output: 0x0 - only GPO1_OUT bit controls GPO1 0x1 - GPO1_OUT bit AND EN1 pin control GPO1 0x2 - GPO1_OUT bit AND EN2 pin control GPO1 0x3 - GPO1_OUT bit AND EN3 pin control GPO1 (Default from OTP memory)
4	GPO1_OUT	R/W	0h	Control for GPO1 signal (when configured to GPO1): 0 - Logic low level 1 - Logic high level (Default from OTP memory)
3	GPO0_OD	R/W	1h	GPO0 signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)
2-1	GPO0_EN_PIN_CTRL	R/W	1h	Control for GPO0 output: 0x0 - only GPO0_OUT bit controls GPO0 0x1 - GPO0_OUT bit AND EN1 pin control GPO0 0x2 - GPO0_OUT bit AND EN2 pin control GPO0 0x3 - GPO0_OUT bit AND EN3 pin control GPO0 (Default from OTP memory)
0	GPO0_OUT	R/W	0h	Control for GPO0 signal: 0 - Logic low level 1 - Logic high level (Default from OTP memory)

7.6.1.1.17 GPO_CONTROL_2 Register (Offset = 10h) [reset = Ah]

GPO_CONTROL_2 is shown in [Figure 43](#) and described in [Table 27](#).

Return to [Summary Table](#).

Figure 43. GPO_CONTROL_2 Register

7	6	5	4	3	2	1	0
RESERVED	GPO2_SEL	GPO1_SEL	GPO2_OD	GPO2_EN_PIN_CTRL	GPO2_OUT		
R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h		

Table 27. GPO_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	GPO2_SEL	R/W	0h	CLKIN/GPO2 pin function: 0 - CLKIN 1 - GPO2 (Default from OTP memory)
4	GPO1_SEL	R/W	0h	PG1/GPO1 pin function: 0 - PG1 1 - GPO1 (Default from OTP memory)
3	GPO2_OD	R/W	1h	GPO2 signal type (when configured to GPO2): 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)

Table 27. GPO_CONTROL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	GPO2_EN_PIN_CTRL	R/W	1h	Control for GPO2 output: 0x0 - only GPO2_OUT bit controls GPO2 0x1 - GPO2_OUT bit AND EN1 pin control GPO2 0x2 - GPO2_OUT bit AND EN2 pin control GPO2 0x3 - GPO2_OUT bit AND EN3 pin control GPO2 (Default from OTP memory)
0	GPO2_OUT	R/W	0h	Control for GPO2 signal (when configured to GPO2): 0 - Logic low level 1 - Logic high level (Default from OTP memory)

7.6.1.1.18 CONFIG Register (Offset = 11h) [reset = 3Ch]

 CONFIG is shown in [Figure 44](#) and described in [Table 28](#).

 Return to [Summary Table](#).

Figure 44. CONFIG Register

7	6	5	4	3	2	1	0
STARTUP_DELAY_SEL	SHUTDOWN_DELAY_SEL	CLKIN_PD	EN3_PD	EN2_PD	EN1_PD	TDIE_WARN_LVL	EN_SPREAD_SPEC
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

Table 28. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STARTUP_DELAY_SEL	R/W	0h	Startup delays from control signal: 0 - 0ms - 7.5ms with 0.5ms steps 1 - 0ms - 15ms with 1ms steps (Default from OTP memory)
6	SHUTDOWN_DELAY_SEL	R/W	0h	Shutdown delays from from signal: 0 - 0ms - 7.5ms with 0.5ms steps 1 - 0ms - 15ms with 1ms steps (Default from OTP memory)
5	CLKIN_PD	R/W	1h	Selects the pull down resistor on the CLKIN input pin. 0 - Pull-down resistor is disabled. 1 - Pull-down resistor is enabled. (Default from OTP memory)
4	EN3_PD	R/W	1h	Selects the pull down resistor on the EN3 pin: 0 - Pull-down resistor is disabled 1 - Pull-down resistor is enabled (Default from OTP memory)
3	EN2_PD	R/W	1h	Selects the pull down resistor on the EN2 pin: 0 - Pull-down resistor is disabled 1 - Pull-down resistor is enabled (Default from OTP memory)
2	EN1_PD	R/W	1h	Selects the pull down resistor on the EN1 pin: 0 - Pull-down resistor is disabled 1 - Pull-down resistor is enabled (Default from OTP memory)
1	TDIE_WARN_LEVEL	R/W	0h	Thermal warning threshold level. 0 - 125C 1 - 140C. (Default from OTP memory)

Table 28. CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN_SPREAD_SPEC	R/W	0h	Enable spread spectrum feature for Buck and Boost converters. 0 - Disabled 1 - Enabled (Default from OTP memory)

7.6.1.1.19 PLL_CTRL Register (Offset = 12h) [reset = 2h]

PLL_CTRL is shown in [Figure 45](#) and described in [Table 29](#).

Return to [Summary Table](#).

Figure 45. PLL_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	EN_PLL	EN_FRAC_DIV	EXT_CLK_FREQ				
R/W-0h	R/W-0h	R/W-0h	R/W-2h				

Table 29. PLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	EN_PLL	R/W	0h	Selection of external clock and PLL operation: 0 - Forced to internal RC oscillator. PLL disabled. 1 - PLL is enabled in STANDBY and ACTIVE modes. Automatic external clock use when available, interrupt generated if external clock appears or disappears. (Default from OTP memory)
5	EN_FRAC_DIV	R/W	0h	This bit must be set to '0'.
4-0	EXT_CLK_FREQ	R/W	2h	Frequency of the external clock (CLKIN): 0x00 - 1 MHz 0x01 - 2 MHz 0x02 - 3 MHz ... 0x16 - 23 MHz 0x17 - 24 MHz 0x18...0x1F - Reserved See electrical specification for input clock frequency tolerance. (Default from OTP memory) Note: To ensure proper operation of PLL, EXT_CLK_FREQ value must not be changed when PLL is enabled.

7.6.1.1.20 PGOOD_CTRL Register (Offset = 13h) [reset = 0h]

PGOOD_CTRL is shown in [Figure 46](#) and described in [Table 30](#).

Return to [Summary Table](#).

Figure 46. PGOOD_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	PGOOD_WIND OW	EN_PGOOD_V ANA	EN_PGOOD_V MON2	EN_PGOOD_V MON1	EN_PGOOD_B OOST	EN_PGOOD_B UCK1	EN_PGOOD_B UCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 30. PGOOD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	PGOOD_WINDOW	R/W	0h	Voltage monitoring method for PG0 and PG1 signals: 0 - Only undervoltage monitoring. 1 - Overvoltage and undervoltage monitoring. (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
5	EN_PGOOD_VANA	R/W	0h	Enable powergood diagnostics for VANA 0 - Disabled 1 - Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
4	EN_PGOOD_VMON2	R/W	0h	Enable powergood diagnostics for VMON2 0 - Disabled 1 - Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
3	EN_PGOOD_VMON1	R/W	0h	Enable powergood diagnostics for VMON1 0 - Disabled 1 - Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
2	EN_PGOOD_BOOST	R/W	0h	Enable powergood diagnostics for Boost 0 - Disabled 1 - Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
1	EN_PGOOD_BUCK1	R/W	0h	Enable powergood diagnostics for Buck1 0 - Disabled 1 - Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
0	EN_PGOOD_BUCK0	R/W	0h	Enable powergood diagnostics for Buck0 0 - Disabled 1 - Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.

7.6.1.1.21 PGOOD_LEVEL_1 Register (Offset = 14h) [reset = 0h]

PGOOD_LEVEL_1 is shown in [Figure 47](#) and described in [Table 31](#).

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Figure 47. PGOOD_LEVEL_1 Register

7	6	5	4	3	2	1	0
RESERVED			VMON1_WINDOW		VMON1_THRESHOLD		
R/W-0h			R/W-0h		R/W-0h		

Table 31. PGOOD_LEVEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	VMON1_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VMON1: 0x0 - +/-2% 0x1 - +/-3% 0x2 - +/-4% 0x3 - +/-6% (Default from OTP memory)
2-0	VMON1_THRESHOLD	R/W	0h	Threshold voltage for VMON1 input: 0x0 - 0.65V (high impedance input, external resistive divider can be used) 0x1 - 0.80V 0x2 - 1.00V 0x3 - 1.10V 0x4 - 1.20V 0x5 - 1.30V 0x6 - 1.80V 0x7 - 1.80V To monitor any other voltage level, select 0x0 and use an external resistive divider to scale down to 0.65V. For other than 0x0 VMONx input is low impedance (internal resistive divider enabled). (Default from OTP memory)

7.6.1.1.22 PGOOD_LEVEL_2 Register (Offset = 15h) [reset = 0h]

PGOOD_LEVEL_2 is shown in [Figure 48](#) and described in [Table 32](#).

Return to [Summary Table](#).

Figure 48. PGOOD_LEVEL_2 Register

7	6	5	4	3	2	1	0
VANA_WINDOW		VANA_THRES HOLD	VMON2_WINDOW		VMON2_THRESHOLD		
R/W-0h		R/W-0h	R/W-0h		R/W-0h		

Table 32. PGOOD_LEVEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VANA_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VANA: 0x0 - +/-4% 0x1 - +/-5% 0x2 - +/-10% 0x3 - +/-10% (Default from OTP memory)
5	VANA_THRESHOLD	R/W	0h	Threshold voltage for VANA input: 0 - 3.3V 1 - 5.0V (Default from OTP memory)
4-3	VMON2_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VMON2: 0x0 - +/-2% 0x1 - +/-3% 0x2 - +/-4% 0x3 - +/-6% (Default from OTP memory)

Table 32. PGOOD_LEVEL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	VMON2_THRESHOLD	R/W	0h	Threshold voltage for VMON2 input: 0x0 - 0.65V (high impedance input, external resistive divider can be used) 0x1 - 0.80V 0x2 - 1.00V 0x3 - 1.10V 0x4 - 1.20V 0x5 - 1.30V 0x6 - 1.80V 0x7 - 1.80V To monitor any other voltage level, select 0x0 and use an external resistive divider to scale down to 0.65V. For other than 0x0 VMONx input is low impedance (internal resistive divider enabled). (Default from OTP memory)

7.6.1.1.23 PGOOD_LEVEL_3 Register (Offset = 16h) [reset = 0h]

PGOOD_LEVEL_3 is shown in [Figure 49](#) and described in [Table 33](#).

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Figure 49. PGOOD_LEVEL_3 Register

7	6	5	4	3	2	1	0
BOOST_WINDOW		BOOST_THRESHOLD		BUCK1_WINDOW		BUCK0_WINDOW	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 33. PGOOD_LEVEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BOOST_WINDOW	R/W	0h	Undervoltage/overvoltage threshold levels for Boost: 0x0 - +/-2% 0x1 - +/-4% 0x2 - +/-6% 0x3 - +/-8% (Default from OTP memory)
5-4	BOOST_THRESHOLD	R/W	0h	(Default from OTP memory)
3-2	BUCK1_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for Buck1: 0x0 - +/-30 mV 0x1 - +/-50 mV 0x2 - +/-70 mV 0x3 - +/-90 mV (Default from OTP memory)
1-0	BUCK0_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for Buck0: 0x0 - +/-30 mV 0x1 - +/-50 mV 0x2 - +/-70 mV 0x3 - +/-90 mV (Default from OTP memory)

7.6.1.1.24 PG_CTRL Register (Offset = 17h) [reset = 2h]

PG_CTRL is shown in [Figure 50](#) and described in [Table 34](#).

Return to [Summary Table](#).

Figure 50. PG_CTRL Register

7	6	5	4	3	2	1	0
PG1_MODE	PGOOD_FAULT_GATES_PG1	RESERVED	PG1_POL	PG0_MODE	PGOOD_FAULT_GATES_PG0	PG0_OD	PG0_POL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

Table 34. PG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG1_MODE	R/W	0h	Operating mode for PG1 signal: 0 - Detecting unusual situations 1 - Showing when requested outputs are not valid. (Default from OTP memory)
6	PGOOD_FAULT_GATES_PG1	R/W	0h	Type of operation for PG1 signal: 0 - Indicates live status of monitored voltage outputs. 1 - Indicates status of PG1_FAULT register, inactive if at least one of PG1_FAULT_x bit is inactive. (Default from OTP memory)
5	RESERVED	R/W	0h	
4	PG1_POL	R/W	0h	PG1 signal polarity. 0 - PG1 signal high when monitored outputs are valid 1 - PG1 signal low when monitored outputs are valid (Default from OTP memory)
3	PG0_MODE	R/W	0h	Operating mode for PG0 signal: 0 - Detecting unusual situations 1 - Showing when requested outputs are not valid. (Default from OTP memory)
2	PGOOD_FAULT_GATES_PG0	R/W	0h	Type of operation for PG0 signal: 0 - Indicates live status of monitored voltage outputs. 1 - Indicates status of PG0_FAULT register, inactive if at least one of PG0_FAULT_x bit is inactive. (Default from OTP memory)
1	PG0_OD	R/W	1h	PG0 signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)
0	PG0_POL	R/W	0h	PG0 signal polarity. 0 - PG0 signal high when monitored outputs are valid 1 - PG0 signal low when monitored outputs are valid (Default from OTP memory)

7.6.1.1.25 PG0_CTRL Register (Offset = 18h) [reset = 0h]

PG0_CTRL is shown in [Figure 51](#) and described in [Table 35](#).

Return to [Summary Table](#).

Figure 51. PG0_CTRL Register

7	6	5	4	3	2	1	0
PG0_RISE_DE_LAY	SEL_PG0_TWARN	SEL_PG0_VANA	SEL_PG0_VM_ON2	SEL_PG0_VM_ON1	SEL_PG0_BOOST	SEL_PG0_BUCK1	SEL_PG0_BUCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 35. PG0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG0_RISE_DELAY	R/W	0h	0 - PG0 rise is not delayed 1 - PG0 rise is delayed 11ms
6	SEL_PG0_TWARN	R/W	0h	PG0 control from thermal warning: 0 - Masked 1 - Affecting PGOOD (Default from OTP memory)
5	SEL_PG0_VANA	R/W	0h	PG0 signal source control from VANA 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
4	SEL_PG0_VMON2	R/W	0h	PG0 signal source control from VMON2 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
3	SEL_PG0_VMON1	R/W	0h	PG0 signal source control from VMON1 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
2	SEL_PG0_BOOST	R/W	0h	PG0 signal source control from Boost 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
1	SEL_PG0_BUCK1	R/W	0h	PG0 signal source control from Buck1 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
0	SEL_PG0_BUCK0	R/W	0h	PG0 signal source control from Buck0 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)

7.6.1.1.26 PG0_FAULT Register (Offset = 19h) [reset = 0h]

 PG0_FAULT is shown in [Figure 52](#) and described in [Table 36](#).

 Return to [Summary Table](#).

Figure 52. PG0_FAULT Register

7	6	5	4	3	2	1	0
RESERVED	PG0_FAULT_T WARN	PG0_FAULT_V ANA	PG0_FAULT_V MON2	PG0_FAULT_V MON1	PG0_FAULT_B OOST	PG0_FAULT_B UCK1	PG0_FAULT_B UCK0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 36. PG0_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PG0_FAULT_TWARN	R	0h	Source for PG0 inactive signal: 0 - TWARN has not set PG0 signal inactive. 1 - TWARN is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when TWARN is valid.

Table 36. PG0_FAULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PG0_FAULT_VANA	R	0h	Source for PG0 inactive signal: 0 - VANA has not set PG0 signal inactive. 1 - VANA is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VANA input is valid.
4	PG0_FAULT_VMON2	R	0h	Source for PG0 inactive signal: 0 - VMON2 has not set PG0 signal inactive. 1 - VMON2 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VMON2 input is valid.
3	PG0_FAULT_VMON1	R	0h	Source for PG0 inactive signal: 0 - VMON1 has not set PG0 signal inactive. 1 - VMON1 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VMON1 input is valid.
2	PG0_FAULT_BOOST	R	0h	Source for PG0 inactive signal: 0 - Boost has not set PG0 signal inactive. 1 - Boost is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Boost output is valid.
1	PG0_FAULT_BUCK1	R	0h	Source for PG0 inactive signal: 0 - Buck1 has not set PG0 signal inactive. 1 - Buck1 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.
0	PG0_FAULT_BUCK0	R	0h	Source for PG0 inactive signal: 0 - Buck0 has not set PG0 signal inactive. 1 - Buck0 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

7.6.1.1.27 PG1_CTRL Register (Offset = 1Ah) [reset = 0h]

PG1_CTRL is shown in [Figure 53](#) and described in [Table 37](#).

Return to [Summary Table](#).

Figure 53. PG1_CTRL Register

7	6	5	4	3	2	1	0
PG1_RISE_DE LAY	SEL_PG1_TW ARN	SEL_PG1_VAN A	SEL_PG1_VM ON2	SEL_PG1_VM ON1	SEL_PG1_BO OST	SEL_PG1_BUC K1	SEL_PG1_BUC K0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 37. PG1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG1_RISE_DELAY	R/W	0h	0 - PG1 rise is not delayed 1 - PG1 rise is delayed 11ms
6	SEL_PG1_TWARN	R/W	0h	PG1 control from thermal warning: 0 - Masked 1 - Affecting PGOOD (Default from OTP memory)
5	SEL_PG1_VANA	R/W	0h	PG1 signal source control from VANA 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)

Table 37. PG1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEL_PG1_VMON2	R/W	0h	PG1 signal source control from VMON2 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
3	SEL_PG1_VMON1	R/W	0h	PG1 signal source control from VMON1 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
2	SEL_PG1_BOOST	R/W	0h	PG1 signal source control from Boost 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
1	SEL_PG1_BUCK1	R/W	0h	PG1 signal source control from Buck1 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
0	SEL_PG1_BUCK0	R/W	0h	PG1 signal source control from Buck0 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)

7.6.1.1.28 PG1_FAULT Register (Offset = 1Bh) [reset = 0h]

PG1_FAULT is shown in [Figure 54](#) and described in [Table 38](#).

Return to [Summary Table](#).

Figure 54. PG1_FAULT Register

7	6	5	4	3	2	1	0
RESERVED	PG1_FAULT_TWARN	PG1_FAULT_VANA	PG1_FAULT_VMON2	PG1_FAULT_VMON1	PG1_FAULT_BOOST	PG1_FAULT_BUCK1	PG1_FAULT_BUCK0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 38. PG1_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PG1_FAULT_TWARN	R	0h	Source for PG1 inactive signal: 0 - TWARN has not set PG1 signal inactive. 1 - TWARN is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when TWARN is valid.
5	PG1_FAULT_VANA	R	0h	Source for PG1 inactive signal: 0 - VANA has not set PG1 signal inactive. 1 - VANA is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VANA input is valid.
4	PG1_FAULT_VMON2	R	0h	Source for PG1 inactive signal: 0 - VMON2 has not set PG1 signal inactive. 1 - VMON2 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VMON2 input is valid.

Table 38. PG1_FAULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PG1_FAULT_VMON1	R	0h	Source for PG1 inactive signal: 0 - VMON1 has not set PG1 signal inactive. 1 - VMON1 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VMON1 input is valid.
2	PG1_FAULT_BOOST	R	0h	Source for PG1 inactive signal: 0 - Boost has not set PG1 signal inactive. 1 - Boost is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Boost output is valid.
1	PG1_FAULT_BUCK1	R	0h	Source for PG1 inactive signal: 0 - Buck1 has not set PG1 signal inactive. 1 - Buck1 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.
0	PG1_FAULT_BUCK0	R	0h	Source for PG1 inactive signal: 0 - Buck0 has not set PG1 signal inactive. 1 - Buck0 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

7.6.1.1.29 WD_CTRL_1 Register (Offset = 1Ch) [reset = 0h]

WD_CTRL_1 is shown in [Figure 55](#) and described in [Table 39](#).

Return to [Summary Table](#).

Figure 55. WD_CTRL_1 Register

7	6	5	4	3	2	1	0
WD_CLOSE_TIME		WD_OPEN_TIME		WD_LONG_OPEN_TIME		WD_RESET_CNTR_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 39. WD_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CLOSE_TIME	R/W	0h	Watchdog close window time select. 00 - 10ms 01 - 20ms 10 - 50ms 11 - 100ms (Default from OTP memory)
5-4	WD_OPEN_TIME	R/W	0h	Watchdog open window time select. 00 - 20ms 01 - 100ms 10 - 200ms 11 - 600ms (Default from OTP memory)
3-2	WD_LONG_OPEN_TIME	R/W	0h	Watchdog long open window time select. 00 - 200ms 01 - 600ms 10 - 2000ms 11 - 5000ms (Default from OTP memory)

Table 39. WD_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	WD_RESET_CNTR_SEL	R/W	0h	Watchdog reset counter threshold select. After the selected number of reset (WDR) pulses system restart sequence is initiated. 00 - system restart disabled 01 - 1 10 - 2 11 - 4 (Default from OTP memory)

7.6.1.1.30 WD_CTRL_2 Register (Offset = 1Dh) [reset = 1h]

WD_CTRL_2 is shown in [Figure 56](#) and described in [Table 40](#).

Return to [Summary Table](#).

Figure 56. WD_CTRL_2 Register

7	6	5	4	3	2	1	0
WD_LOCK	RESERVED		WD_SYS_RESTART_FLAG_MODE	WD_EN_OTP_READ	WDI_PD	WDR_POL	WDR_OD
R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

Table 40. WD_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_LOCK	R	0h	Lock bit for watchdog controls. Locks all controls to watchdog in registers WD_CTRL_1, WD_CTRL_2. Lock bit also locks itself. Once lock bit is written 1 it cannot be written 0. Only reset can clear it. 0 - Not locked 1 - Locked WD_STATUS register is not affected by WD_LOCK bit. WD_SYSTEM_RESTART_FLAG and WD_RESET_CNTR_STATUS can be cleared even if WD_LOCK=1.
6-5	RESERVED	R/W	0h	
4	WD_SYS_RESTART_FLAG_MODE	R/W	0h	WD_SYSTEM_RESTART_FLAG mode select. 0 - WD_SYSTEM_RESTART_FLAG is only a status bit. 1 - WD_SYSTEM_RESTART_FLAG prevents further system restarts until it is cleared. (Default from OTP memory)
3	WD_EN_OTP_READ	R/W	0h	Read OTP during system restart sequence 0 - OTP read not enabled during system restart sequence 1 - OTP read enabled during system restart sequence (Default from OTP memory)
2	WDI_PD	R/W	0h	Selects the pull down resistor on the WDI pin: 0 - Pull-down resistor is disabled 1 - Pull-down resistor is enabled (Default from OTP memory)
1	WDR_POL	R/W	0h	Watchdog reset output (WDR) polarity select 0 - Active high 1 - Active low (Default from OTP memory)
0	WDR_OD	R/W	1h	Watchdog reset output (WDR) signal type 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)

7.6.1.1.31 WD_STATUS Register (Offset = 1Eh) [reset = 0h]

WD_STATUS is shown in [Figure 57](#) and described in [Table 41](#).

Return to [Summary Table](#).

Figure 57. WD_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			WD_CLR_SYSTEM_RESTART_FLAG	WD_SYSTEM_RESTART_FLAG	WD_CLR_RESET_CNTR	WD_RESET_CNTR_STATUS	
R/W-0h			R-0h	R-0h	R-0h	R-0h	

Table 41. WD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	WD_CLR_SYSTEM_RESTART_FLAG	R	0h	Clear bit for WD_SYSTEM_RESTART_FLAG. Write 1 to generate a clear pulse. Reg bit value returns to 0 after clearing is finished.
3	WD_SYSTEM_RESTART_FLAG	R	0h	Watchdog requested system restart has occurred. Can be cleared by writing WD_CLR_SYSTEM_RESTART_FLAG bit 1.
2	WD_CLR_RESET_CNTR	R	0h	Watchdog reset counter clear. Write 1 to generate a clear pulse.
1-0	WD_RESET_CNTR_STATUS	R	0h	Current status of watchdog reset counter.

7.6.1.1.32 RESET Register (Offset = 1Fh) [reset = 0h]

RESET is shown in [Figure 58](#) and described in [Table 42](#).

Return to [Summary Table](#).

Figure 58. RESET Register

7	6	5	4	3	2	1	0
RESERVED							SW_RESET
R/W-0h							R-0h

Table 42. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SW_RESET	R	0h	Software commanded reset. When written to 1, the registers will be reset to default values and OTP memory is read. The bit is automatically cleared.

7.6.1.1.33 INT_TOP_1 Register (Offset = 20h) [reset = 0h]

INT_TOP_1 is shown in [Figure 59](#) and described in [Table 43](#).

Return to [Summary Table](#).

Figure 59. INT_TOP_1 Register

7	6	5	4	3	2	1	0
I_MEAS_INT	DIAG_INT	BOOST_INT	BUCK_INT	SYNC_CLK_INT	TDIE_SD_INT	TDIE_WARN_INT	OVP_INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 43. INT_TOP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I_MEAS_INT	R	0h	Latched status bit indicating that the load current measurement result is available in I_LOAD_1 and I_LOAD_2 registers. Write 1 to clear interrupt.

Table 43. INT_TOP_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DIAG_INT	R	0h	Interrupt indicating that INT_DIAG register has a pending interrupt. The reason for the interrupt is indicated in INT_DIAG register. This bit is cleared automatically when INT_DIAG register is cleared to 0x00.
5	BOOST_INT	R	0h	Interrupt indicating that BOOST have a pending interrupt. The reason for the interrupt is indicated in INT_BOOST register. This bit is cleared automatically when INT_BOOST register is cleared to 0x00.
4	BUCK_INT	R	0h	Interrupt indicating that BUCK0 and/or BUCK1 have a pending interrupt. The reason for the interrupt is indicated in INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.
3	SYNC_CLK_INT	R	0h	Latched status bit indicating that the external clock frequency became valid or invalid. Write 1 to clear interrupt.
2	TDIE_SD_INT	R	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The converters have been disabled if they were enabled. The converters cannot be enabled if this bit is active. The actual status of the thermal warning is indicated by TDIE_SD_INT_STAT bit in TOP_STAT register. Write 1 to clear interrupt. Clearing TSD interrupt automatically re-enables converters. Clearing this interrupt will also clear thermal warning status.
1	TDIE_WARN_INT	R	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TDIE_WARN_INT_STAT bit in TOP_STAT register. Write 1 to clear interrupt.
0	OVP_INT	R	0h	Latched status bit indicating that the input voltage has exceeded the over-voltage detection level. The actual status of the over-voltage is indicated by OVP bit in TOP_STAT register. Write 1 to clear interrupt.

7.6.1.1.34 INT_TOP_2 Register (Offset = 21h) [reset = 0h]

 INT_TOP_2 is shown in [Figure 60](#) and described in [Table 44](#).

 Return to [Summary Table](#).

Figure 60. INT_TOP_2 Register

7	6	5	4	3	2	1	0
RESERVED							RESET_REG_INT
R/W-0h							R-0h

Table 44. INT_TOP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_REG_INT	R	0h	Latched status bit indicating that either VANA supply voltage has been below undervoltage threshold level or the host has requested a reset (SW_RESET bit in RESET register). The converters have been disabled, and registers are reset to default values and the normal startup procedure is done. Write 1 to clear interrupt.

7.6.1.1.35 INT_BUCK Register (Offset = 22h) [reset = 0h]

 INT_BUCK is shown in [Figure 61](#) and described in [Table 45](#).

 Return to [Summary Table](#).

Figure 61. INT_BUCK Register

7	6	5	4	3	2	1	0
RESERVED	BUCK1_PG_IN T	BUCK1_SC_IN T	BUCK1_ILIM_I NT	RESERVED	BUCK0_PG_IN T	BUCK0_SC_IN T	BUCK0_ILIM_I NT
R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h

Table 45. INT_BUCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	BUCK1_PG_INT	R	0h	Latched status bit indicating that BUCK1 powergood event has been detected. Write 1 to clear.
5	BUCK1_SC_INT	R	0h	Latched status bit indicating that the BUCK1 output voltage has fallen below 0.35 V level during operation or BUCK1 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
4	BUCK1_ILIM_INT	R	0h	Latched status bit indicating that BUCK1 output current limit has been triggered. Write 1 to clear.
3	RESERVED	R/W	0h	
2	BUCK0_PG_INT	R	0h	Latched status bit indicating that BUCK0 powergood event has been detected. Write 1 to clear.
1	BUCK0_SC_INT	R	0h	Latched status bit indicating that the BUCK0 output voltage has fallen below 0.35 V level during operation or BUCK0 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
0	BUCK0_ILIM_INT	R	0h	Latched status bit indicating that BUCK0 output current limit has been triggered. Write 1 to clear.

7.6.1.1.36 INT_BOOST Register (Offset = 23h) [reset = 0h]

 INT_BOOST is shown in [Figure 62](#) and described in [Table 46](#).

 Return to [Summary Table](#).

Figure 62. INT_BOOST Register

7	6	5	4	3	2	1	0
RESERVED					BOOST_PG_IN T	BOOST_SC_IN T	BOOST_ILIM_I NT
R/W-0h					R-0h	R-0h	R-0h

Table 46. INT_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	BOOST_PG_INT	R	0h	Latched status bit indicating that Boost powergood event has been detected. Write 1 to clear.

Table 46. INT_BOOST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BOOST_SC_INT	R	0h	Latched status bit indicating that the Boost output voltage has fallen to input voltage level or below 2.5 V level during operation or BOOST output didn't reach 2.5 V level in 1 ms from enable. Write 1 to clear.
0	BOOST_ILIM_INT	R	0h	Latched status bit indicating that Boost output current limit has been triggered. Write 1 to clear.

7.6.1.1.37 INT_DIAG Register (Offset = 24h) [reset = 0h]

INT_DIAG is shown in [Figure 63](#) and described in [Table 47](#).

Return to [Summary Table](#).

Figure 63. INT_DIAG Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_PG_INT	RESERVED	VMON1_PG_INT	RESERVED	VANA_PG_INT
R/W-0h			R-0h	R/W-0h	R-0h	R/W-0h	R-0h

Table 47. INT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	VMON2_PG_INT	R	0h	Latched status bit indicating that VMON2 powergood event has been detected. Write 1 to clear.
3	RESERVED	R/W	0h	
2	VMON1_PG_INT	R	0h	Latched status bit indicating that VMON1 powergood event has been detected. Write 1 to clear.
1	RESERVED	R/W	0h	
0	VANA_PG_INT	R	0h	Latched status bit indicating that VANA powergood event has been detected. Write 1 to clear.

7.6.1.1.38 TOP_STATUS Register (Offset = 25h) [reset = 0h]

TOP_STATUS is shown in [Figure 64](#) and described in [Table 48](#).

Return to [Summary Table](#).

Figure 64. TOP_STATUS Register

7	6	5	4	3	2	1	0
RESERVED				SYNC_CLK_STAT	TDIE_SD_STAT	TDIE_WARN_STAT	OVP_STAT
R-0h				R-0h	R-0h	R-0h	R-0h

Table 48. TOP_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	SYNC_CLK_STAT	R	0h	Status bit indicating the status of external clock (CLKIN): 0 - External clock frequency is valid 1 - External clock frequency is not valid.

Table 48. TOP_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TDIE_SD_STAT	R	0h	Status bit indicating the status of thermal shutdown: 0 - Die temperature below thermal shutdown level 1 - Die temperature above thermal shutdown level.
1	TDIE_WARN_STAT	R	0h	Status bit indicating the status of thermal warning: 0 - Die temperature below thermal warning level 1 - Die temperature above thermal warning level.
0	OVP_STAT	R	0h	Status bit indicating the status of input overvoltage monitoring: 0 - Input voltage below overvoltage threshold level 1 - Input voltage above overvoltage threshold level.

7.6.1.1.39 BUCK_STATUS Register (Offset = 26h) [reset = 0h]

BUCK_STATUS is shown in [Figure 65](#) and described in [Table 49](#).

Return to [Summary Table](#).

Figure 65. BUCK_STATUS Register

7	6	5	4	3	2	1	0
BUCK1_STAT	BUCK1_PG_S TAT	RESERVED	BUCK1_ILIM_S TAT	BUCK0_STAT	BUCK0_PG_S TAT	RESERVED	BUCK0_ILIM_S TAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 49. BUCK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_STAT	R	0h	Status bit indicating the enable/disable status of BUCK1: 0 - BUCK1 converter is disabled 1 - BUCK1 converter is enabled.
6	BUCK1_PG_STAT	R	0h	Status bit indicating BUCK1 output voltage validity (raw status) 0 - BUCK1 output is not valid 1 - BUCK1 output is valid.
5	RESERVED	R	0h	Reserved
4	BUCK1_ILIM_STAT	R	0h	Status bit indicating BUCK1 current limit status (raw status) 0 - BUCK1 output current is below current limit threshold level 1 - BUCK1 output current is at current limit threshold level.
3	BUCK0_STAT	R	0h	Status bit indicating the enable/disable status of BUCK0: 0 - BUCK0 converter is disabled 1 - BUCK0 converter is enabled.
2	BUCK0_PG_STAT	R	0h	Status bit indicating BUCK0 output voltage validity (raw status) 0 - BUCK0 output is not valid 1 - BUCK0 output is valid.
1	RESERVED	R	0h	Reserved
0	BUCK0_ILIM_STAT	R	0h	Status bit indicating BUCK0 current limit status (raw status) 0 - BUCK0 output current is below current limit threshold level 1 - BUCK0 output current is at current limit threshold level.

7.6.1.1.40 BOOST_STATUS Register (Offset = 27h) [reset = 0h]

BOOST_STATUS is shown in [Figure 66](#) and described in [Table 50](#).

Return to [Summary Table](#).

Figure 66. BOOST_STATUS Register

7	6	5	4	3	2	1	0
RESERVED				BOOST_STAT	BOOST_PG_S TAT	RESERVED	BOOST_ILIM_ STAT
R-0h				R-0h	R-0h	R-0h	R-0h

Table 50. BOOST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BOOST_STAT	R	0h	Status bit indicating the enable/disable status of Boost: 0 - Boost converter is disabled 1 - Boost converter is enabled.
2	BOOST_PG_STAT	R	0h	Status bit indicating Boost output voltage validity (raw status) 0 - Boost output is not valid 1 - Boost output is valid.
1	RESERVED	R	0h	Reserved
0	BOOST_ILIM_STAT	R	0h	Status bit indicating Boost current limit status (raw status) 0 - Boost output current is below current limit threshold level 1 - Boost output current is at current limit threshold level.

7.6.1.1.41 DIAG_STATUS Register (Offset = 28h) [reset = 0h]

DIAG_STATUS is shown in [Figure 67](#) and described in [Table 51](#).

Return to [Summary Table](#).

Figure 67. DIAG_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_PG_S TAT	RESERVED	VMON1_PG_S TAT	RESERVED	VANA_PG_ST AT
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

Table 51. DIAG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	VMON2_PG_STAT	R	0h	Status bit indicating VMON2 input voltage validity (raw status) 0 - VMON2 voltage is not valid 1 - VMON2 voltage is valid.
3	RESERVED	R	0h	
2	VMON1_PG_STAT	R	0h	Status bit indicating VMON1 input voltage validity (raw status) 0 - VMON1 voltage is not valid 1 - VMON1 voltage is valid.
1	RESERVED	R	0h	
0	VANA_PG_STAT	R	0h	Status bit indicating VANA input voltage validity (raw status) 0 - VANA voltage is not valid 1 - VANA voltage is valid.

7.6.1.1.42 TOP_MASK_1 Register (Offset = 29h) [reset = 0h]

TOP_MASK_1 is shown in [Figure 68](#) and described in [Table 52](#).

Return to [Summary Table](#).

Figure 68. TOP_MASK_1 Register

7	6	5	4	3	2	1	0
I_MEAS_MASK	RESERVED			SYNC_CLK_M ASK	RESERVED	TDIE_WARN_ MASK	RESERVED
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 52. TOP_MASK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I_MEAS_MASK	R/W	0h	Masking for load current measurement ready interrupt MEAS_INT in INT_TOP_1 register. 0 - Interrupt generated 1 - Interrupt not generated. (Default from OTP memory)
6-4	RESERVED	R/W	0h	
3	SYNC_CLK_MASK	R/W	0h	Masking for external clock detection interrupt SYNC_CLK_INT in INT_TOP_1 register: 0 - Interrupt generated 1 - Interrupt not generated. (Default from OTP memory)
2	RESERVED	R/W	0h	
1	TDIE_WARN_MASK	R/W	0h	Masking for thermal warning interrupt TDIE_WARN_INT in INT_TOP_1 register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect TDIE_WARN_STAT status bit in TOP_STAT register. (Default from OTP memory)
0	RESERVED	R/W	0h	

7.6.1.1.43 TOP_MASK_2 Register (Offset = 2Ah) [reset = 1h]

TOP_MASK_2 is shown in [Figure 69](#) and described in [Table 53](#).

Return to [Summary Table](#).

Figure 69. TOP_MASK_2 Register

7	6	5	4	3	2	1	0
RESERVED							RESET_REG_ MASK
R/W-0h							R/W-1h

Table 53. TOP_MASK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_REG_MASK	R/W	1h	Masking for register reset interrupt RESET_REG_INT in INT_TOP_2 register: 0 - Interrupt generated 1 - Interrupt not generated. (Default from OTP memory)

7.6.1.1.44 BUCK_MASK Register (Offset = 2Bh) [reset = 0h]

BUCK_MASK is shown in [Figure 70](#) and described in [Table 54](#).

Return to [Summary Table](#).

Figure 70. BUCK_MASK Register

7	6	5	4	3	2	1	0
BUCK1_PGF_MASK	BUCK1_PGR_MASK	RESERVED	BUCK1_ILIM_MASK	BUCK0_PGF_MASK	BUCK0_PGR_MASK	RESERVED	BUCK0_ILIM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 54. BUCK_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_PGF_MASK	R/W	0h	Masking of powergood invalid detection for BUCK1 power good interrupt BUCK1_PG_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STAT register. (Default from OTP memory)
6	BUCK1_PGR_MASK	R/W	0h	Masking of powergood valid detection for BUCK1 power good interrupt BUCK1_PG_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STAT register. (Default from OTP memory)
5	RESERVED	R/W	0h	
4	BUCK1_ILIM_MASK	R/W	0h	Masking for BUCK1 current monitoring interrupt BUCK1_IMON_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_IMON_STAT status bit in BUCK_STAT register. (Default from OTP memory)
3	BUCK0_PGF_MASK	R/W	0h	Masking of powergood invalid detection for BUCK0 power good interrupt BUCK0_PG_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register. (Default from OTP memory)
2	BUCK0_PGR_MASK	R/W	0h	Masking of powergood valid detection for BUCK0 power good interrupt BUCK0_PG_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register. (Default from OTP memory)
1	RESERVED	R/W	0h	
0	BUCK0_ILIM_MASK	R/W	0h	Masking for BUCK0 current monitoring interrupt BUCK0_IMON_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_IMON_STAT status bit in BUCK_STAT register. (Default from OTP memory)

7.6.1.1.45 BOOST_MASK Register (Offset = 2Ch) [reset = 0h]

BOOST_MASK is shown in [Figure 71](#) and described in [Table 55](#).

Return to [Summary Table](#).

Figure 71. BOOST_MASK Register

7	6	5	4	3	2	1	0
RESERVED				BOOST_PGF_MASK	BOOST_PGR_MASK	RESERVED	BOOST_ILIM_MASK
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 55. BOOST_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	BOOST_PGF_MASK	R/W	0h	Masking of powergood invalid detection for Boost power good interrupt BOOST_PG_INT in INT_BOOST register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BOOST_PG_STAT status bit in BOOST_STAT register. (Default from OTP memory)
2	BOOST_PGR_MASK	R/W	0h	Masking of powergood valid detection for Boost power good interrupt BOOST_PG_INT in INT_BOOST register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BOOST_PG_STAT status bit in BOOST_STAT register. (Default from OTP memory)
1	RESERVED	R/W	0h	
0	BOOST_ILIM_MASK	R/W	0h	Masking for Boost current monitoring interrupt BOOST_IMON_INT in INT_BOOST register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BOOST_IMON_STAT status bit in BOOST_STAT register. (Default from OTP memory)

7.6.1.1.46 DIAG_MASK Register (Offset = 2Dh) [reset = 0h]

DIAG_MASK is shown in [Figure 72](#) and described in [Table 56](#).

Return to [Summary Table](#).

Figure 72. DIAG_MASK Register

7	6	5	4	3	2	1	0
RESERVED		VMON2_PGF_MASK	VMON2_PGR_MASK	VMON1_PGF_MASK	VMON1_PGR_MASK	VANA_PGF_MASK	VANA_PGR_MASK
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 56. DIAG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	VMON2_PGF_MASK	R/W	0h	Masking of VMON2 invalid detection for powergood interrupt VMON2_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VMON2_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)

Table 56. DIAG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	VMON2_PGR_MASK	R/W	0h	Masking of VMON2 valid detection for powergood interrupt VMON2_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VMON2_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)
3	VMON1_PGF_MASK	R/W	0h	Masking of VMON1 invalid detection for powergood interrupt VMON1_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VMON1_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)
2	VMON1_PGR_MASK	R/W	0h	Masking of VMON1 valid detection for powergood interrupt VMON1_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VMON1_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)
1	VANA_PGF_MASK	R/W	0h	Masking of VANA invalid detection for powergood interrupt VANA_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VANA_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)
0	VANA_PGR_MASK	R/W	0h	Masking of VANA valid detection for powergood interrupt VANA_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VANA_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)

7.6.1.1.47 SEL_I_LOAD Register (Offset = 2Eh) [reset = 0h]

SEL_I_LOAD is shown in [Figure 73](#) and described in [Table 57](#).

Return to [Summary Table](#).

Figure 73. SEL_I_LOAD Register

7	6	5	4	3	2	1	0
RESERVED						LOAD_CURRENT_BUCK_SELECT	
R/W-0h						R/W-0h	

Table 57. SEL_I_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	LOAD_CURRENT_BUCK_SELECT	R/W	0h	Start the current measurement on the selected Buck converter: 0 - BUCK0 1 - BUCK1 2 - BUCK0 3 - BUCK1 The measurement is started when register is written.

7.6.1.1.48 I_LOAD_2 Register (Offset = 2Fh) [reset = 0h]

 I_LOAD_2 is shown in [Figure 74](#) and described in [Table 58](#).

 Return to [Summary Table](#).

Figure 74. I_LOAD_2 Register

7	6	5	4	3	2	1	0
RESERVED							BUCK_LOAD_CURRENT_8
R-0h							R-0h

Table 58. I_LOAD_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	BUCK_LOAD_CURRENT_8	R	0h	This register describes the MSB bit of the average load current on selected converter with a resolution of 20 mA per LSB and max 10 A current.

7.6.1.1.49 I_LOAD_1 Register (Offset = 30h) [reset = 0h]

 I_LOAD_1 is shown in [Figure 75](#) and described in [Table 59](#).

 Return to [Summary Table](#).

Figure 75. I_LOAD_1 Register

7	6	5	4	3	2	1	0
BUCK_LOAD_CURRENT_7_0							
R-0h							

Table 59. I_LOAD_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK_LOAD_CURRENT_7_0	R	0h	This register describes 8 LSB bits of the average load current on selected converter with a resolution of 20 mA per LSB and max 10 A current.

7.6.1.1.50 FREQ_SEL Register (Offset = 31h) [reset = 0h]

 FREQ_SEL is shown in [Figure 76](#) and described in [Table 60](#).

 Return to [Summary Table](#).

Figure 76. FREQ_SEL Register

7	6	5	4	3	2	1	0
RESERVED					BOOST_FREQ_SEL	BUCK_FREQ_SEL	
R/W-0h					R/W-0h	R/W-0h	

Table 60. FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	BOOST_FREQ_SEL	R/W	0h	Boost switching frequency: 0 - 2 MHz 1 - 4 MHz (Default from OTP memory)

Table 60. FREQ_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	BUCK_FREQ_SEL	R/W	0h	Buck0 and Buck1 switching frequency: 0x0 - 2 MHz 0x1 - 3 MHz 0x2 - 4 MHz 0x3 - 4 MHz (Default from OTP memory)

7.6.1.1.51 BOOST_ILIM_CTRL Register (Offset = 32h) [reset = 0h]

BOOST_ILIM_CTRL is shown in [Figure 77](#) and described in [Table 61](#).

Return to [Summary Table](#).

Figure 77. BOOST_ILIM_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						BOOST_ILIM	
R/W-0h						R/W-0h	

Table 61. BOOST_ILIM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	BOOST_ILIM	R/W	0h	Sets the current limit of Boost. 00 - 1.0 A 01 - 1.4 A 10 - 1.9 A 11 - 2.8 A (Default from OTP memory)

7.6.1.1.52 ECC_STATUS Register (Offset = 33h) [reset = 0h]

ECC_STATUS is shown in [Figure 78](#) and described in [Table 62](#).

Return to [Summary Table](#).

Figure 78. ECC_STATUS Register

7	6	5	4	3	2	1	0
RESERVED						DED	SED
R-0h						R-0h	R-0h

Table 62. ECC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	DED	R	0h	OTP error correction status: 0 - No dual errors detected 1 - Dual errors detected and not corrected
0	SED	R	0h	OTP error correction status: 0 - No single errors detected 1 - Single errors detected and corrected

7.6.1.1.53 WD_DIS_CTRL_CODE Register (Offset = 34h) [reset = 0h]

WD_DIS_CTRL_CODE is shown in [Figure 79](#) and described in [Table 63](#).

Return to [Summary Table](#).

Figure 79. WD_DIS_CTRL_CODE Register

7	6	5	4	3	2	1	0
WD_DIS_UNLOCK_CODE							
R-0h							

Table 63. WD_DIS_CTRL_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_DIS_UNLOCK_CODE	R	0h	Unlocking WD_DIS_CTRL bit: Set WD_DIS_CTRL_LOCK=0 by writing 0x87, 0x65, 0x1B by 3 consecutive I2C write sequences to WD_DIS_CTRL_CODE register. Locking WD_DIS_CTRL bit: Set WD_DIS_CTRL_LOCK=1 by writing anything to WD_DIS_CTRL_CODE register or write WD_LOCK=1. Reading this address returns always 0x00. WD_DIS_CTRL can be unlocked only if WD_LOCK=0.

7.6.1.1.54 WD_DIS_CONTROL Register (Offset = 35h) [reset = 0h]

WD_DIS_CONTROL is shown in [Figure 80](#) and described in [Table 64](#).

Return to [Summary Table](#).

Figure 80. WD_DIS_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED						WD_DIS_CTRL_LOCK	WD_DIS_CTRL
R/W-0h						R-0h	R/W-0h

Table 64. WD_DIS_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	WD_DIS_CTRL_LOCK	R	0h	Lock status for WD_DIS_CTRL bit. 0 - Not locked, WD_DIS_CTRL bit can be written. 1 - Locked, WD_DIS_CTRL bit is forced to 0 and it cannot be written. Lock can be opened by writing 0x87, 0x65, 0x1B by 3 consecutive I2C write sequences to WD_DIS_CTRL_CODE register if WD_LOCK=0. Lock can be closed by writing anything to WD_DIS_CTRL_CODE register or writing WD_LOCK=1.
0	WD_DIS_CTRL	R/W	0h	Watchdog disable pin control. 0 - Watchdog cannot be disabled by WD_DIS pin. 1 - Watchdog can be disabled by WD_DIS pin. (Default from OTP memory) This bit can be written 1 only if WD_LOCK=0 and WD_DIS_CTRL_LOCK=0.

8 Application and Implementation

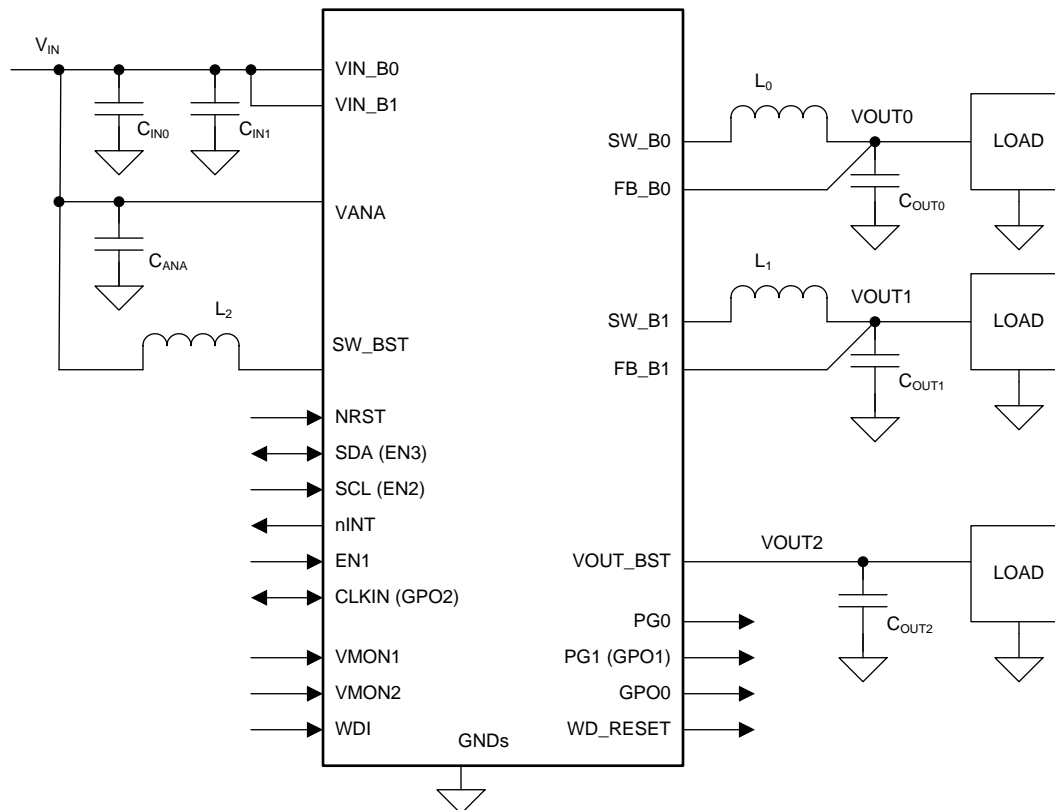
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP87702-Q1 is a power-management unit including a boost converter, two step-down converters, and three general-purpose digital output signals.

8.2 Typical Application



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Figure 81. LP87702-Q1 Typical Application

8.2.1 Design Requirements

Table 65. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Output voltages	1.8 V, 1.24 V, 5 V
Switching frequency	4 MHz

8.2.2 Detailed Design Procedure

The performance of the LP87702-Q1 device depends greatly on the care taken in designing the printed circuit board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from system power rail during turnon of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can easily become the performance limiting items. The separate buck converter power pins VIN_Bx are not connected together internally. The VIN_Bx power connections shall be connected together outside the package using power plane construction.

8.2.2.1 Application Components

8.2.2.1.1 Inductor Selection

The inductors L_0 , L_1 , and L_2 are shown in the [Typical Application](#). The inductance and DCR of the inductor affects the control loop of the buck and boost converter. It is recommended to use inductors or similar ones listed in [Table 66](#). Pay attention to the saturation current and temperature rise current of the inductor. Check that the saturation current is higher than the peak current limit and the temperature rise current is higher than the maximum expected rms output current. For minimum effective inductance to ensure good performance refer to [Specifications](#). DC resistance of the inductor should be less than 0.05 Ω for good efficiency at high-current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Shielded inductors are preferred as they radiate less noise.

Table 66. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS L x W x H (mm)	RATED DC CURRENT, I _{SAT} max (typ) / I _{TEMP} max (typ) (A)	DCR typ / max (m Ω)
TOKO	DFE252012PD-R47M	0.47 μ H (20%)	2.5 x 2 x 1.2	5.2 (-) / 4 (-) ⁽¹⁾	- / 27
TOKO	DFE252012PD-1R0M	1 μ H (20%)	2.5 x 2 x 1.2	3.8 (4.5) / 3.2 (3.8) ⁽¹⁾	35 / 42
Tayo Yuden	MDMK2020TR47MMV	0.47 μ H (20%)	2 x 2 x 1.2	4.2 (4.8) / 2.3 (2.45)	40 / 46
TDK	TFM252012ALMA1R0MTAA	0.47 μ H (20%)	2.5 x 2 x 1.2	5.8 (6.5) / 4.9 (5.6)	19 / 24

(1) Operating temperature range is up to 125°C including self temperature rise.

8.2.2.1.2 Buck Input Capacitor Selection

The input capacitors C_{IN0} and C_{IN1} are shown in the [Typical Application](#). A ceramic input bypass capacitor of 10 μ F is required for both converters. Place the input capacitor as close as possible to the VIN_Bx pin and PGND_Bx pin of the device. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. DC bias characteristics of the capacitors must also be considered. Minimum effective input capacitance to ensure good performance is 1.9 μ F per buck input at maximum input voltage including tolerances and ambient temperature range. In addition there must be at least 22 μ F of additional capacitance common for all the power input pins on the system power rail. See [Table 67](#).

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. In addition ferrite can be used in front of the input capacitor to reduce the EMI.

Table 67. Recommended Buck Input Capacitors (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM21BR71A106KE22	10 μ F (10%)	0805	2 x 1.25 x 1.25	10 V
TDK	CGA4J3X7S1A106K125AB	10 μ F (10%)	0805	2 x 1.25 x 1.25	10 V

8.2.2.1.3 Buck Output Capacitor Selection

The output capacitor C_{OUT0} and C_{OUT1} are shown in *Typical Application*. A ceramic local output capacitor of 22 μF is required for both outputs. Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance for good performance is 15 μF per including the DC voltage roll-off, tolerances, aging and temperature effects.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its RESR. The RESR is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part. See [Table 68](#).

POL capacitors can be used to improve load transient performance and to decrease the ripple voltage. A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreases the PFM switching frequency. Note that the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (100- μF range) output capacitors. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be longer. At shutdown the output voltage is discharged to 0.6 V level using forced-PWM operation. This can increase the input voltage if the load current is small and the output capacitor is large compared to input capacitor. Below 0.6 V level the output capacitor is discharged by the internal discharge resistor and with large capacitor more time is required to settle V_{OUT} down as a consequence of the increased time constant.

Table 68. Recommended Buck Output Capacitors (X7R or X7T Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM31CR71A226KE02	22 μF (10%)	1206	3.2 x 1.6 x 1.6	10 V
TDK	CGA5L1X7S1A226M160AC	22 μF (20%)	1206	3.2 x 1.6 x 1.6	10 V

8.2.2.1.4 Boost Input Capacitor Selection

A ceramic input capacitor of 10 μF is sufficient for most applications. Place the input capacitor close to the SW_BST pin of the device. Use X7R types, do not use Y5V or F. See [Table 69](#).

Table 69. Recommended Boost Input Capacitors (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM21BR71A106KE22	10 μF (10%)	0805	2.0 x 1.25 x 1.25	10 V

8.2.2.1.5 Boost Output Capacitor Selection

Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. Place the output capacitor as close as possible to the V_{OUT_BST} pin and $PGND_BST$ pin of the device. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to support load transients. See [Table 70](#).

Table 70. Recommended Boost Output Capacitors (X7R or X7T Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM31CR71A226KE02	22 μF (10%)	1206	3.2 x 1.6 x 1.6	10 V

8.2.2.1.6 Supply Filtering Components

The VANA input is used to supply analog and digital circuits in the device. See [Table 71](#) recommended components from for VANA input supply filtering.

Table 71. Recommended Supply Filtering Components

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM188R71C104KA37D	100 nF (10%)	0603	1.6 x 0.8 x 0.8	16 V
Murata	GCM155R71C104KA55D	100 nF (10%)	0402	1.0 x 0.5 x 0.5	16 V

8.2.3 Current Limit vs Maximum Output Current

For both the buck converters and the boost the current limit must be set high enough to account for inductor ripple current on top of the maximum output current. Forward current limit for the buck converters is set by BUCK0_ILIM, BUCK1_ILIM and for boost by BOOST_ILIM.

For the buck converter the inductor current ripple can be calculated using [Equation 1](#) and [Equation 2](#):

$$D = \frac{V_{OUT}}{V_{IN(max)} \times \eta} \tag{1}$$

$$\Delta I_L = \frac{(V_{IN(max)} - V_{OUT}) \times D}{f_{SW} \times L} \tag{2}$$

Example using [Equation 1](#) and [Equation 2](#):

$$V_{IN(max)} = 5.5 \text{ V}$$

$$V_{OUT} = 1 \text{ V}$$

$$\eta = 0.75$$

$$f_{SW} = 1.8 \text{ MHz}$$

$$L = 0.38 \text{ }\mu\text{H}$$

$$\text{then } D = 0.242 \text{ and } \Delta I_L = 1.59 \text{ A}$$

Peak current is half of the current ripple. If $I_{LIM_FWD_SET_OTP}$ is 3 A, the minimum forward current limit would be 2.85 A when taking the -5% tolerance into account. In this case the difference between set peak current and maximum load current = 0.795 A + 0.15 A = 0.945 A.

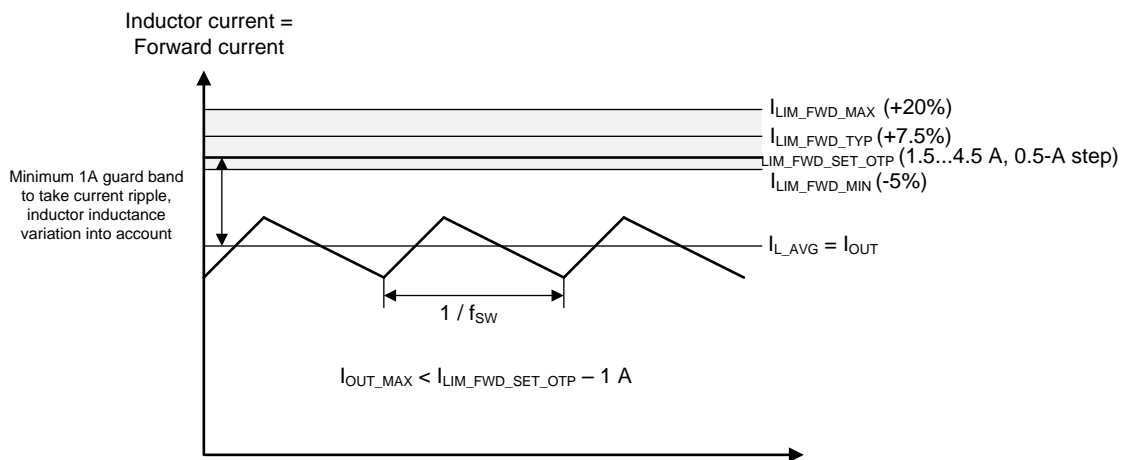


Figure 82. Current Limit vs Maximum Output Current

8.2.4 Application Curves

Unless otherwise specified: $V_{IN} = 3.3\text{ V}$, $V_{OUT_BUCK} = 1\text{ V}$, $V_{OUT_BOOST} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, f_{SW} -setting 4 MHz, $L_0 = L_1 = 0.47\text{ }\mu\text{H}$ (TOKO DFE252012PD-R47M), $L_2 = 1\text{ }\mu\text{H}$ (TFM252012ALMA1R0), C_{OUT_BUCK} , C_{POL_BUCK} , and $C_{OUT_BOOST} = 22\text{ }\mu\text{F}$. Measurements are done using connections in [Figure 81](#).

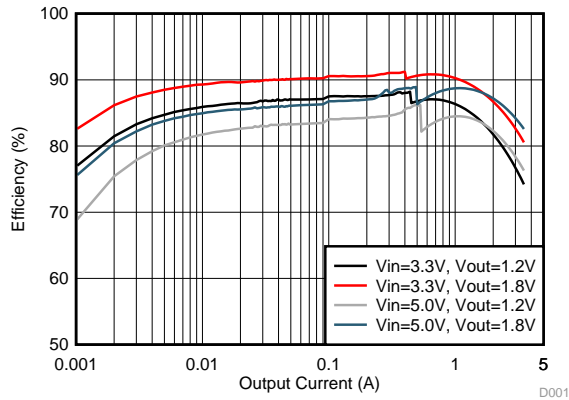
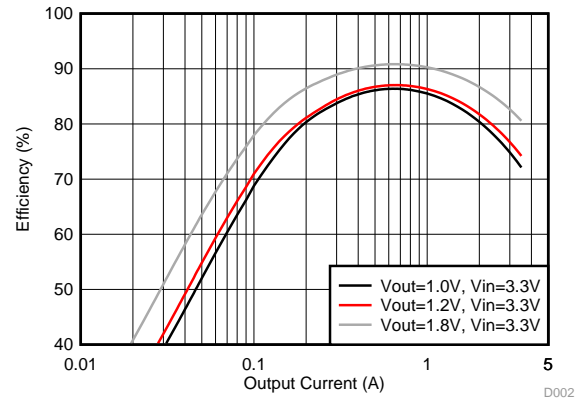
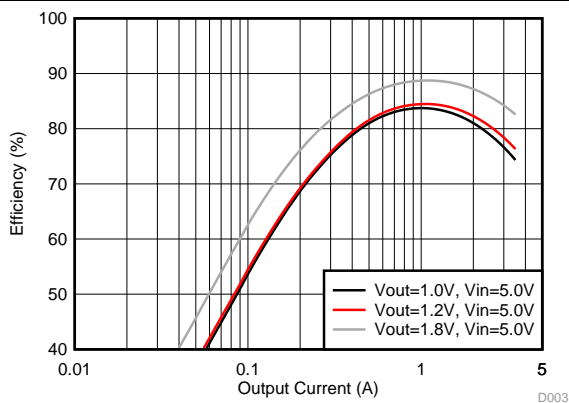


Figure 83. Buck Efficiency in AUTO (PFM/PWM) Mode



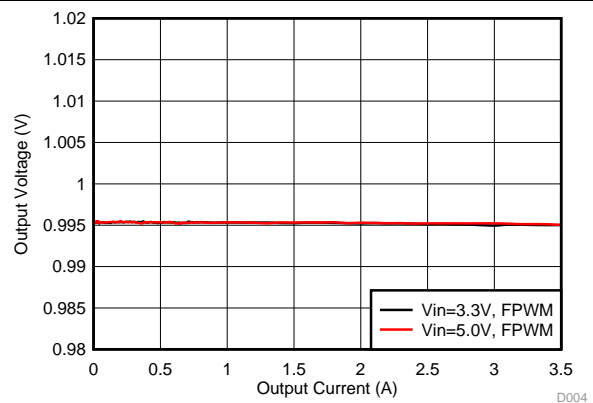
$V_{IN} = 3.3\text{ V}$

Figure 84. Buck Efficiency in Forced PWM Mode



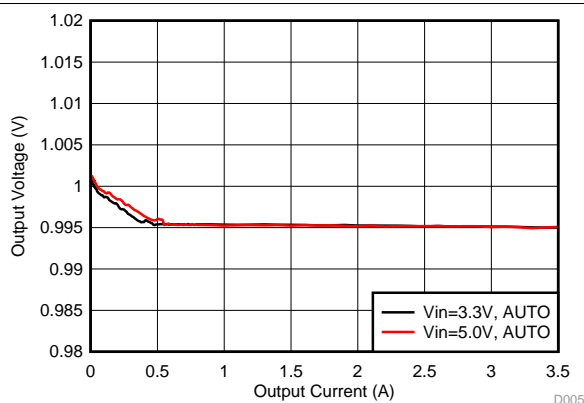
$V_{IN} = 5\text{ V}$

Figure 85. Buck Efficiency in Forced PWM Mode



$V_{OUT} = 1\text{ V}$

Figure 86. Buck Output Voltage vs Load Current in Forced PWM Mode



$V_{OUT} = 1\text{ V}$

Figure 87. Buck Output Voltage vs Load Current in AUTO Mode

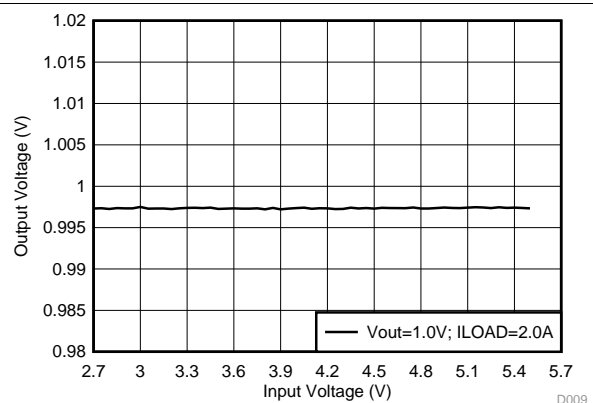
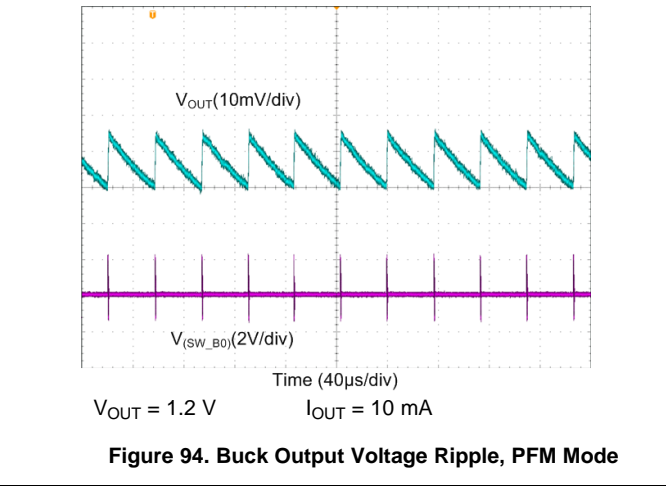
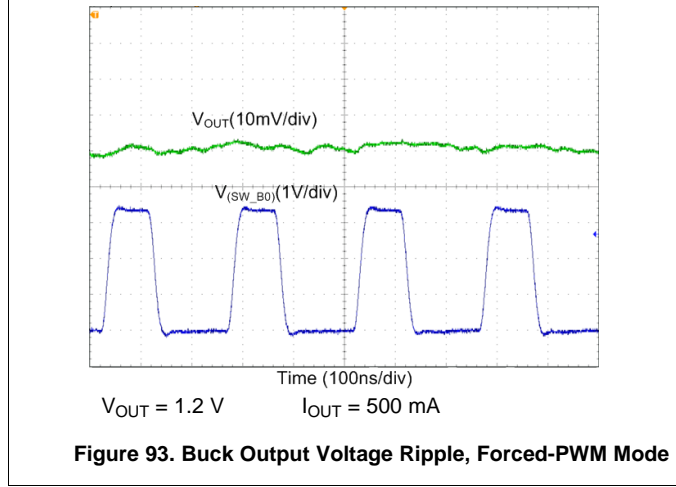
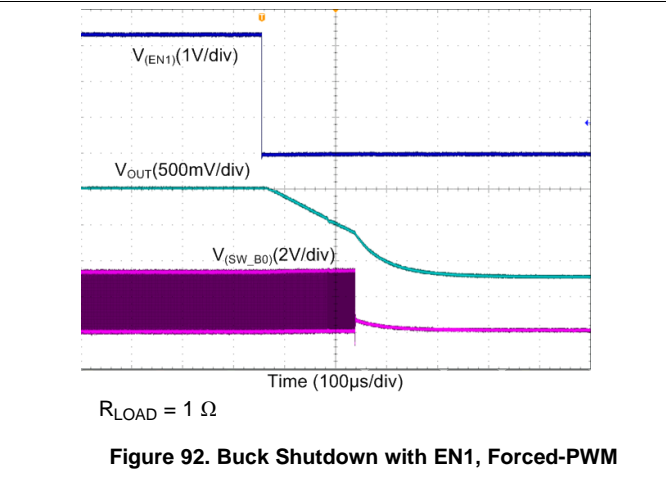
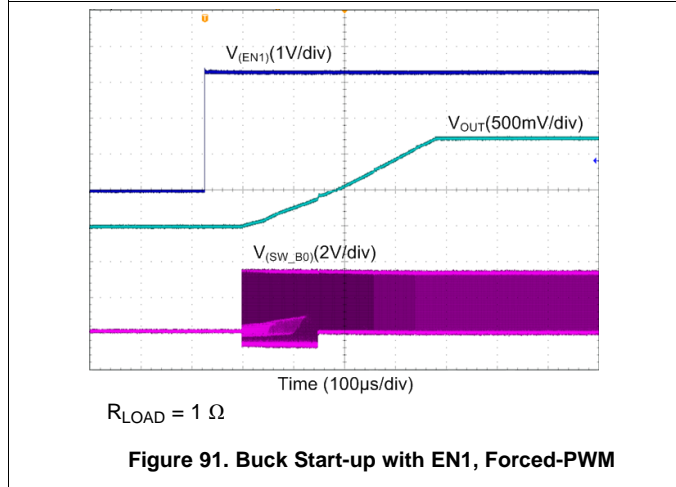
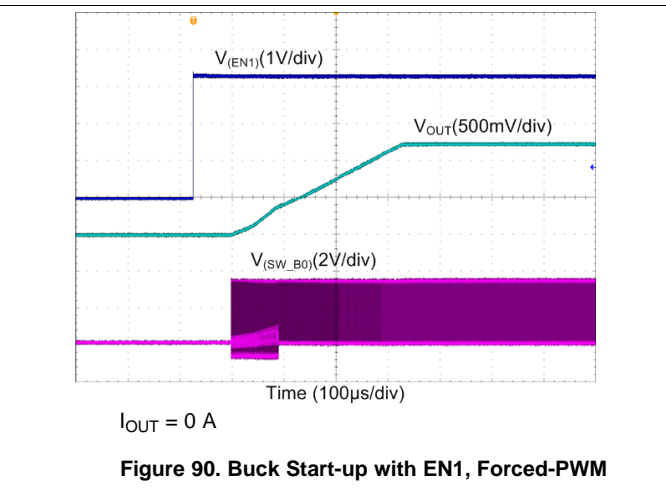
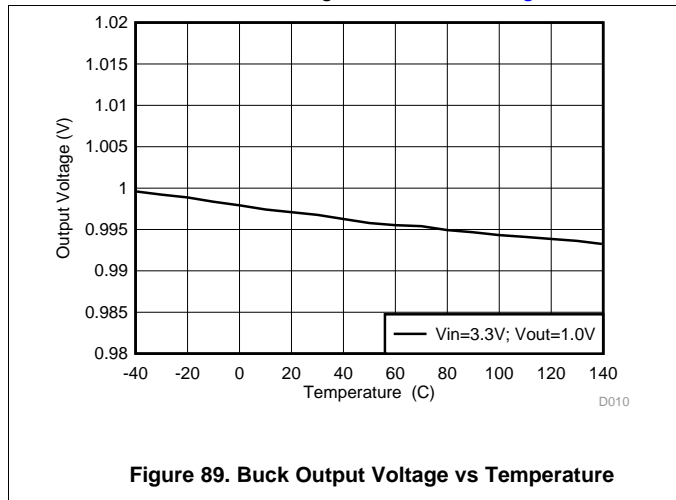
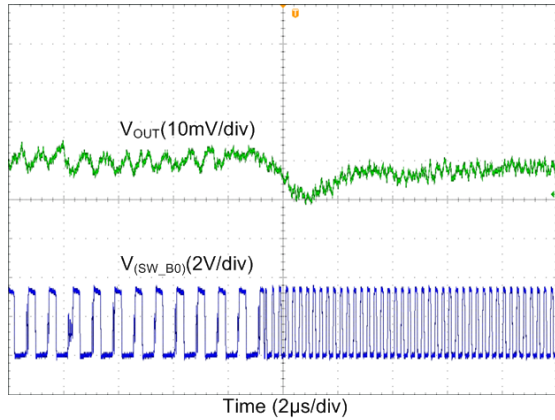


Figure 88. Buck Output Voltage vs Input Voltage in PWM Mode

Unless otherwise specified: $V_{IN} = 3.3\text{ V}$, $V_{OUT_BUCK} = 1\text{ V}$, $V_{OUT_BOOST} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, f_{SW} -setting 4 MHz, $L_0 = L_1 = 0.47\ \mu\text{H}$ (TOKO DFE252012PD-R47M), $L_2 = 1\ \mu\text{H}$ (TFM252012ALMA1R0), C_{OUT_BUCK} , C_{POL_BUCK} , and $C_{OUT_BOOST} = 22\ \mu\text{F}$. Measurements are done using connections in Figure 81.

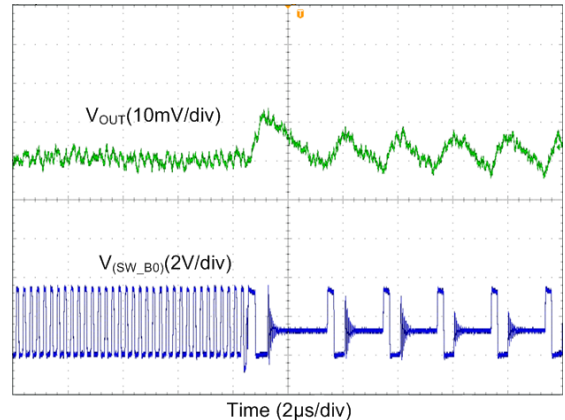


Unless otherwise specified: $V_{IN} = 3.3\text{ V}$, $V_{OUT_BUCK} = 1\text{ V}$, $V_{OUT_BOOST} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, f_{SW} -setting 4 MHz, $L_0 = L_1 = 0.47\text{ }\mu\text{H}$ (TOKO DFE252012PD-R47M), $L_2 = 1\text{ }\mu\text{H}$ (TFM252012ALMA1R0), C_{OUT_BUCK} , C_{POL_BUCK} , and $C_{OUT_BOOST} = 22\text{ }\mu\text{F}$. Measurements are done using connections in [Figure 81](#).



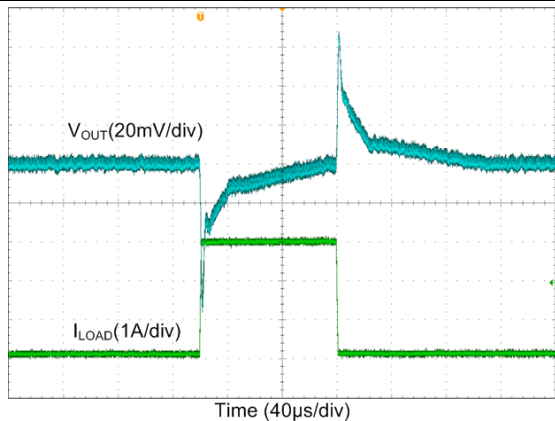
$V_{OUT} = 1.2\text{ V}$

Figure 95. Buck Transient from PFM-to-PWM Mode



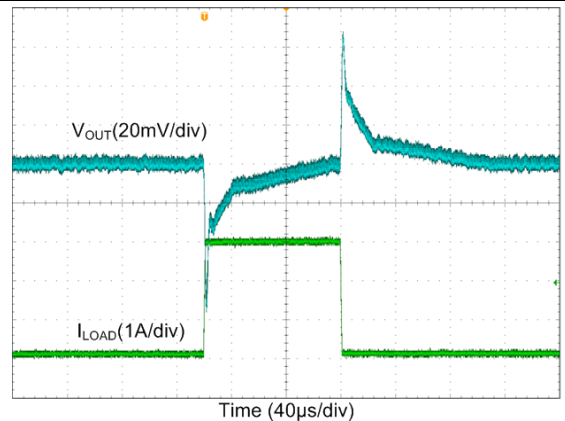
$V_{OUT} = 1.2\text{ V}$

Figure 96. Buck Transient from PWM-to-PFM Mode



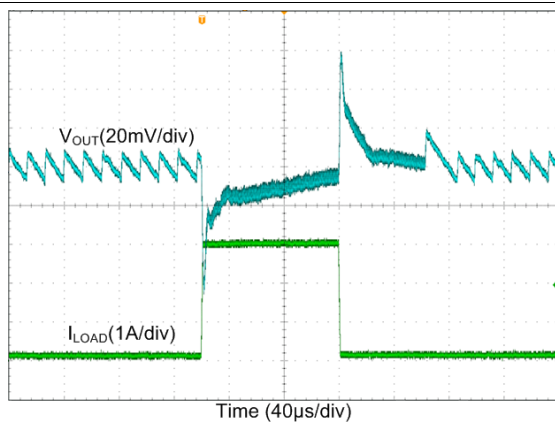
$I_{OUT} = 0\text{ A} \rightarrow 3\text{ A} \rightarrow 0\text{ A}$ $T_R = T_F = 1\text{ }\mu\text{s}$ $V_{OUT} = 1\text{ V}$

Figure 97. Buck Transient Load Step Response, Forced-PWM Mode



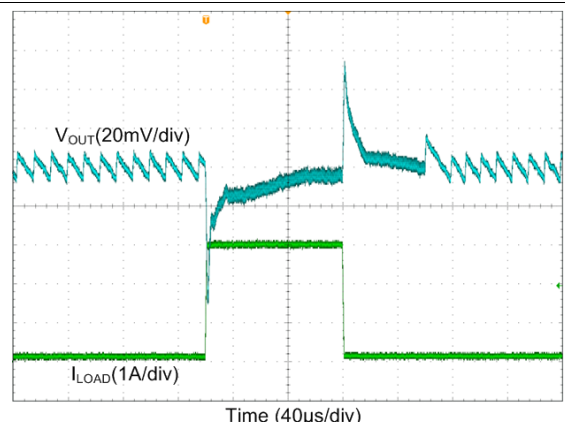
$I_{OUT} = 0\text{ A} \rightarrow 3\text{ A} \rightarrow 0\text{ A}$ $T_R = T_F = 1\text{ }\mu\text{s}$ $V_{OUT} = 1.2\text{ V}$

Figure 98. Buck Transient Load Step Response, Forced-PWM Mode



$I_{OUT} = 0\text{ A} \rightarrow 3\text{ A} \rightarrow 0\text{ A}$ $T_R = T_F = 1\text{ }\mu\text{s}$ $V_{OUT} = 1\text{ V}$

Figure 99. Buck Transient Load Step Response, Auto Mode



$V_{OUT} = 1.2\text{ V}$

Figure 100. Buck Transient Load Step Response, Auto Mode

Unless otherwise specified: $V_{IN} = 3.3\text{ V}$, $V_{OUT_BUCK} = 1\text{ V}$, $V_{OUT_BOOST} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, f_{SW} -setting 4 MHz, $L_0 = L_1 = 0.47\ \mu\text{H}$ (TOKO DFE252012PD-R47M), $L_2 = 1\ \mu\text{H}$ (TFM252012ALMA1R0), C_{OUT_BUCK} , C_{POL_BUCK} , and $C_{OUT_BOOST} = 22\ \mu\text{F}$. Measurements are done using connections in Figure 81.

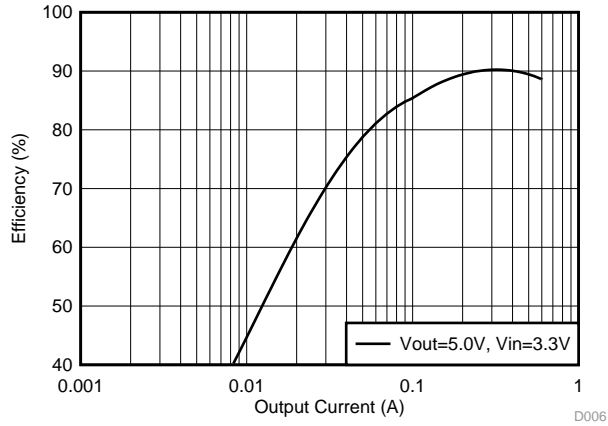


Figure 101. Boost Efficiency

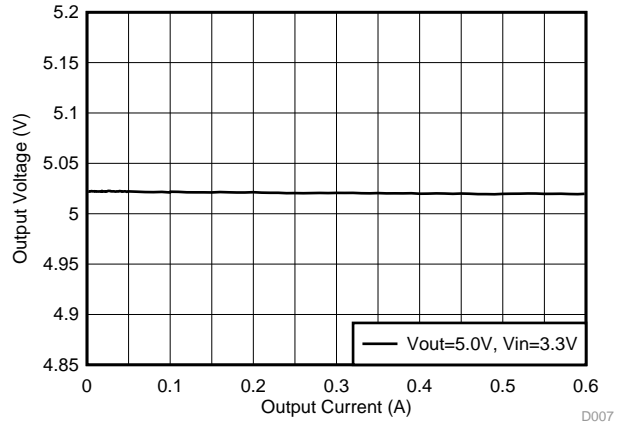
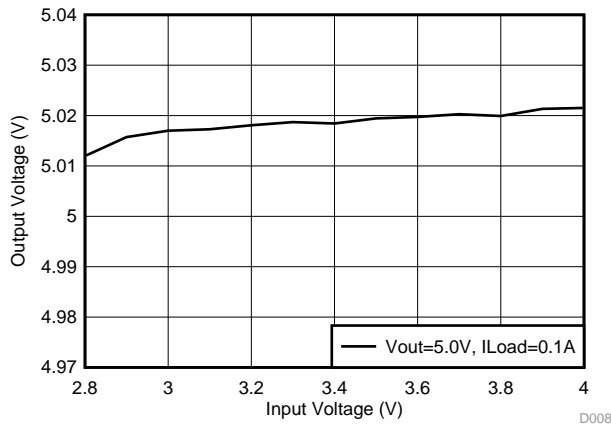
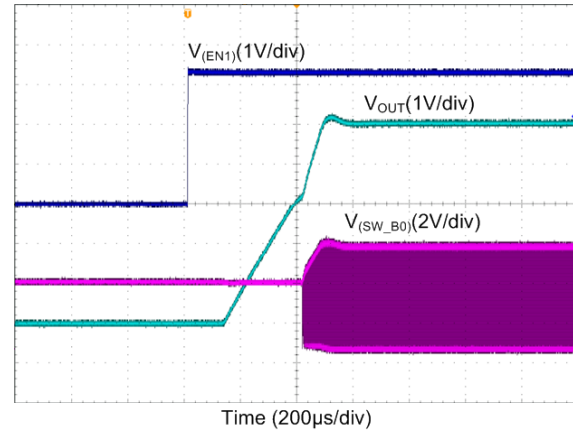


Figure 102. Boost Output Voltage vs Load Current



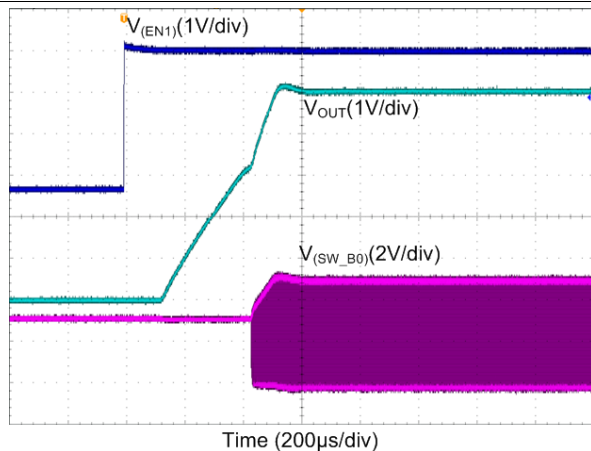
$I_{OUT} = 0.1\text{ A}$

Figure 103. Boost Output Voltage vs Input Voltage



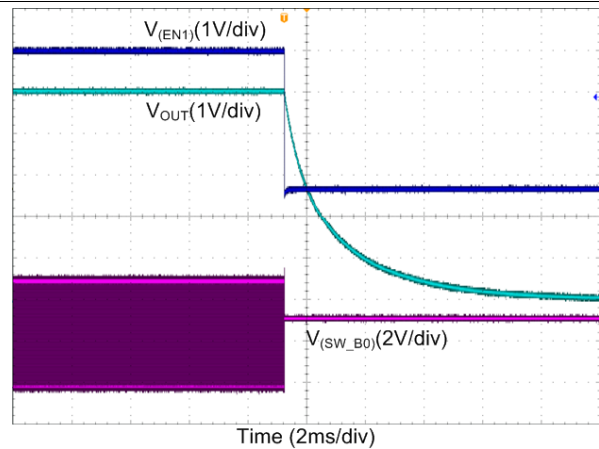
$I_{OUT} = 0\text{ A}$

Figure 104. Boost Start-up With EN1, Forced-PWM



$R_{LOAD} = 50\ \Omega$

Figure 105. Boost Start-up With EN1, Forced-PWM



$R_{LOAD} = 50\ \Omega$

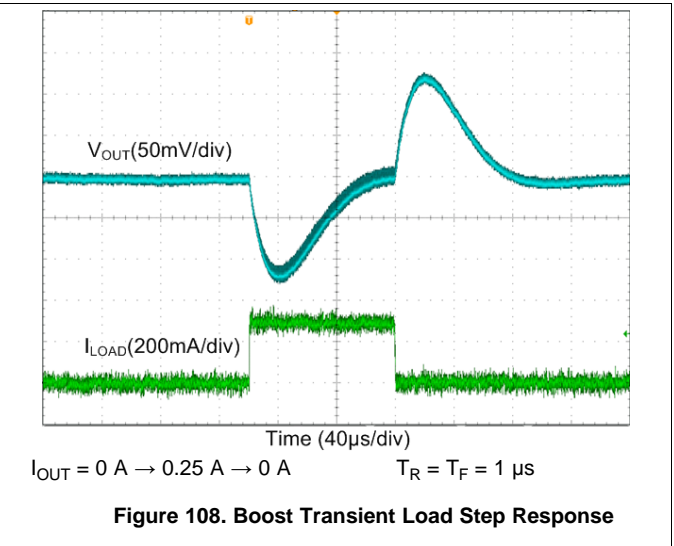
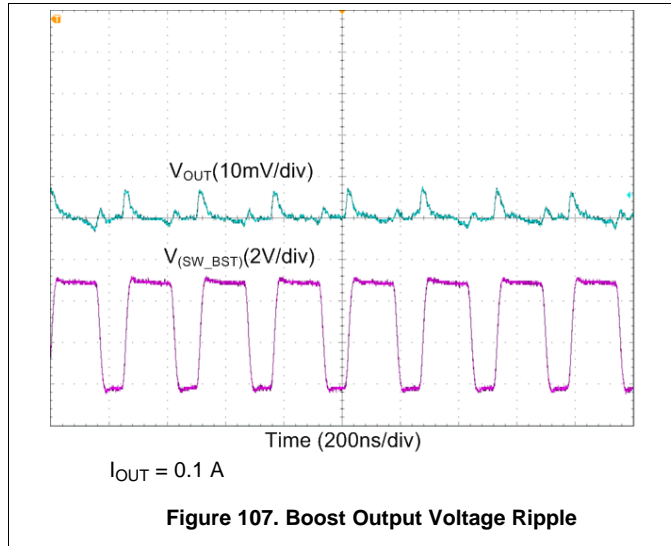
Figure 106. Boost Shutdown With EN1, Forced-PWM

LP87702-Q1

SNVSAL1A – DECEMBER 2017 – REVISED JULY 2018

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Unless otherwise specified: $V_{IN} = 3.3\text{ V}$, $V_{OUT_BUCK} = 1\text{ V}$, $V_{OUT_BOOST} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, f_{SW} -setting 4 MHz, $L_0 = L_1 = 0.47\text{ }\mu\text{H}$ (TOKO DFE252012PD-R47M), $L_2 = 1\text{ }\mu\text{H}$ (TFM252012ALMA1R0), C_{OUT_BUCK} , C_{POL_BUCK} , and $C_{OUT_BOOST} = 22\text{ }\mu\text{F}$. Measurements are done using connections in [Figure 81](#).



9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.8 V and 5.5 V. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high drop in the LP87702-Q1 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP87702-Q1 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high frequency and large switching currents of the LP87702-Q1 make the choice of layout important. Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to several amps, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place C_{IN} as close as possible to the VIN_Bx pin and the PGND_Bx pin. Route the V_{IN} trace wide and thick to avoid IR drops. The trace between the positive node of the input capacitor and device VIN_Bx pin(s) as well as the trace between the negative node of the input capacitor and power PGND_Bx pin(s) must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor - parasitic inductance on these traces must be kept as tiny as possible for proper device operation.
2. The output filter, consisting of L and C_{OUT} , converts the switching signal at SW_Bx to the noiseless output voltage. It should be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the LP87702-Q1's output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) should be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.
4. If remote voltage sensing can be used for the load, connect the device feedback pins FB_Bx to the respective sense pins on the load capacitor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND_Bx, VIN_Bx, and SW_Bx, as well as high bandwidth signals such as the I^2C . Avoid both capacitive as well as inductive coupling by keeping the sense lines short and direct. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible.
5. PGND_Bx, VIN_Bx and SW_Bx should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND_Bx, VIN_Bx and SW_Bx.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ($R_{\theta JA}$) and junction-to-board ($R_{\theta JB}$) thermal resistances and thereby reduces the device junction temperature, T_J . TI strongly recommends performing a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process, by using a thermal modeling analysis software.

10.2 Layout Example

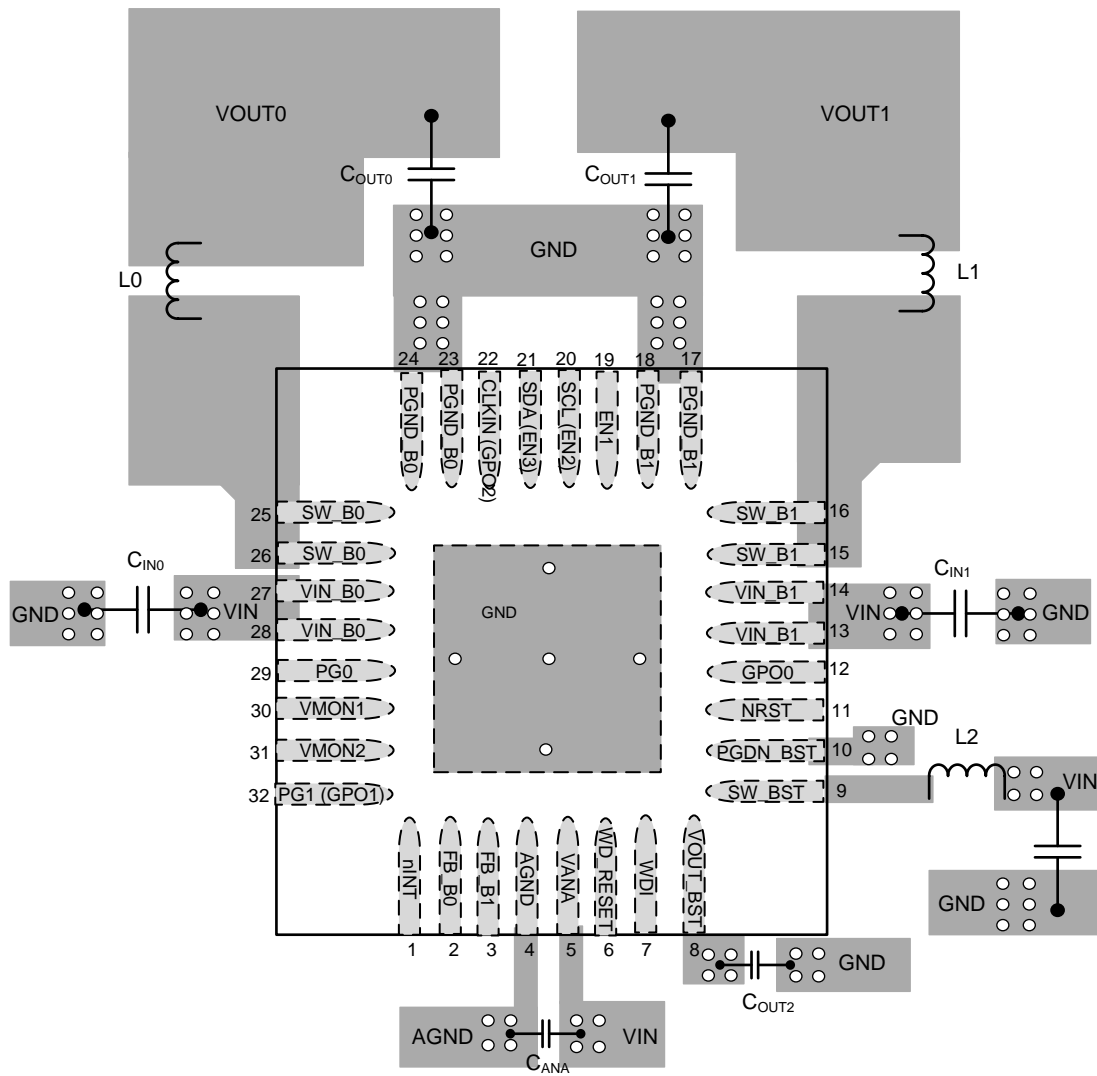


Figure 109. LP87702-Q1 Board Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, go to the device product folder on ti.com. In the upper right corner, click *Alert me* to register for a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

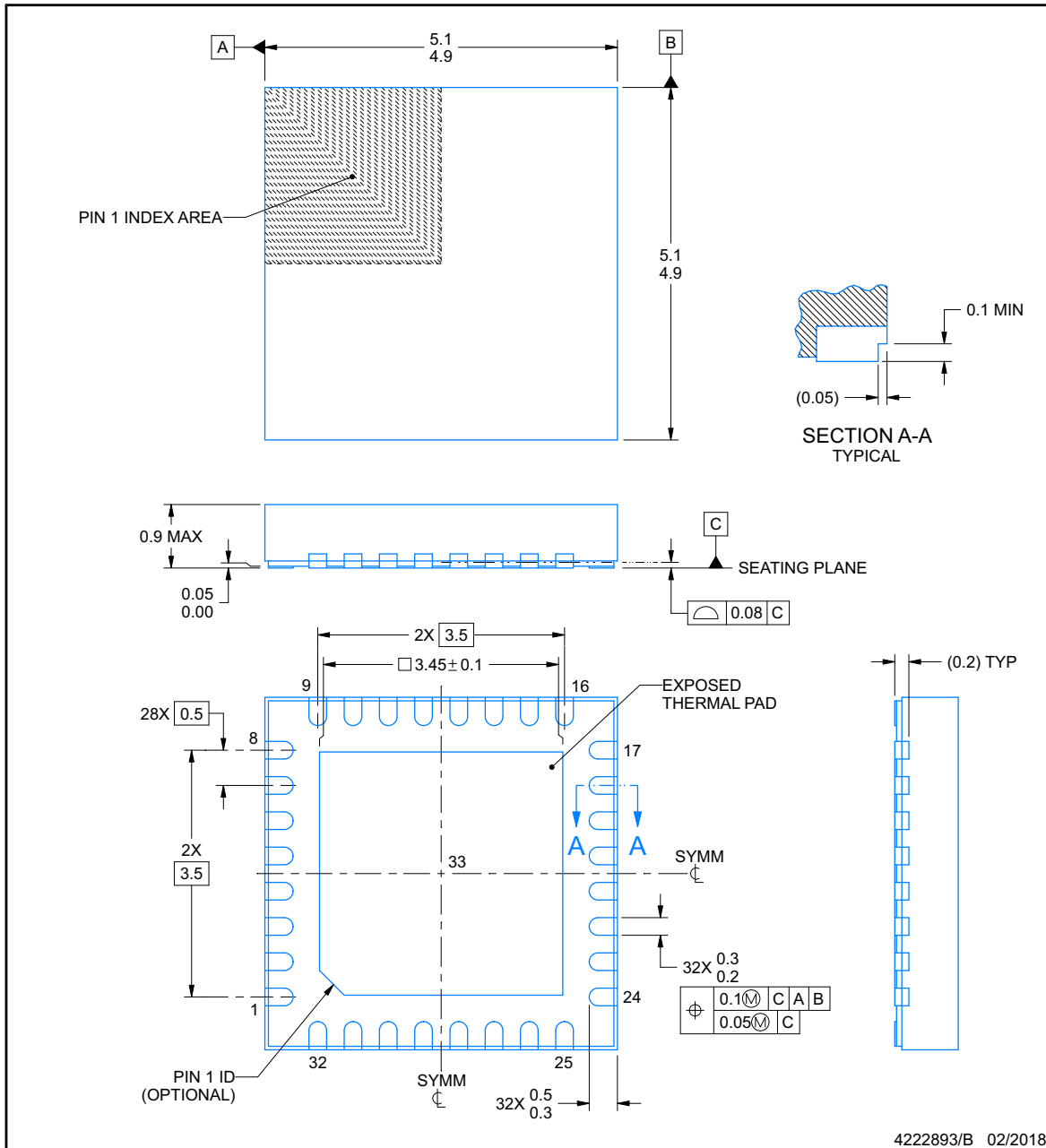


RHB0032N

PACKAGE OUTLINE

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

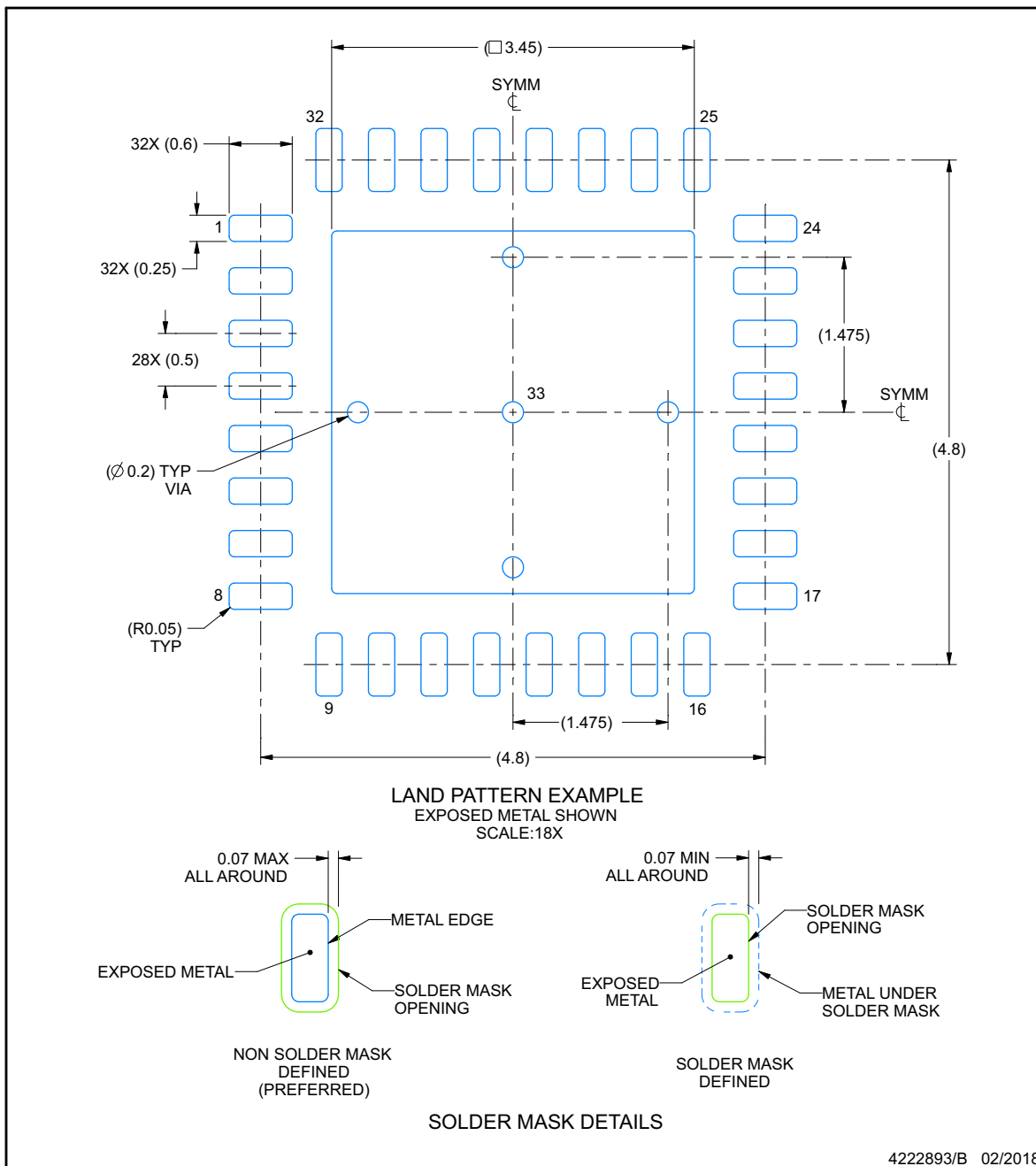
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032N

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

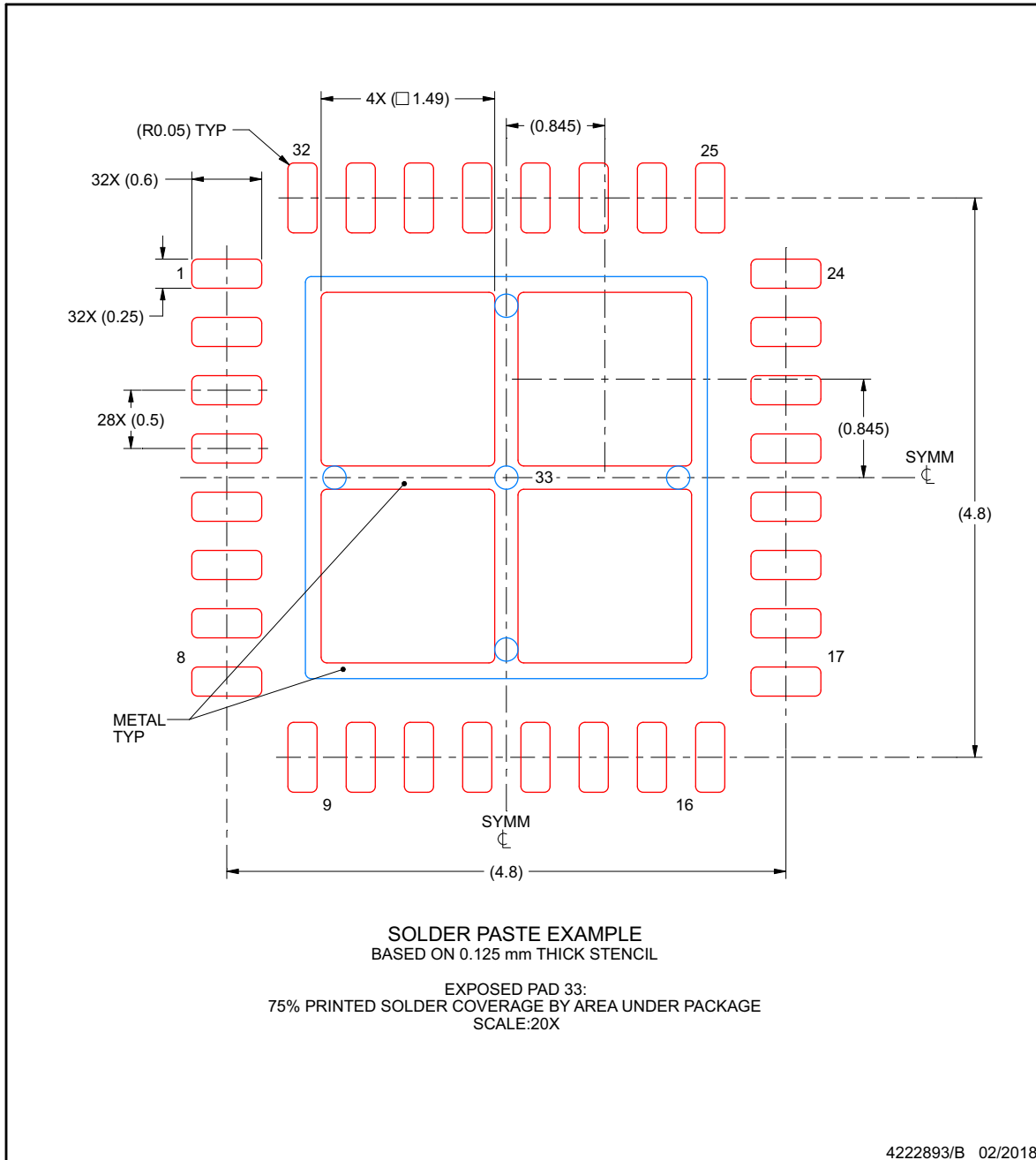
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032N

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP87702DRHBRQ1	PREVIEW	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU	Level-2-260C-1 YEAR	-40 to 125	LP8770Q 2D RHB	
LP87702DRHBTQ1	PREVIEW	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU	Level-2-260C-1 YEAR	-40 to 125	LP8770Q 2D RHB	
P87702DRHBRQ1	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU	Level-2-260C-1 YEAR	-40 to 125	P8770Q 2D RHB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP87702DRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
LP87702DRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP87702DRHBRQ1	VQFN	RHB	32	3000	370.0	355.0	55.0
LP87702DRHBTQ1	VQFN	RHB	32	250	195.0	200.0	45.0

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