Data Sheet | August 23, 2007 | FN6487.1

100V Triple Linear Bias Supply

The ISL6720A is a low cost linear regulator for generating a low voltage bias supply from intermediate distributed voltages commonly used in telecom and datacom applications. It produces three separate outputs, an adjustable 0V to 20V output rated at up to 125mA which can be back-biased from an external source such as an auxiliary transformer winding, a 50mA switched regulated output adjustable between 0V and 15V, and a fixed continuous 5V output rated at 25mA.

The ISL6720A may be used as a start-up or a continuous low power regulator. When operating as a start-up regulator, it is capable of sourcing over 100mA from a 100V source for short durations. This period of time allows the power supply to start-up and provide a low voltage alternate power source, such as the output of a transformer winding, to the VIO output. This allows the remaining outputs to be operated from a lower source voltage thereby minimizing power loss.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6720AARZ*	67 20AARZ	-40 to +105	11 Ld DFN	L11.4x4

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

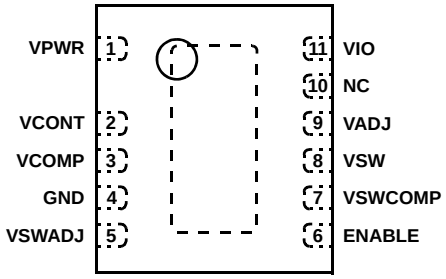
- 100V Input Capability
- Adjustable Auxiliary Winding Regulator with 40V Withstand Capability
- Up to 125mA Combined Output Current on Switched and Unswitched Outputs
- 250µs Delayed Start (VIO, VSW) after Continuous (VCONT) Output
- Regulated Switched (VSW) and Unswitched Outputs (VIO)
- 5V @ 25mA Continuous Output (VCONT)
- 2-Stage Over-Temperature Protection
- Package Compliant with IPC2221A, Creepage and Clearance Spacing Requirements
- Pb-Free Available (RoHS Compliant)

Applications

- Telecom/Datacom DC/DC Converters
- Low Power Bias Supplies

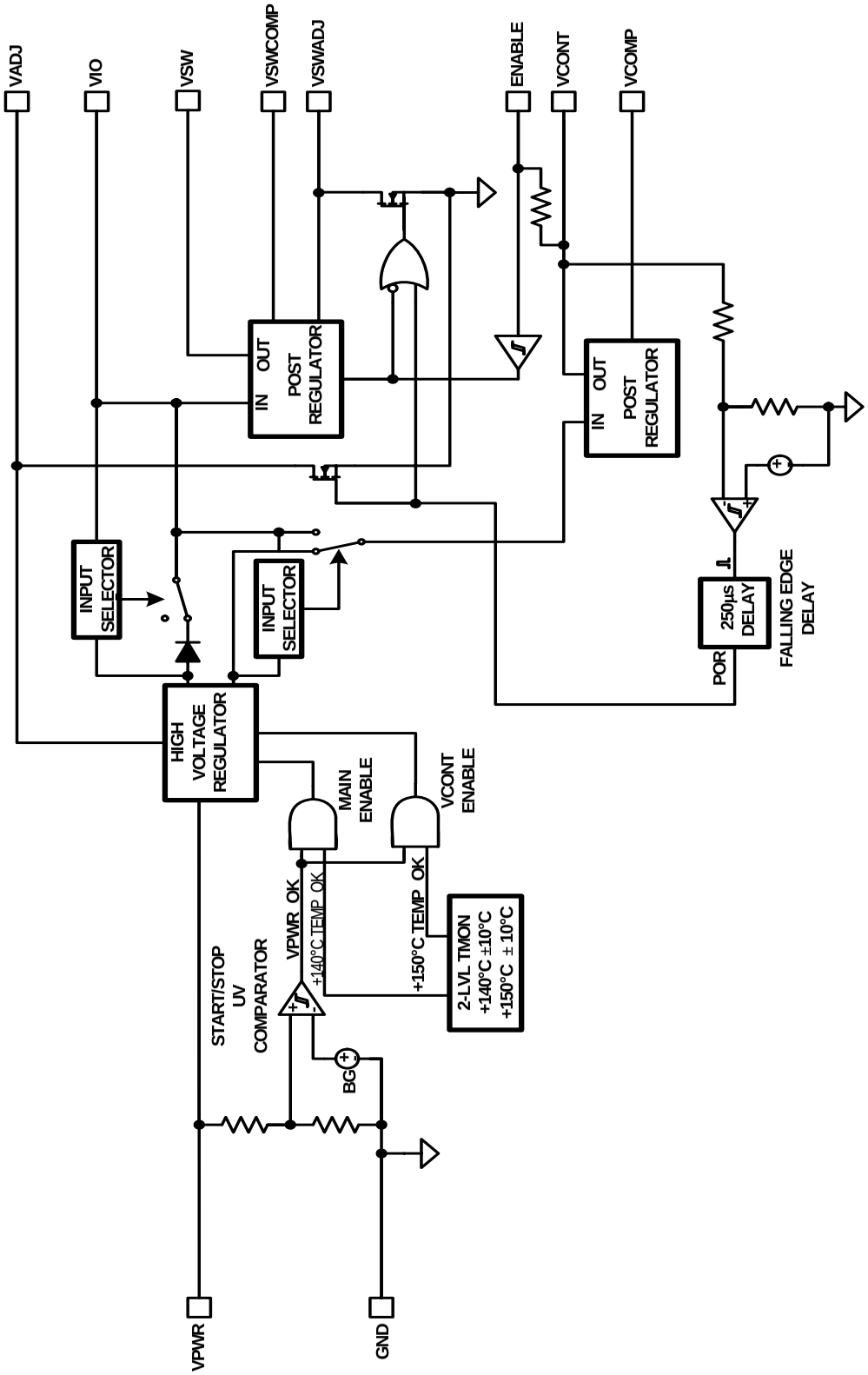
Pinout

ISL6720A
(11 LD DFN)
TOP VIEW

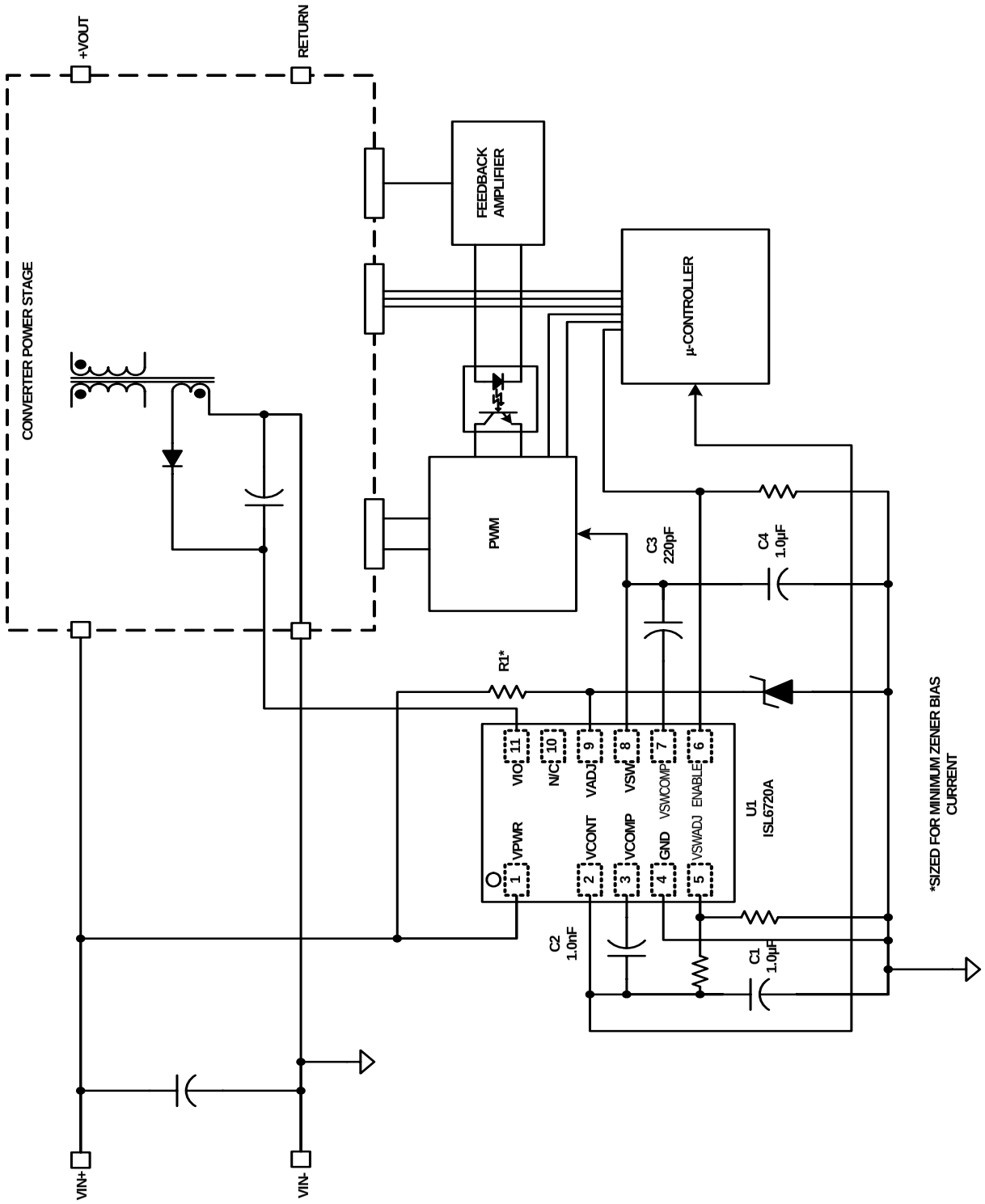


CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Block Diagram



Typical Application



Absolute Maximum Ratings (Note 3)

Supply Voltage, PWR. . . . . GND -0.3V to +105V
VIO, VADJ . . . . . GND -0.3V to +40V
VSW. . . . . GND -0.3V to +23V
All others . . . . . GND -0.3V to +6.0V

Operating Conditions

Temperature Range
ISL6720AARZ. . . . . -40°C to +105°C
Supply Voltage Range (Typical). . . . . 18VDC to 80VDC

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
11 Ld DFN	36	2.0

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Functional Block Diagram” on page 2 and “Typical Application” on page 3. 17 V < VPWR < 100V, $C_{VSW} = C_{VCONT} = 1\mu F$, $I_{VCONT} = -250\mu A$, $I_{VSW} = -500\mu A$, VSW Enabled, T_A = -40°C to +105°C (Note 4), Typical values are at T_A = +25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE, VPWR					
Supply Voltage				100	V
Start-Up Current, I_{PWR}	VPWR = 12V		320	470	µA
Operating Current, I_{PWR}	VSW Enabled, VPWR = 100V I_{VIO} = 0		1.3	1.7	mA
	VSW Disabled, VPWR = 100V, I_{VIO} = 0		1.2	1.7	mA
	VIO Biased Externally at 40V, VSW Enabled, VPWR = 100V I_{VSW} = -50mA, I_{VCONT} = -25mA		1.2	1.7	mA
UVLO START Threshold	VADJ = VSWADJ = 0V, I_{VCONT} = 0mA, VSW Disabled	12.4		16.9	V
UVLO STOP Threshold	VADJ = VSWADJ = 0V, I_{VCONT} = -1mA, VSW Disabled	11.5		15.3	V
Hysteresis	UVLO START to UVLO STOP	0.8	1.2	1.7	V
OUTPUT VOLTAGE VIO					
Overall Accuracy	I_{VIO} = 0mA to -125mA , VADJ = 10V, 20V, VPWR = 48V VSW Disabled	VADJ - 4.5		VADJ - 0.5	V
	I_{VIO} = 0mA to -10mA , VADJ = 10V, 20V, VPWR = 48V VSW Disabled	VADJ - 3.5		VADJ - 0.5	V
Setpoint Range	VPWR = 48V, VSW Disabled, I_{VIO} = 0mA for minimum setpoint I_{VIO} = -125mA for max setpoint	0.5		20.0	V
Source Voltage Headroom	VPWR - VIO, minimum VPWR = 17V, 100V VADJ = 20V, I_{VIO} = -125mA VIO final = 0.95 x VIO initial			5.5	V
Maximum V_{OUT}, Faulted VADJ	VPWR = 48V, 100V VADJ = 40V, VSW Disabled, I_{VIO} = 0mA			23.0	V
VADJ Discharge Device, VOL	VPWR = 12V, I_{VADJ} = 10mA			0.65	V
Operational Current (source)	VPWR = 17V, 100V VADJ = 15V, VSW Disabled VIO remains greater than 10.5V	-125			mA

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Functional Block Diagram” on page 2 and “Typical Application” on page 3. 17 V < VPWR < 100V, C_{VSW} = C_{VCONT} = 1µF, I_{VCONT} = -250µA, I_{VSW} = -500µA, VSW Enabled, T_A = -40°C to +105°C (Note 4), Typical values are at T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit	VPWR = 17V, 48V VADJ = 15V, VSW Disabled	-225	-380	-500	mA
Maximum External Bias	VPWR = 17V, 100V VADJ = 0V, VSWADJ = 0V, VSW Enabled $I_{VIO} \leq$ 1.00mA			40	V
Load Capacitance Range	(Notes 5, 6)	0.1			µF
VADJ Bias Current	VPWR = 100V, VSW Disabled VADJ = 0V, 40V	-75	-25	1	µA
OUTPUT VOLTAGE VSW					
Load Capacitance Range	(Note 5)	0.47	1.0	1.5	µF
Compensation Capacitance	(Note 5)	180	220	260	pF
Overall Accuracy	VPWR = 48V I_{VSW} = -500µA to -50mA VADJ = 0V, VIO = 22V, 40V ext.				
	VSWADJ = 0.471V	-5		+5	%
	VSWADJ = 1.000V	-3		+3	%
	VSWADJ = 2.143V	-3		+3	%
Setpoint Range	VPWR = 48V, VADJ = 0V, VIO = 40V ext.				
	VSWADJ = 0V	0		1.5	V
	VSWADJ = 2.25V	15			V
Source Voltage Headroom, VIO - VSW	VPWR = 21V, VADJ = 0V, VSW = 15V, I_{VSW} = -50mA VIO - VSW VSW final = 0.95 x VSW initial		1.0	1.5	V
Source Voltage Headroom, VPWR - VSW	VIO = 17 V ext., VADJ = 0V, VSW = 15V, I_{VSW} = -50mA VPWR - VSW VSW final = 0.95 x VSW initial			5.5	V
Minimum Required Load				-500	µA
VSWADJ Discharge Device, VOL	VPWR = 48V, I_{VSWADJ} = 10mA VSW Disabled, VADJ = 15V		0.10	0.25	V
Maximum V_{OUT}, Faulted VSWADJ	VSWADJ = 4V, VIO = 40V, I_{VSW} = -50mA	15.1		23	V
VSWADJ DC Gain	VSW = VADJ*G_{VSWADJ}		7		V/V
Long Term Stability	T_A = +125°C, 1000 hours, (Note 5) VPWR = 48V, VSWADJ = 1.0V, I_{VSW} = -50mA, VADJ = 0V, VIO = 40V ext.		0.3		%
Operational Current (source)	VPWR = 48V, VADJ = 0V VIO = 17V ext., VSWADJ = 2.14V	-50			mA
Current Limit	VPWR = 100V, VADJ = 0V VIO = 40V ext.	-80	-225	-300	mA
VSWADJ Bias Current	VPWR = 100V, VIO = 40V ext. VSWADJ = 0V, 5V	-1.0		1.0	µA
OUTPUT VOLTAGE VCONT					
Overall Accuracy	VPWR = 17V, 100V I_{VCONT} = -250µA to -25mA VADJ = 0V, VIO = 10V, 40V ext. T_A = -40 to +105°C	4.925	5.000	5.075	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to “Functional Block Diagram” on page 2 and “Typical Application” on page 3. 17 V < VPWR < 100V, C_{VSW} = C_{VCONT} = 1µF, I_{VCONT} = -250µA, I_{VSW} = -500µA, VSW Enabled, T_A = -40°C to +105°C (Note 4), Typical values are at T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source Voltage Headroom VIO - VCONT	VPWR = 48V, VADJ = 0V VIO biased ext. I_{VCONT} = 0.95 x I_{VIO} + 0.05 x I_{VPWR}				
	I_{VCONT} = -25mA, minimum		3.4	5.0	V
	I_{VCONT} = -5mA, minimum		3.1	4.5	V
Minimum Required Load				-250	µA
Long Term Stability	T_A = +125°C, 1000 hours, (Note 5) VPWR = 100V, VADJ = 0V VSW Disabled, I_{VCONT} = -25mA		0.2		%
Operational Current (source)	VPWR = 17V, VADJ = 0V VSW Disabled	-25			mA
Current Limit	VPWR = 17V, 100V, VADJ = 0V VIO = 0V, 40V ext., VSW Disabled	-30	-95	-150	mA
Output Capacitance	(Note 5)	0.47	1.0	1.5	µF
Compensation Capacitance	(Note 5)	800	1000	1200	pF
ENABLE					
High Level Input Voltage (VIH)	% of VCONT VPWR = 48V, VSWADJ = 2.14V VADJ = 20V, I_{VIO} = 0mA	54	60	66	%
Low Level Input Voltage (VIL)	% of VCONT VPWR = 48V, VSWADJ = 2.14V VADJ = 20V, I_{VIO} = 0mA	34	40	46	%
Hysteresis	% of VCONT VPWR = 48V, VSWADJ = 2.14V VADJ = 20V, I_{VIO} = 0mA	16	20	24	%
Pull-Up Resistance	V_{ENABLE} = 0V		100		kΩ
Turn-On Delay	$t_{VSW,}$ 10% to $t_{ENABLE,}$ 60%	5		50	µs
Turn-Off Delay	$t_{VSW,}$ 90% to $t_{ENABLE,}$ 40%	1		15	µs
POR					
Turn-On Delay	$t_{VCONT,}$10% to t_{VPWR} > UVLO, I_{VCONT} = 0µA	150		500	µs
POR Threshold, VCONT increasing	% of VCONT	70	89	98	%
POR Hysteresis			200		mV
THERMAL PROTECTION					
Thermal Shutdown 1, VSW off, VIO off			140		°C
Thermal Shutdown 1 Clear			95		°C
Hysteresis 1, Internal Protection			45		°C
Thermal Shutdown 2, VCONT off			150		°C
Thermal Shutdown 2 Clear			105		°C
Hysteresis 2, Internal Protection			45		°C

NOTES:

4. Specifications at -40°C and +105°C are guaranteed by +25°C test with margin limits.
5. Limits established by characterization and are not production tested.
6. The maximum load capacitance is limited only by practical considerations. Large values of capacitance combined with high supply voltage (VPWR) may activate the thermal protection prior to reaching steady state operation.

Typical Performance Curves

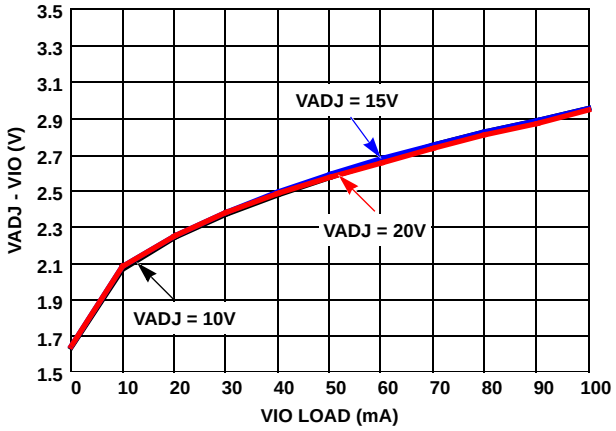


FIGURE 1. VADJ - VIO vs I_{VIO} @ VPWR = 25V, +25°C

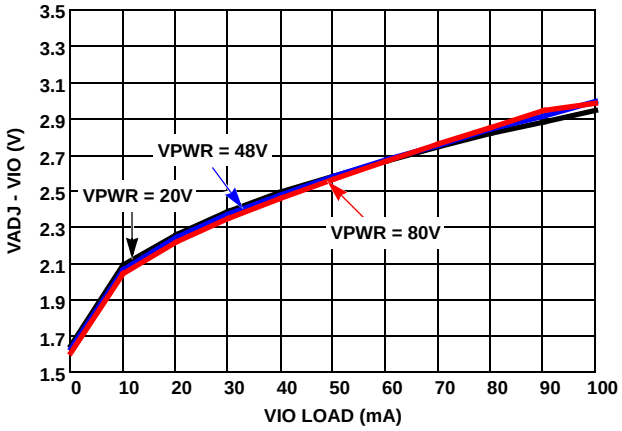


FIGURE 2. VADJ - VIO vs I_{VIO} @ VADJ = 15V, +25°C

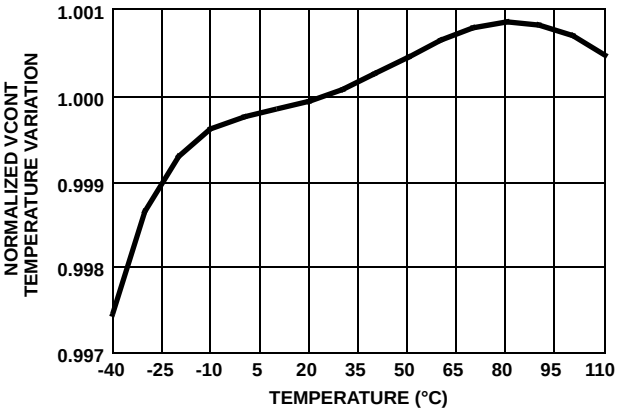


FIGURE 3. VCONT REGULATION vs TEMPERATURE

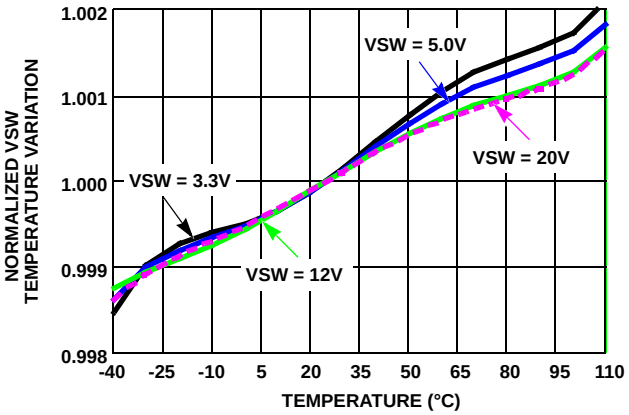


FIGURE 4. VSW REGULATION vs TEMPERATURE

Pin Descriptions

VPWR - VPWR is the primary power connection for the IC. The under voltage lockout (UVLO) feature of VPWR enables/disables all outputs even if VIO is externally biased.

To optimize noise immunity, bypass VPWR to GND with a ceramic capacitor as close to the VPWR and GND pins as possible.

VCONT - A 25mA continuous output that derives its source voltage from either VIO (when enabled and sufficient) or VPWR (when VIO is not available). VCONT sequences on before VIO and VSW by approximately 250µs.

The over-temperature protection feature protects VCONT at a higher temperature than VIO and VSW. This ensures VIO and VSW shutdown at a lower temperature and allows VCONT to remain on.

VCOMP - A 1000pF compensating capacitor is placed between VCOMP and VCONT to stabilize the control loop. This value may vary depending on the output load and capacitance applied between VCONT and GND.

VIO - This is the unswitched low voltage output supply. It may be used as is, or may be back-biased by an auxiliary power source such as a transformer winding. VIO should be bypassed to GND with a 0.1µF capacitor. Although a minimum capacitance is not required, it does provide the source voltage bypass for VSW and VCONT when VIO is capable of supporting those outputs. Smaller values of capacitance will result in larger disturbances during load transients. Its output is adjustable from 0V to 20.0V using a reference on VADJ, such as a zener diode and bias resistor. VIO may be soft-started with a capacitance to ground from VADJ.

VADJ - The feedback adjustment pin for VIO. An external reference on VADJ sets the voltage on VIO. The reference may be a resistor/zener diode combination from VPWR. VADJ has a discharge device that activates momentarily during power-up and power-down sequences to allow VIO to be soft started.

GND - Signal and power ground connections for this device.

VSW - This is the switched regulated low voltage output supply derived from VIO. Bypass to GND with a 1.0µF capacitor. Its output is adjustable from 0V to 15.0V using an appropriate divider from VCONT to VADJ and GND. VSW is nominally 7 x VSWADJ. Protection circuitry prevents the output from exceeding 23V in the event of a fault on VSWADJ (short high). The minimum output current capability is 50mA with transient capability to > 80mA. VSW may be soft-started by placing a capacitor from VSWADJ to GND.

ENABLE - The positive logic on/off control input that controls the VSW output. A logic high enables VSW.

VSWCOMP - A 220pF compensating capacitor is placed between VSWCOMP and VSW to stabilize the control loop. This value may vary depending on the output load and capacitance applied between VSW and GND.

VSWADJ - The feedback adjustment pin for VSW. A divider from VCONT to GND sets the output voltage for VSW. VSWADJ has a node discharge device that activates momentarily at power-up, when disabled (ENABLE low), and during power-down sequences. VSW is nominally 7 x VSWADJ.

Functional Description

Features

The control circuitry used in Telecom/Datacom DC/DC converters often requires an operating bias voltage significantly lower than the source voltage available to the converter. Many applications use a discrete linear regulator from the input source to create the bias supply. Often an auxiliary winding from the power transformer is used to supplement or replace the linear supply once the converter is operating. The auxiliary winding bias voltage may require regulation, as well, to minimize the voltage variation inherent in unregulated transformer winding outputs. When implemented discretely, this circuitry occupies significant PWB area, a considerable problem in today's high density converters.

The ISL6720A triple linear regulator simplifies the start-up and operating bias circuitry needed in Telecom and Datacom DC/DC converters by integrating these functions, and more, in a small 4mmx4mm DFN package.

VIO

VIO is the primary output of the ISL6720A, providing bias voltage whenever the input source voltage, VPWR, is above its under voltage lockout (UVLO) threshold. VIO, which is an abbreviation for "voltage input/output", is adjustable from 0.5V to 20V using the VADJ input, and may be back-biased up to 40V from an external source independent of VPWR. The back-bias voltage must be higher than the VIO setpoint to disable the internal VIO regulator. The transition from internal VIO to external VIO is not abrupt. As the back-bias voltage increases above the VIO setpoint, the load current on VIO gradually transfers from the VIO regulator to external back-bias source. Depending on load, the back-bias voltage may have to exceed the VIO setpoint by as much as 3V before the VIO regulator is off.

The output voltage of VIO is set by applying a reference voltage to VADJ. The reference voltage may be set by using a resistor and zener diode combination from the VPWR input. VIO ranges from 0.5V to 4.5V below the voltage applied to VADJ depending on the load on VIO. VIO can source more than 125mA for short durations, limited only by the device power dissipation and the thermal constraints of the application.

$$VIO = VADJ - V_{OFFSET} \quad V \qquad \text{(EQ. 1)}$$

where V_{OFFSET} ranges from 0.5V to 4.5V.

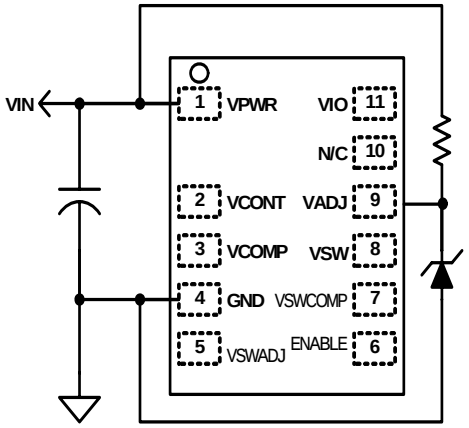


FIGURE 5. SETPOINT ADJUSTMENT FOR VIO

VIO may be soft-started using the VADJ input. By limiting the rate of rise of VADJ, the risetime of VIO may be controlled. Soft-start may be accomplished by placing a capacitor to ground from VADJ. The capacitor to ground and the resistor from VPWR determine the RC charging characteristic for the voltage at VADJ. Since VADJ is pulled low at power-up and power-down, soft-start always starts from a known state. The soft-start rate cannot exceed the intrinsic risetime set by the current limit threshold of the output. As load capacitance increases, the intrinsic risetime increases. In general, placing large capacitance values on VIO should be avoided, particularly if the source voltage applied to VPWR is high. Having a large load capacitance and high input voltage results in high power dissipation for a longer duration and may activate the over-temperature protection before VIO can be biased externally. Under such conditions, steady state operation would not be achievable.

If the auxiliary transformer winding used to back-bias VIO requires a large value of capacitance, it can be isolated from VIO using a diode as shown in Figure 6.

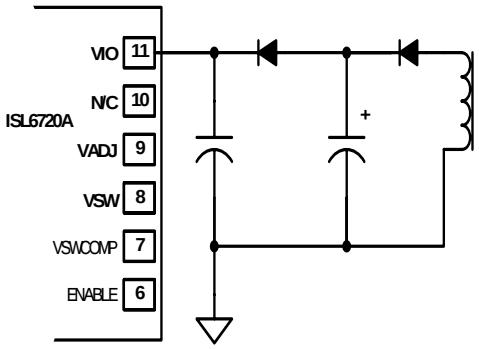


FIGURE 6. ISOLATING VIO FROM LARGE CAPACITANCES

VSW

VSW is the switched output and may be turned on and off using the ENABLE pin (GND = off). The output is adjustable from 1.5V to 15V, but must always be at least 1.5V lower than VIO and 5.5V lower than VPWR. VSW uses VIO as its input source. If the external source applied to VIO is unable to supply adequate voltage, VPWR will be selected as an alternate source for VIO (and VSW). VSW is capable of sourcing up to 50mA continuously, and up to 80mA on a transient basis.

The output voltage is adjusted using the VSWADJ input. The voltage applied to this pin, multiplied by an internal gain of 7, sets the output voltage.

$$VSW = 7 \times VSWADJ \quad V \qquad \text{(EQ. 2)}$$

With a 220pF capacitor from VSW to VSWCOMP, the load capacitance on VSW should be 1.0µF nominal, with a range of 0.47µF to 1.5µF. VSW requires a minimum load of 500µA. These conditions must be met even if the VSW output is not used.

VCONT

VCONT, which has a tight tolerance output and can source 25mA, is a continuos output. It remains on during most fault conditions and precedes VIO and VSW during power-up. It may be used as reference for other circuitry, or may be used to power a micro-controller or other similar device.

VCONT selects VIO as its primary source voltage, but also uses VPWR if VIO is not present or capable.

VIO must have at least 5V of headroom above VCONT or VPWR is selected as the source. VCONT is enabled when VPWR exceeds its UVLO threshold and its operation precedes the enabling of VIO and VSW by 250µs, nominal.

VCONT requires a minimum 250µA load for stability. It should be bypassed to GND with a 1µF capacitor and requires a 1nF compensation capacitor between VCOMP and VCONT. These conditions must be met even if the VCONT output is not used.

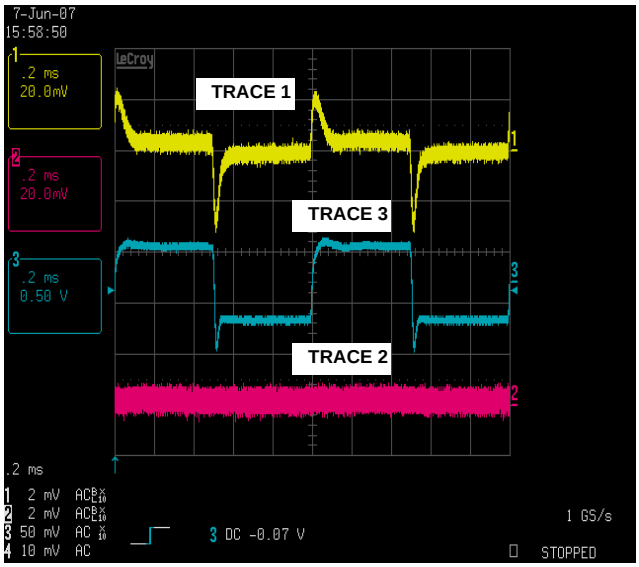


FIGURE 7. VSW TRANSIENT RESPONSE, 0mA to 50mA STEP, TRACE1: VSW, TRACE2: VCONT, TRACE3: VIO

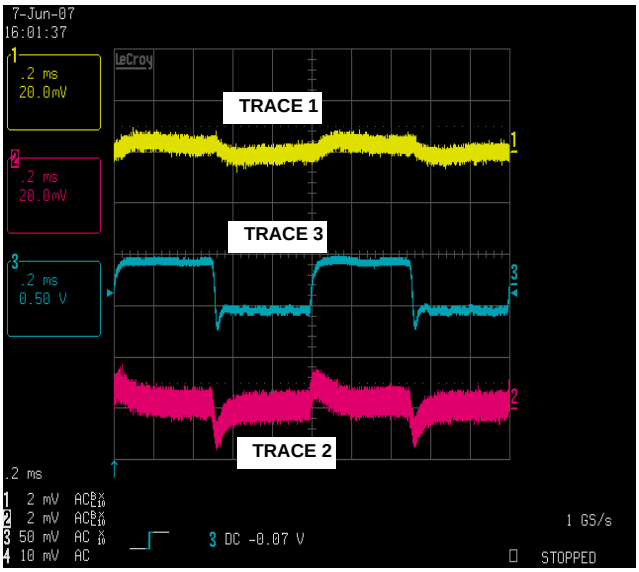


FIGURE 8. VCONT TRANSIENT RESPONSE, 0mA to 25mA STEP, TRACE1: VSW, TRACE2: VCONT, TRACE3: VIO

Figure 7 depicts the output deviation on each output when VSW experiences a 0mA to 50 mA step load. VIO Is unloaded without back-bias and VCONT has a 250µA (minimum) load.

Figure 8 depicts the output deviation on each output when VCONT experiences a 0mA to 25mA step load. VIO Is unloaded without back-bias and VSW has a 500µA (minimum) load.

Over-Temperature Protection

The ISL6720A has a two-stage over-temperature shutdown mechanism. VIO and VSW shutdown approximately +10°C lower than VCONT. The hysteresis for both thresholds is large so that the IC has sufficient time to operate at start-up loading levels without prematurely re-triggering the over temperature protection. At rated load on each output, a +105°C junction temperature, and with VPWR at 80V, the thermal mass combined with the over-temperature thresholds allows approximately 10ms of start-up time.

VPWR

VPWR provides the source voltage for the IC and load until VIO is back biased. The IC is disabled (all outputs off) when UVLO is active.

If the application requires high currents or longer start-up times than the thermal protection allows, the device dissipation may be reduced by adding a resistor or resistors in series between the input voltage and VPWR. The dropping resistance must be selected such that VPWR remains above the UVLO threshold of VPWR and at least 5.5V greater than VIO under maximum load and minimum input voltage to maintain regulation.

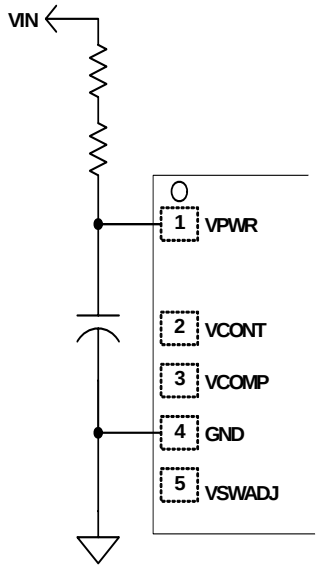


FIGURE 9. ADDING DROPPING RESISTORS TO VPWR

PWB Layout Requirements

Careful layout is essential for satisfactory operation of the device. In particular, the compensation capacitors must be connected to VCOMP and VSWCOMP with short trace lengths.

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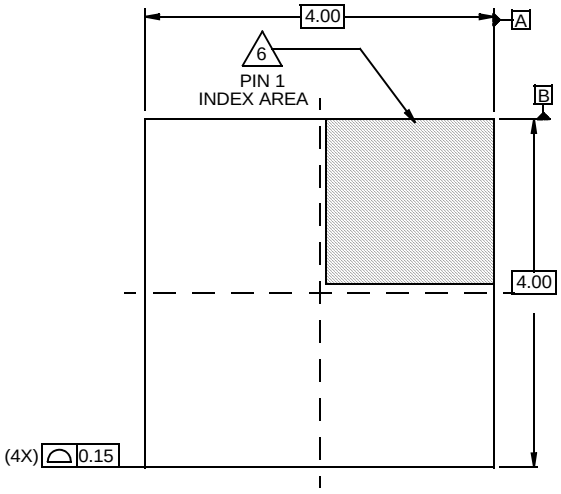
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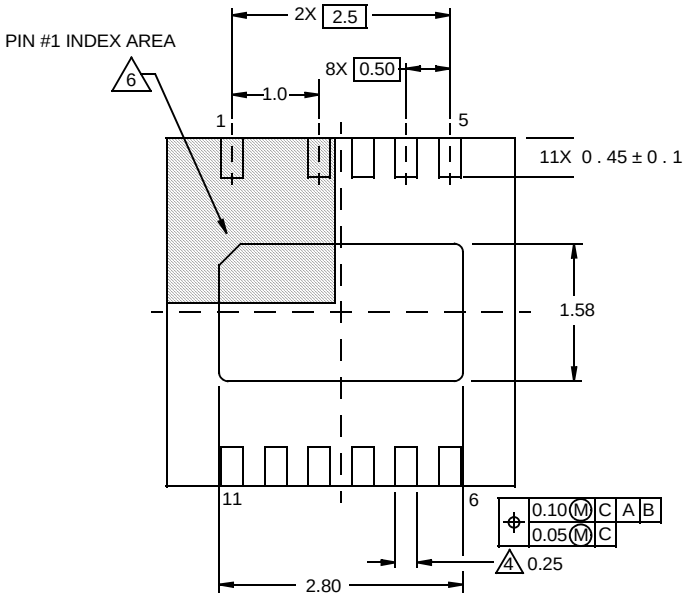
Package Outline Drawing

L11.4x4

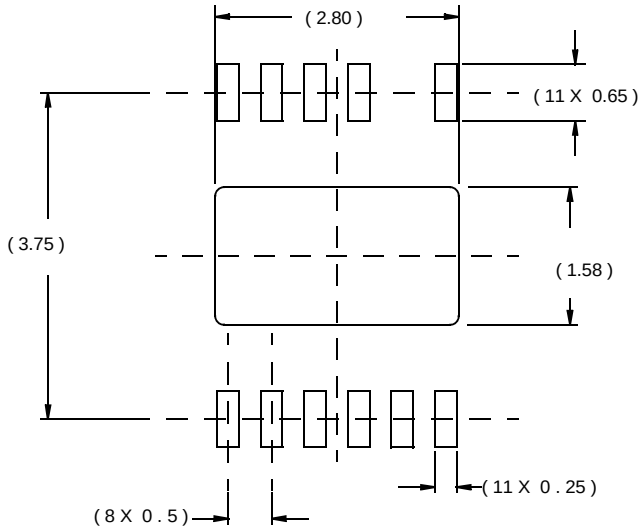
11 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 6/07



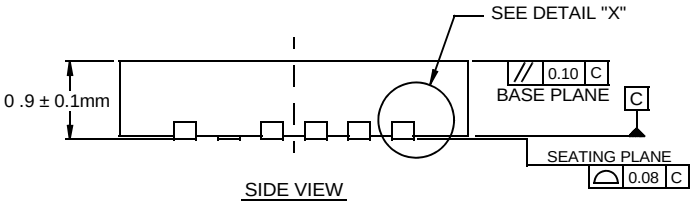
TOP VIEW



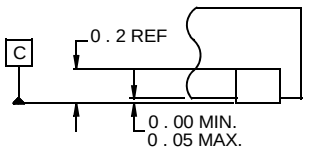
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.