2A DDR Termination Regulator

FEATURES

- Source and sink current capability of 2A
- Low output voltage offset, ±20mV
- High accuracy output voltage at full-load
- V_{OUT} adjustable by external resistors
- Low external component count
- Current limit protection
- Thermal protection
- SO-8 and TO-252-5 packages

APPLICATIONS

- Mother Boards
- Graphic Cards
- DDR Termination Voltage Supply - supports DDR1 (1.25V_{TT}), DDR2 (0.9V_{TT}), and meets JEDEC SSTL-2 and SSTL-3 term. specifications

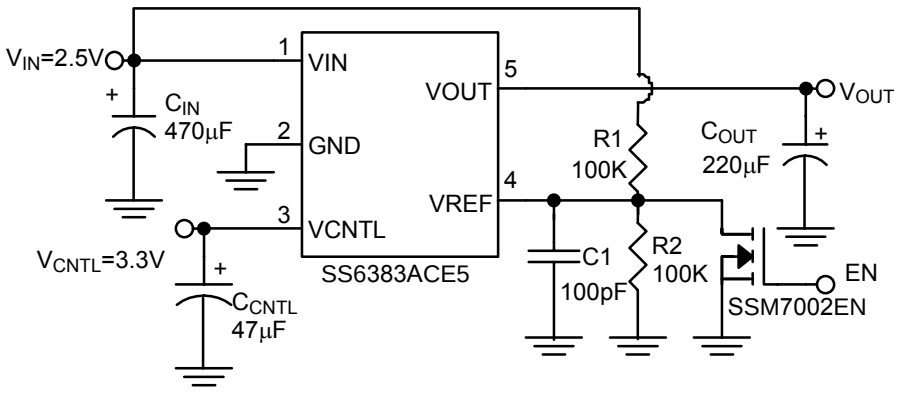
DESCRIPTION

The SS6383A linear regulator is designed to provide 2A source and sink current while regulating an output voltage to within 20mV.

The SS6383A converts voltage supplies ranging from 1.6V to 6V into an output voltage that is set by two external voltage-divider resistors. It provides an excellent voltage source for active termination schemes for high-speed transmission lines such as those seen in high-speed memory buses.

The built-in current-limiting in source and sink mode, together with thermal shutdown, provides maximum protection to the SS6383A against fault conditions.

TYPICAL APPLICATION CIRCUIT



This device is available with Pb-free lead finish (second-level interconnect) as SS6383AGxx

ORDERING INFORMATION

SS6383AXXX XX

- Packing
  - TR: Tape and reel
- Package type
  - CE5: TO-252-5, commercial
  - GE5: TO-252-5, Pb-free, commercial
  - CS: SO-8, commercial
  - GS: SO-8, Pb-free, commercial

Example: SS6383AGE5TR

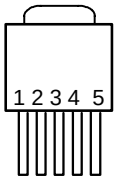
→ in TO-252-5 package, Pb-free lead finish, shipped on tape and reel

PIN CONFIGURATION

TO-252-5

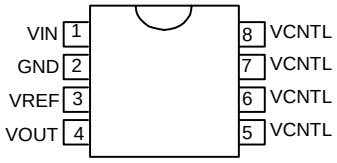
TOP VIEW

1: VIN
2: GND
3. VCNTL
4. VREF
5: VOUT



SO-8

TOP VIEW

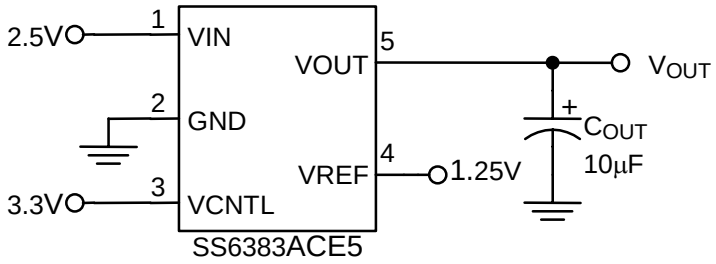


ABSOLUTE MAXIMUM RATINGS

Supply Voltage		-0.4V to 7V
Operating Temperature Range		-40°C~85°C
Storage Temperature Range		-65°C ~150°C
Lead Temperature (Solder, 10sec)		260°C
Thermal Resistance θ_{JC}	TO-252	12.5°C /W
	SO-8	40°C /W
Thermal Resistance θ_{JA}	TO-252	100°C /W
(Assumes no ambient airflow, no heatsink)	SO-8	160°C /W

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

(V_{CNTL}=3.3V, V_{IN}=2.5V, V_{REF}=0.5V_{IN}, C_{OUT}=10µF, T_A=25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Voltage (DDR1/2)	Keep $V_{CNTL} \geq V_{IN}$ during power on and off sequences	V_{IN}	1.6	2.5/1.8		V
		V_{CNTL}	3.0	3.3	6	
Output Voltage	I_{OUT} = 0mA	V_{OUT}		V_{REF}		V
Output Voltage Offset	I_{OUT} = 0mA	V_{OS}	-20		20	mV
Load Regulation (DDR1/2)	I_{OUT} =0.1mA ~ +2A	ΔV_{LOR}		10	20	mV
	I_{OUT} =0.1mA ~ -2A			10	20	
Quiescent Current	V_{REF}<0.2V, V_{OUT} = OFF	I_Q		8	30	µA
Operating Current of V_{CNTL}	No load	I_{CNTL}		3	10	mA
V_{REF} Bias Current	V_{REF}=1.25V		0		1	µA
Current Limit		I_{IL}	2.2	3	4.5	A
THERMAL PROTECTION						
Thermal Shutdown Temperature	3.3V≤V_{CNTL}≤5V	T_{SD}	125	150		°C
Thermal Shutdown Hysteresis	Guaranteed by design			30		°C
SHUTDOWN SPECIFICATIONS						
Shutdown Threshold	Output ON (V_{REF}=0V→1.25V)		0.8			V
	Output OFF (V_{REF}=1.25V→0V)				0.2	

Note 2: V_{OS} is the voltage measurement, which is defined as the difference between V_{OUT} and V_{REF}.
Note 3: Load regulation is measured at constant junction temperature, using pulse testing with a low ON time.
Note 4: Current limit is measured by pulsing a short time.
Note 5: To operate the system safely; V_{CNTL} must be always greater than V_{IN}.
Note 6: Specifications are guaranteed by Statistical Quality Controls (SQC), and not production tested, within the operating temperature range of -40°C to 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS

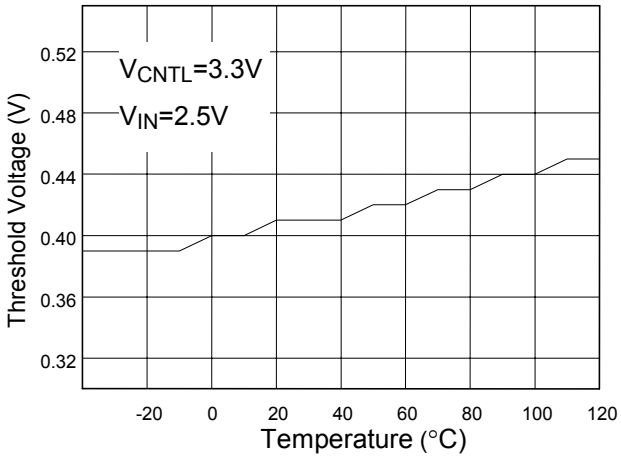


Fig. 1 Turn-On Threshold vs. Temp.

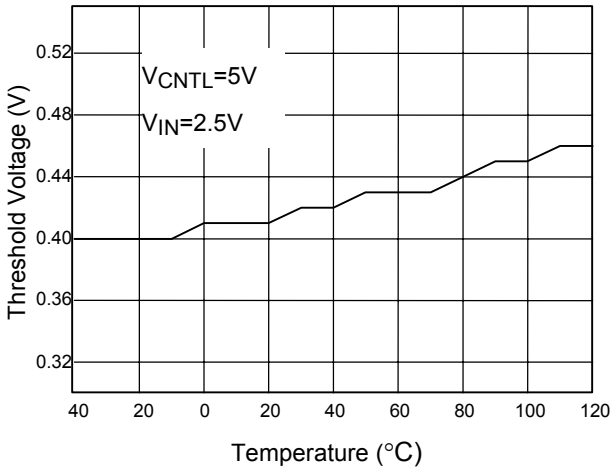


Fig. 2 Turn On Threshold vs. Temp.

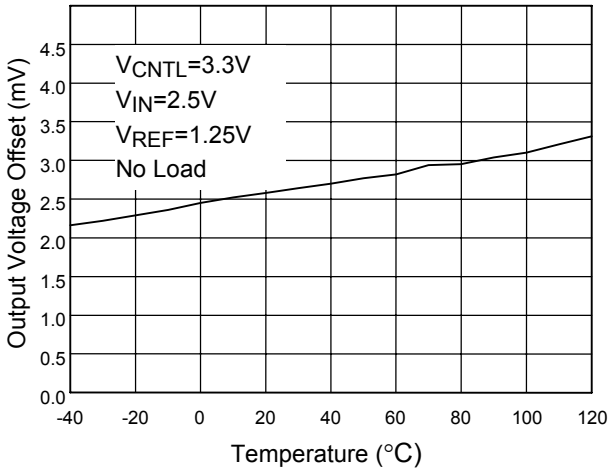


Fig. 3 Output Voltage Offset vs. Temp.

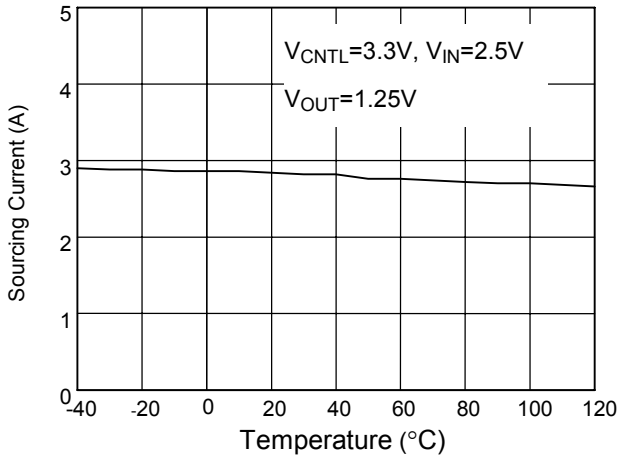


Fig. 4 Current-Limit (Sourcing) vs. Temp.

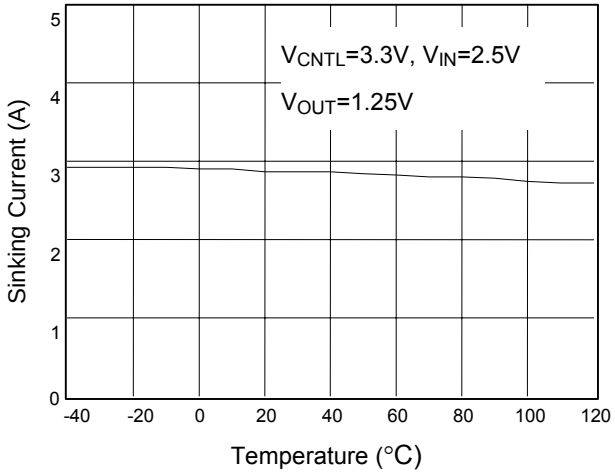


Fig. 5 Current Limit (Sinking) vs. Temp.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

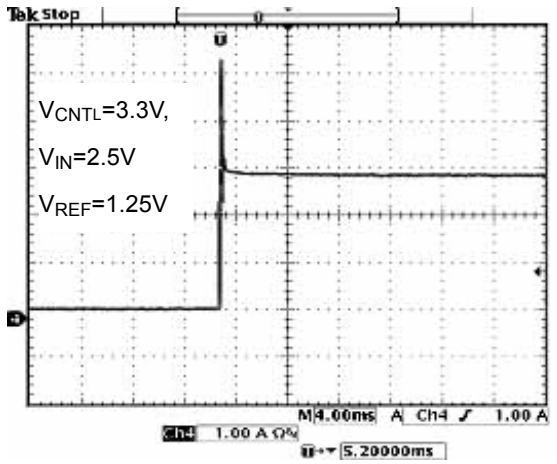


Fig. 6 Output Short-Circuit (Sinking)

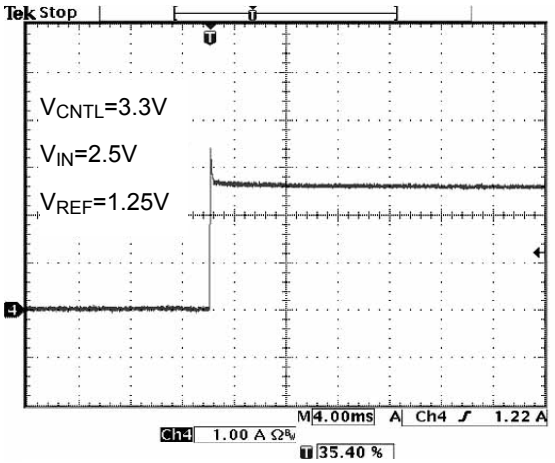


Fig.7 Output Short-Circuit (Sourcing)

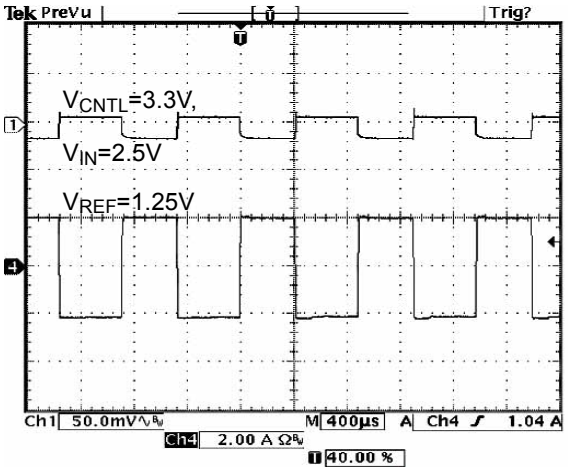


Fig.8 Transient Response at $1.25V_{TT}$/2A

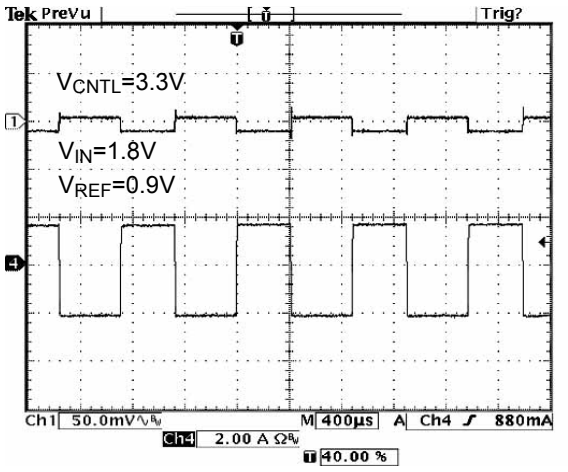
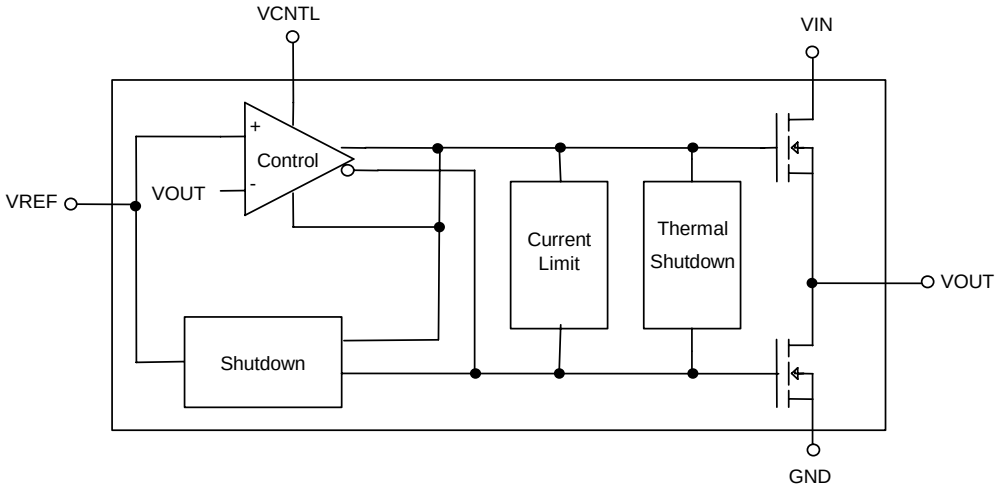


Fig. 9 Transient Response at $0.9V_{TT}$/2A

BLOCK DIAGRAM



PIN DESCRIPTIONS (TO-252-5)

PIN 1: VIN - Input supply pin. It provides main power to create the external reference voltage by divider resistors for regulating V_{REF} and V_{OUT}.

PIN 2: GND - Ground pin.

PIN 3: VCNTL - Input supply pin. It is used to supply all the internal control circuitry.

PIN 4: VREF - Reference voltage input. Pull this pin low to shutdown device.

PIN 5: VOUT - Output pin.

APPLICATION INFORMATION

Layout Consideration

As the SS6383A is in SO-8 and TO-252-5 packages, it is unable to dissipate heat easily when it operates at high current. To avoid exceeding the maximum junction temperature, a suitable copper area must be used.

The large copper area shown at V_{CNTL} pins is able to relieve the thermal dissipation. Using the via to direct heat into the large copper area shown on the bottom layer also helps significantly.

All capacitors should be placed as close as possible to the relevant pins.

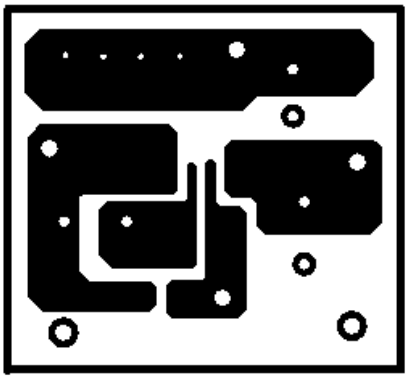


Figure 10. Top layer

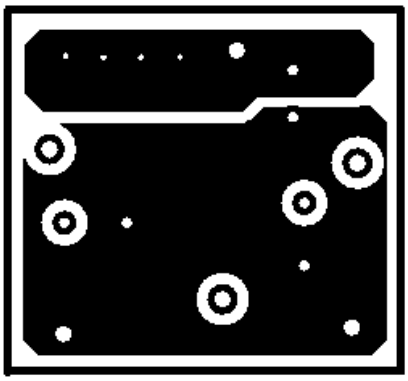


Figure 11. Bottom layer

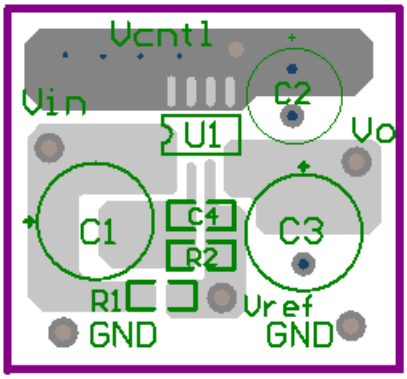
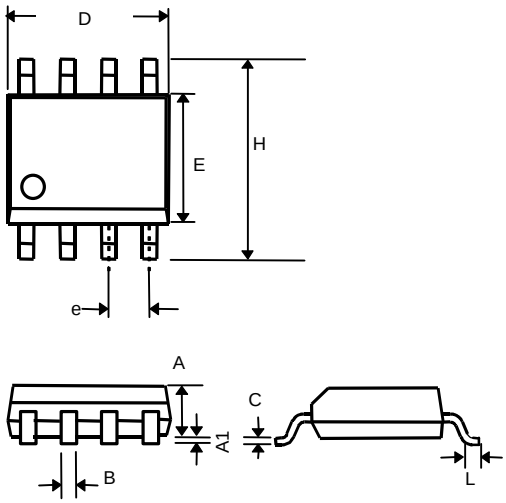


Figure 12. Placement

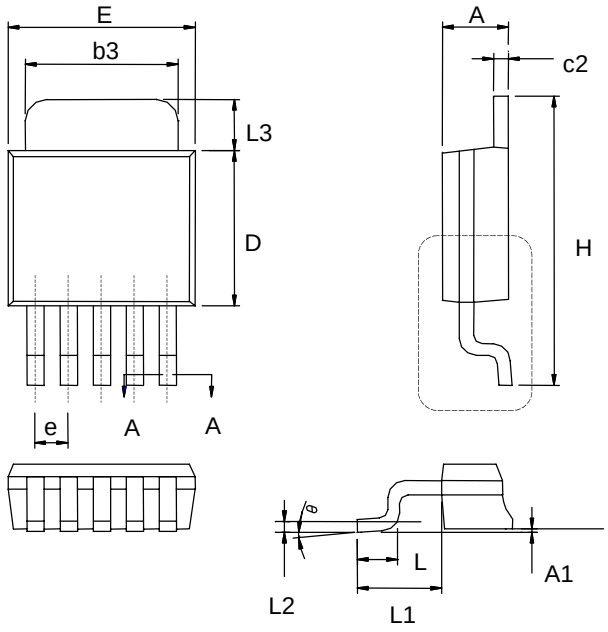
PHYSICAL DIMENSIONS

SO-8



SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27(TYP)	
H	5.80	6.20
L	0.40	1.27

TO-252-5



SYMBOL	MIN	MAX
A	2.19	2.38
A1	0	0.13
b3	5.21	5.46
c2	0.46	0.58
D	5.33	5.59
E	6.35	6.73
e	1.27 BSC	
H	9.40	10.41
L	1.4	1.78
L1	2.67 REF	
L2	0.51 BSC	
L3	1.52	2.03
θ	0°	8°