1 PRODUCT OVERVIEW

SAM87 PRODUCT FAMILY

Samsung's SAM87 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture
— Selectable CPU clock sources
— Release of Idle and Stop power-down modes by interrupt
— Built-in basic timer circuit with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of six CPU clocks) can be assigned to specific interrupt levels.

S3C8847/C8849/P8849 MICROCONTROLLERS

The S3C8847 microcontroller has a 24-Kbyte on-chip program memory and the S3C8849 has a 32-Kbyte. Both chips have a 272-byte general-purpose internal register file. The interrupt structure has nine interrupt sources with nine interrupt vectors. The CPU recognizes seven interrupt priority levels.

Using a modular design approach, the following peripherals were integrated with the SAM87 core to make the S3C8847/C8849/P8849 microcontrollers suitable for use in color television and other types of screen display applications:

— Four programmable I/O ports (26 pins total: 16 general-purpose I/O pins; 10 n-channel, open-drain output pins)
— 4-bit resolution A/D converter (4 channels)
— 14-bit PWM output (Two channels: push-pull type, open-drain type)
— Basic timer (BT) with watchdog timer function
— One 8-bit timer/counter (T0) with interval timer and PWM mode
— One 8-bit general-purpose timer/counter (TA) with prescalers
— On-screen display (OSD) with a wide range of programmable features, including halftone control signal output

The S3C8847 and the S3C8849 are available in versatile 42-pin SDIP package.

OTP

The S3C8847/C8849 microcontrollers are also available in OTP (One Time Programmable) version, named the S3P8849. The S3P8849 microcontroller has an on-chip 32-Kbyte one-time-programmable EPROM instead of a masked ROM. The KS88P8432 is comparable to the S3C8847/C8849, both in function and pin configuration.

FEATURES

CPU

- SAM87 CPU core

Memory

- 24-Kbyte (S3C8847) or 32-Kbyte (S3C8849) internal program memory
- 272-byte general-purpose register area

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 750 ns (minimum) with an 8 MHz CPU clock

Interrupts

- 9 interrupt sources with 9 vectors
- 7 interrupt levels
- Fast interrupt processing for select levels

General I/O

- Four I/O ports (26 pins total)
- Six open-drain pins for up to 6 V loads
- Four open-drain pins for up to 5 V loads

8-Bit Basic Timer

- Three selectable internal clock frequencies
- Watchdog or oscillation stabilization function

Timer/Counters

- One 8-bit timer/counter (T0) with three internal clocks or an external clock and interval timer mode or PWM mode.
- One general-purpose 8-bit timer/counters with interval timer mode (timer A)

A/D Converter

- Four analog input pins; 4-bit resolution
- 3.125 µs conversion time (8 MHz CPU clock)

Pulse Width Modulation Module

- 14-bit PWM with two-channel output (push-pull type, open-drain type)
- 8-bit PWM with four-channel, push-pull and open-drain
- PWM counter and data capture input pin
- Frequency: 5.859 kHz to 23.437 kHz with a 6 MHz CPU clock

On-Screen Display (OSD)

- Video RAM: 252 × 13-bits
- Character generator ROM: 384 × 18 × 16-bits (384 display characters; fixed; 2, variable; 382)
- 252 display positions (12 rows × 21 columns)
- 16-dot × 18-dot character resolution
- 16 different character sizes
- Eight character colors
- Vertical direction fade-in/fade-out control
- Eight colors for character and frame background
- Halftone control signal output; selectable for individual characters
- Synchronous polarity selector for H-sync and V-sync input

Oscillator Frequency

- 5 MHz to 8 MHz external crystal oscillator
- Maximum 8 MHz CPU clock

Operating Temperature Range

- – 20°C to + 85°C

Operating Voltage Range

- 4.5 V to 5.5 V

Package Type

- 42-pin SDIP

BLOCK DIAGRAM

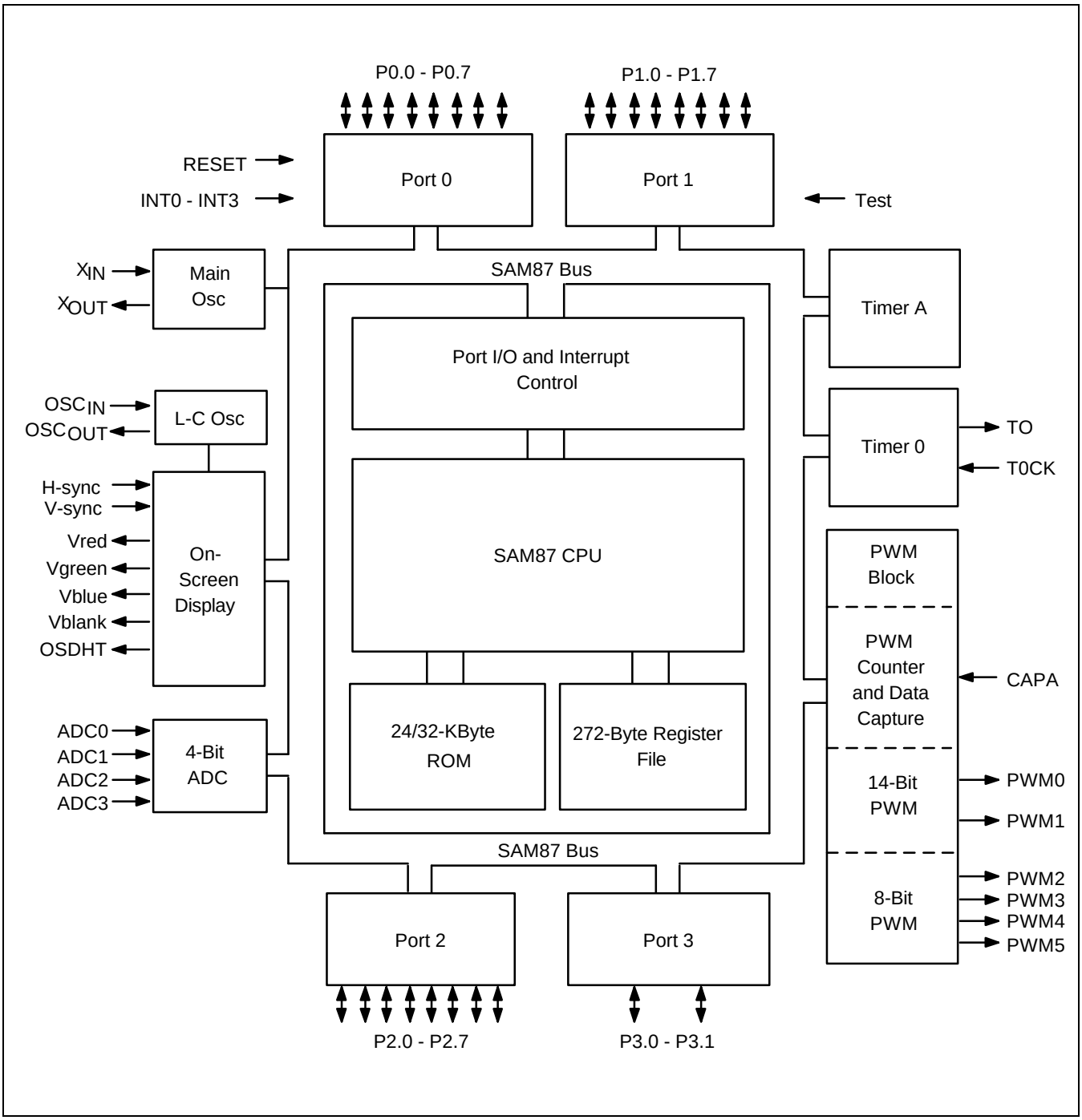


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

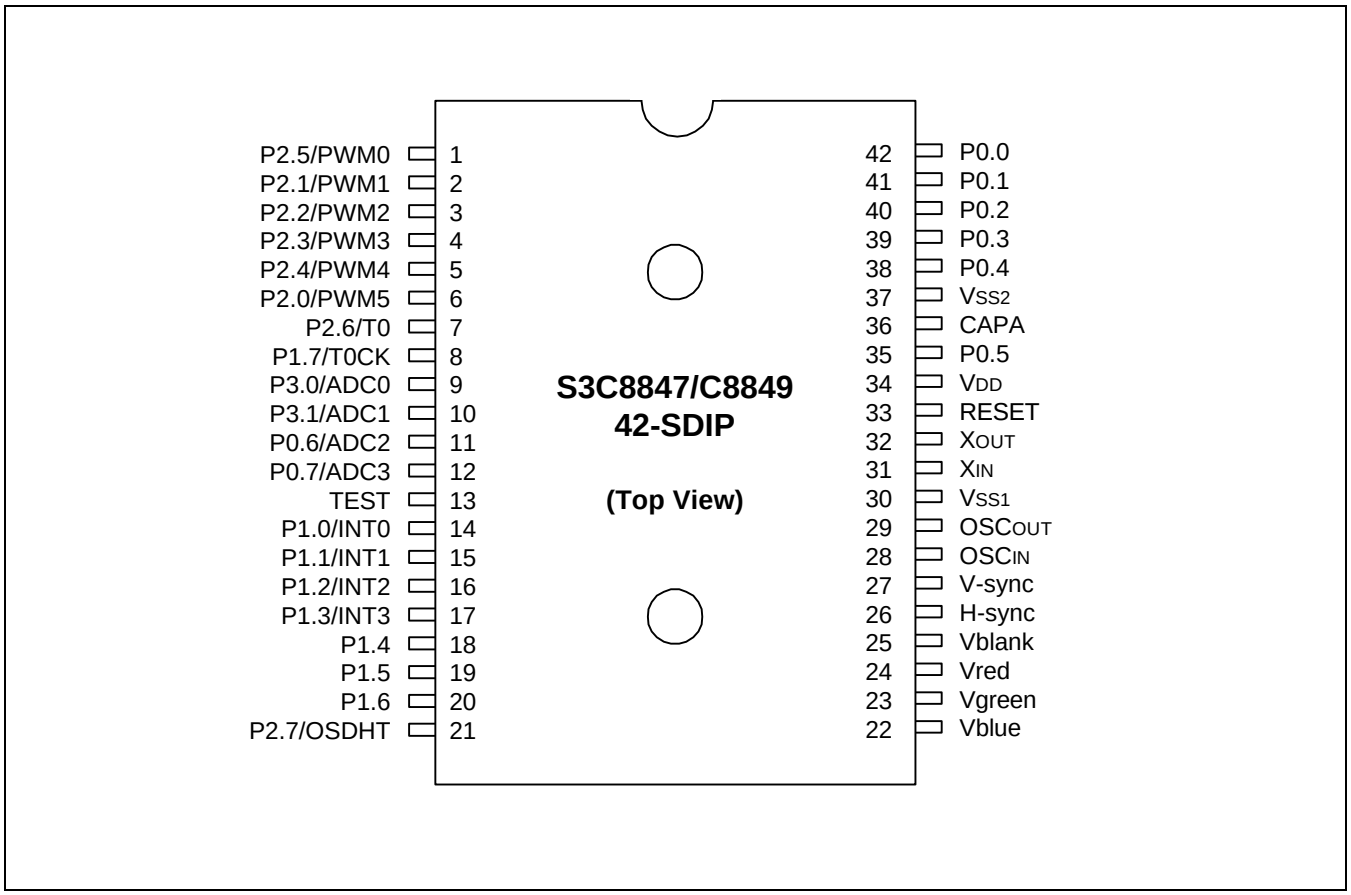


Figure 1-2. S3C8847/C8849/P8849 Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. S3C8847/C8849/P8849 Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Numbers	Share Pins
P0.0–P0.3	I/O	General I/O port (4-bit), configurable for digital input or n-channel open-drain, push-pull output. Pins can withstand up to 5 V loads.	2	39–42	(see pin description)
P0.4–P0.5		General I/O port (2-bit), configurable for digital input or push-pull output.	3	38, 35	
P0.6–P0.7		General I/O port (2-bit), configurable for digital input or n-channel open-drain output. P0.6–P0.7 can withstand up to 5 V loads. Multiplexed for alternative use as external inputs, ADC2–ADC3.	6	11–12	ADC2–ADC3
P1.0–P1.3	I/O	General I/O port (4-bit), configurable for digital input or n-channel open-drain output. P1.0–P1.3 can withstand up to 6 V loads. Multiplexed for alternative use as external interrupt inputs, INT0–INT3.	7	14–17	INT0–INT3
P1.4–P1.5		General I/O port (2-bit), configurable for digital input or n-channel open-drain output. P1.4–P1.5 can withstand up to 6 V loads. High current port(10mA)	5	18–19	
P1.6–P1.7		General I/O port (2-bit), configurable for digital input or push-pull output. Each pin has an alternative function. P1.7: T0CK (Timer 0 clock input)	3	20, 8	T0CK
P2.0–P2.7	I/O	General I/O port (8-bit). Input/output mode or n-channel open-drain, push-pull output mode are software configurable. Pins can withstand up to 5 V loads. Each pin has an alternative function. P2.0: PWM5 (8-bit PWM output) P2.1: PWM1 (14-bit PWM output) P2.2: PWM2 (8-bit PWM output) P2.3: PWM3 (8-bit PWM output) P2.4: PWM4 (8-bit PWM output) P2.5: PWM0 (14-bit PWM output) P2.6: T0 (Timer 0 PWM and interval output) P2.7: OSDHT (Halftone signal output)	2	1–7, 21	PWM0–PWM5 T0, OSDHT
P3.0–P3.1	I/O	General I/O port (2-bit), configurable for digital input or n-channel open-drain output. P3.0–P3.1 can withstand up to 5 V loads. Multiplexed for alternative use as external inputs ADC0–ADC1.	6	9–10	ADC0–ADC1

Table 1-1. S3C8847/C8849/P8849 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Numbers	Share Pins
PWM0–PWM1	O	Output pin for 14-bit PWM circuit	2	1, 2	P2.5, P2.1
PWM2–PWM5	O	Output pin for 8-bit PWM circuit	2	3–6	P2.2–P2.4, P2.0
ADC0–ADC3	I	Analog inputs for 4-bit A/D converter	6	9–12	P3.0–P3.1, P0.6–P0.7
INT0–INT3	I	External interrupt input pins	7	14–17	P1.0–P1.3
T0	O	Timer 0 output (interval, PWM)	2	7	P2.6
T0CK	I	Timer 0 clock input	3	8	P1.7
OSDHT	O	Halftone control signal output for OSD	2	21	P2.7
Vblue, Vgreen Vred, Vblank	O	Digital blue, green, red, and video blank signal outputs for OSD	4	22–25	–
H-sync, V-sync	I	H-sync, V-sync input for OSD	1	26, 27	–
OSC_{IN}, OSC_{OUT}	I, O	L-C oscillator pins for OSD clock frequency generation	–	28, 29	–
X_{IN}, X_{OUT}	I, O	System clock pins	–	31, 32	–
RESET	I	System reset input pin	8	33	–
TEST	–	Test Pin (must be connected to V_{SS}). Factory test mode is activated when 12V is applied.	–	13	–
V_{DD}, V_{SS1}, V_{SS2}	–	Power supply pins	–	34, 30, 37	–
CAPA	I	Input for capture A module	1	36	–

PIN CIRCUITS

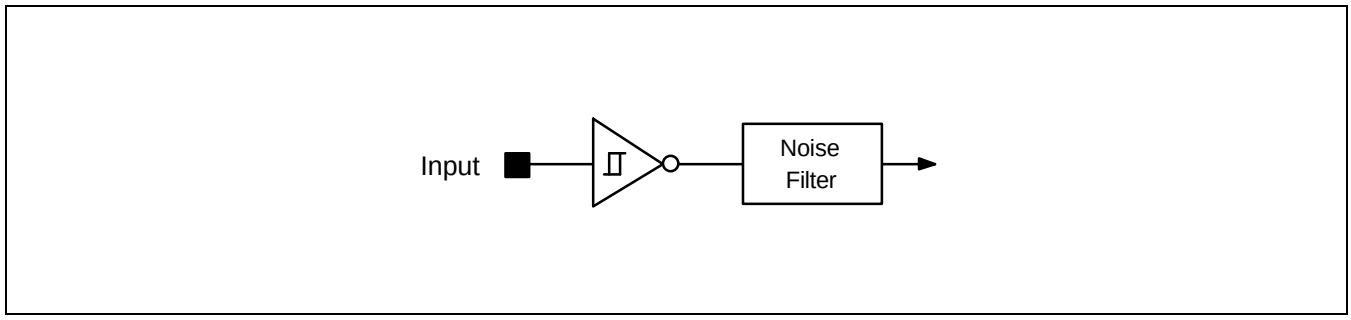


Figure 1-3. Pin Circuit Type 1 (V-Sync H-Sync, CAPA)

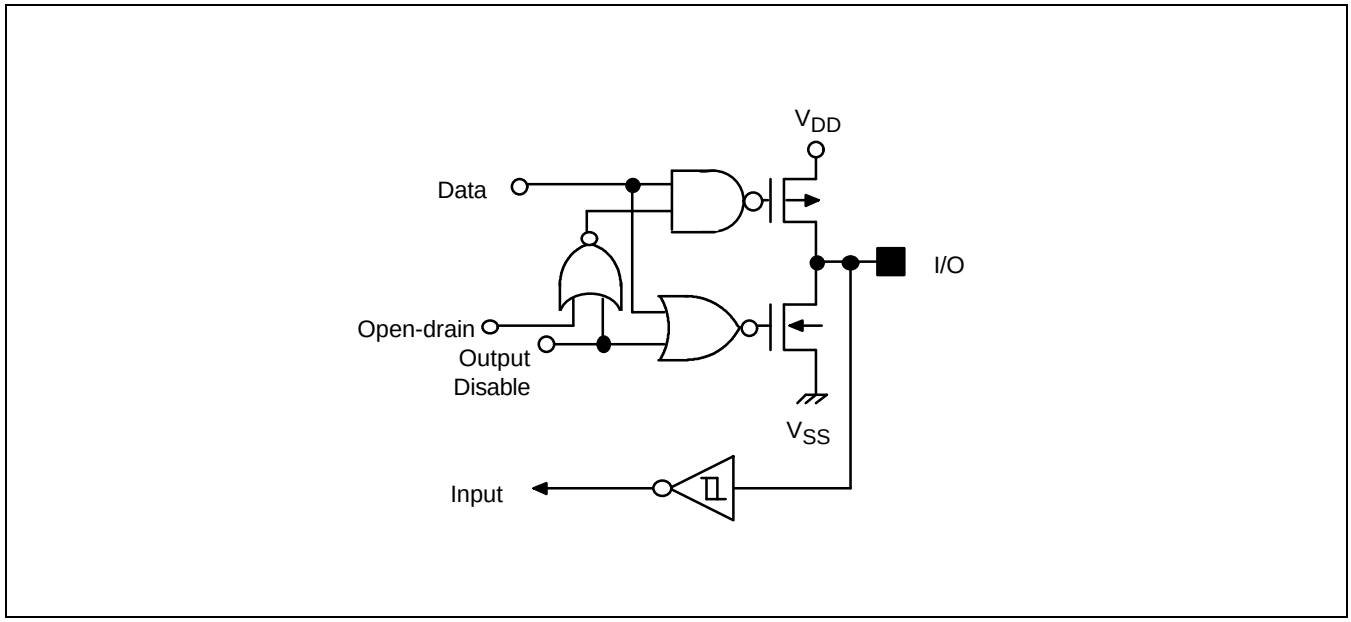


Figure 1-4. Pin Circuit Type 2 (P2.0–P2.7, P0.0–P0.3, PWM0–PWM5, T0, OSDHT)

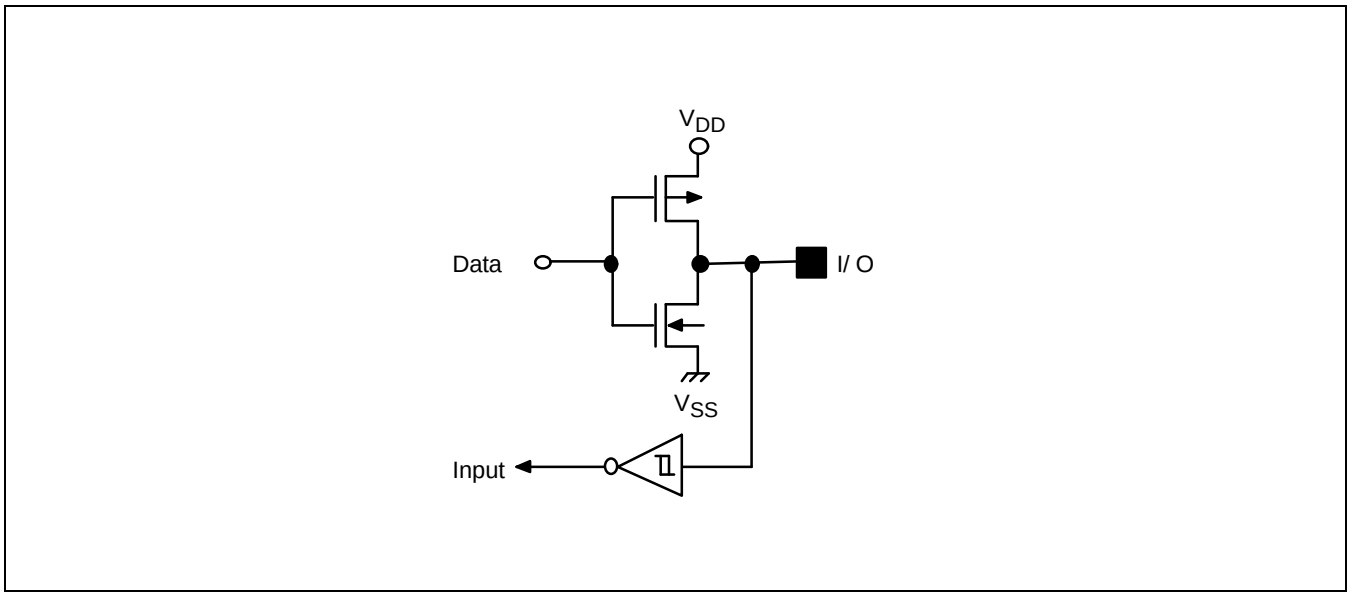


Figure 1-5. Pin Circuit Type 3 (P0.4–P0.5, P1.6–P1.7, T0CK)

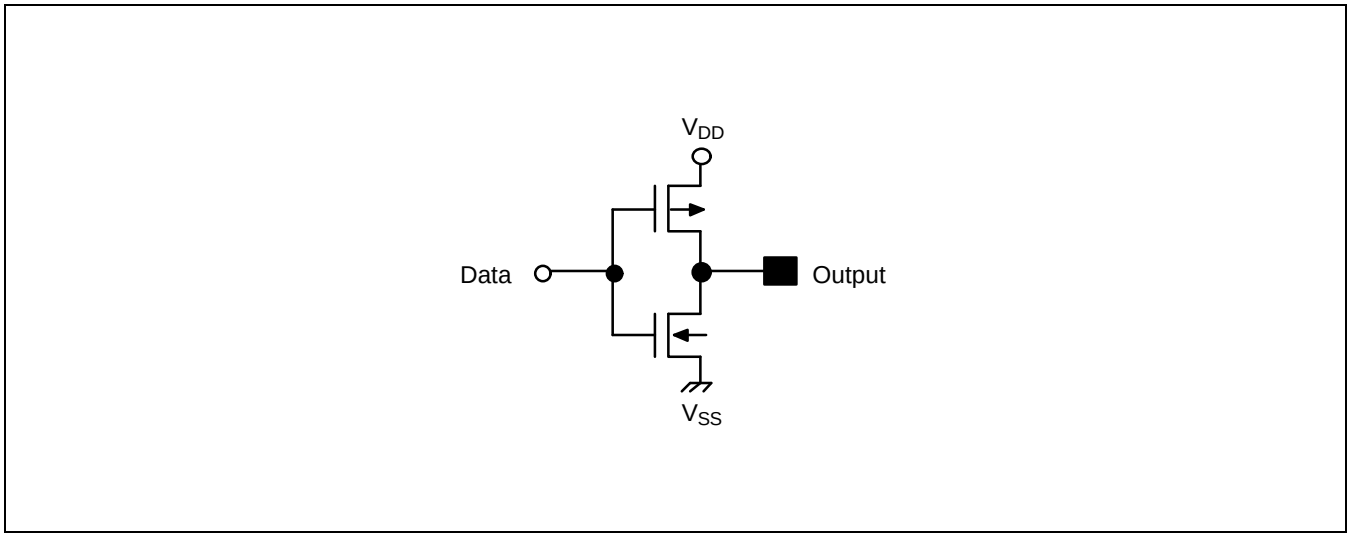
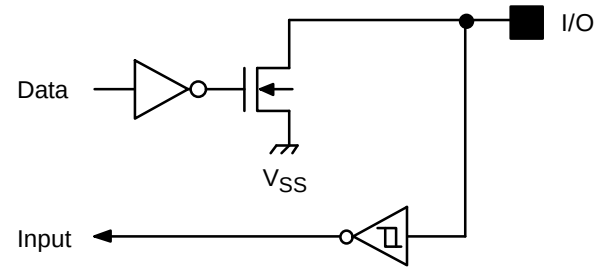
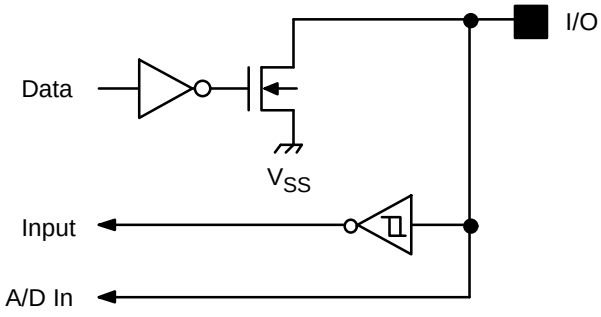


Figure 1-6. Pin Circuit Type 4 (Vblue, Vgreen, Vred, Vblank)



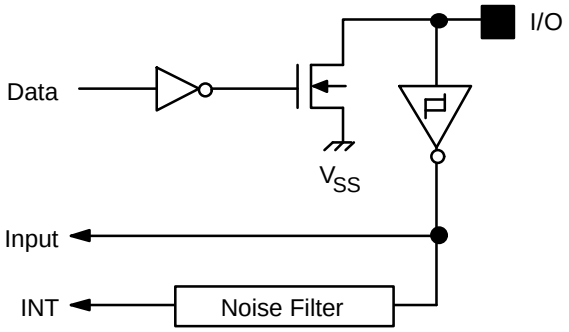
NOTE: Circuit type 5 can withstand up to 6 V loads.

Figure 1-7. Pin Circuit Type 5 (P1.4–P1.5)



NOTE: Circuit type 6 can withstand up to 5 V loads.

Figure 1-8. Pin Circuit Type 6 (P3.0–P3.1, P0.6–P0.7, ADC0–ADC3)



NOTE: Circuit type 7 can withstand up to 6 V loads.

Figure 1-9. Pin Circuit Type 7 (P1.0–P1.3, INT0–INT3)

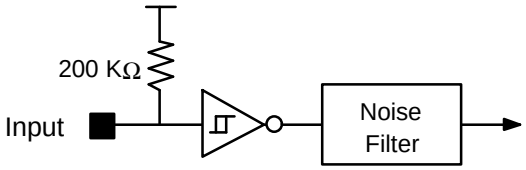


Figure 1-10. Pin Circuit Type 8 (RESET)

15 ELECTRICAL DATA

OVERVIEW

In this section, the S3C8847 and the S3C8849 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— D.C. electrical characteristics
— I/O capacitance
— A.C. electrical characteristics
— Input timing measurement points for t_{NF1} and t_{NF2}
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by RESET
— Main oscillator and L-C oscillator frequency
— Clock timing measurement points for X_{IN}
— Main oscillator clock stabilization time (t_{ST})
— A/D converter electrical characteristics
— Characteristic curves

Table 15-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	–	– 0.3 to + 6.0	V
Input Voltage	V_{I1}	P1.0–P1.5 (open-drain)	– 0.3 to + 7	V
	V_{I2}	All port pins except V_{I1}	– 0.3 to V_{DD} + 0.3	
Output Voltage	V_O	All output pins	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output Current Low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for port 1	+ 100	
		Total pin current for ports 0, 2, and 3	+ 100	
Operating Temperature	T_A	–	– 20 to + 85	°C
Storage Temperature	T_{STG}	–	– 65 to + 150	°C

Table 15-2. D.C. Electrical Characteristics

(T_A = – 20 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	All input pins except V_{IH2}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}, X_{OUT}	2.7 V			
Input Low Voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}, X_{OUT}			1.0 V	
Output High Voltage	V_{OH}	I_{OH} = – 500 µA P0.0–P0.5, P1.6–P1.7, P2 R, G, B, Vblank	V_{DD} – 0.8	–	–	V
Output Low Voltage	V_{OL1}	I_{OL} = 4 mA P0.0–P0.5, P1.6–P1.7	–	–	0.4	V
	V_{OL2}	I_{OL} = 10 mA P1.4–P1.5	–	–	0.8	
	V_{OL3}	I_{OL} = 2 mA P1.0–P1.3, P3.0–P3.1, P0.6–P0.7	–	–	0.4	
	V_{OL4}	I_{OL} = 1 mA R, G, B, Vblank, P2	–	–	0.4	V

Table 15-2. D.C. Electrical Characteristics (Continued)

(T_A = – 20 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Leakage Current	I_{LIH1}	$V_{IN} = V_{DD}$ All input pins except I_{LIH2} and I_{LIH3}	–	–	3	µA
	I_{LIH2}	$V_{IN} = V_{DD}$, OSC_{IN}, OSC_{OUT}			10	
	I_{LIH3}	$V_{IN} = V_{DD}$, X_{IN}, X_{OUT}	2.5	10	20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except I_{LIL2}, I_{LIL3}, and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V, OSC_{IN}, OSC_{OUT}			– 10	
	I_{LIL3}	V_{IN} = 0 V, X_{IN}, X_{OUT}	– 2.5	– 10	– 20	
Output High Leakage Current	I_{LOH1}	$V_{OUT} = V_{DD}$ All output pins except I_{LOH2}	–	–	3	µA
	I_{LOH2}	V_{OUT} = 6 V P1.0–P1.5			10	
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0 V All output pins	–	–	– 3	µA
Supply Current (note)	I_{DD1}	Normal mode; V_{DD} = 4.5 V to 5.5 V 8-MHz CPU clock	–	7	20	mA
	I_{DD2}	Idle mode; V_{DD} = 4.5 V to 5.5 V 8-MHz CPU clock		2	10	
	I_{DD3}	Stop mode; V_{DD} = 4.5 V to 5.5 V		1	10	µA

NOTE: Supply current does not include the current drawn through internal pull-up resistors or external output current loads.

Table 15-3. Input/output Capacitance

(T_A = – 20 °C to + 85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 15-4. A.C. Electrical Characteristics

(T_A = – 20 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V-sync Pulse Width	t_{VW}	–	4	–	–	µs
H-sync Pulse Width	t_{HW}	–	3	–	–	µs
Noise Filter	t_{NF1}	P1.0–P1.3	–	350	–	ns
	t_{NF2}	RESET, H-sync, V-sync	–	1000		
	t_{NF3}	Glitch filter (oscillator block)	–	25		
	t_{NF4}	CAPA	–	5	–	t_{CAPA}

NOTE: $f_{CAPA} = f_{OSC}/128$

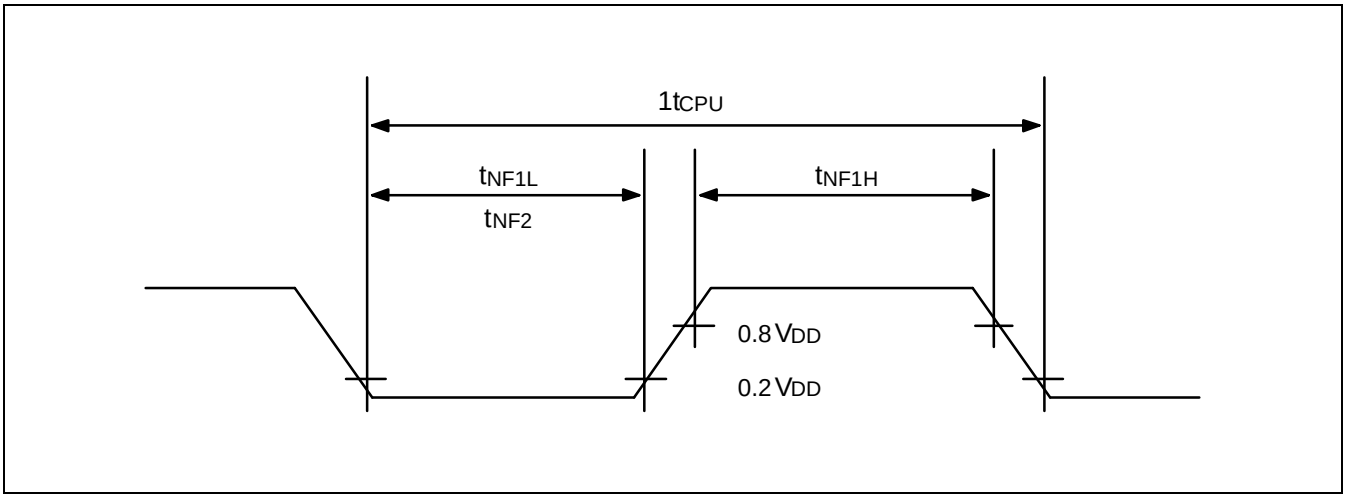


Figure 15-1. Input Timing Measurement Points for t_{NF1} and t_{NF2}

Table 15-5. Data Retention Supply Voltage in Stop Mode

(T_A = – 20 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}	Stop mode	2	–	6	V
Data Retention Supply Current	I_{DDDR}	Stop mode, V_{DDDR} = 2.0 V	–	–	5	µA

NOTES:
1. Supply current does not include the current drawn through internal pull-up resistors or external output current loads.
2. During the oscillator stabilization wait time (t_{WAIT}), all the CPU operations must be stopped.

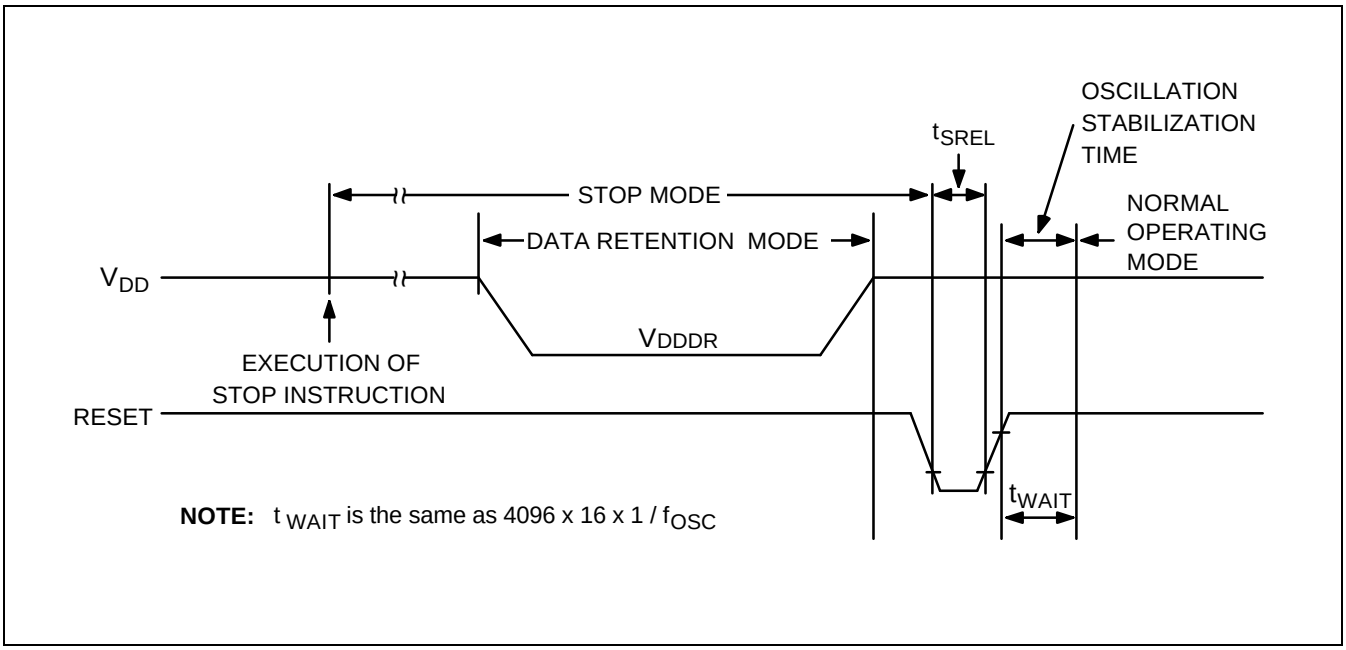
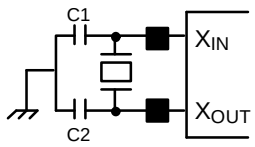
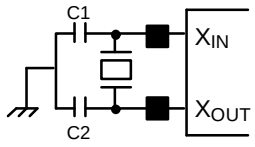
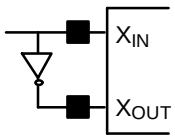
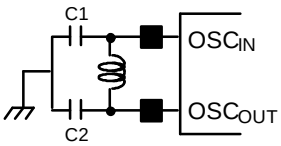


Figure 15-2. Stop Mode Release Timing When Initiated by a RESET

Table 15-6. Main Oscillator and L-C Oscillator Frequency

(T_A = – 20 °C + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		OSD block active	5	6	8	MHz
		OSD block inactive	0.5	6	8	
Ceramic		OSD block active	5	6	8	MHz
		OSD block inactive	0.5	6	8	
External Clock		OSD block active	5	6	8	MHz
		OSD block inactive	0.5	6	8	
L-C Oscillator		Recommend value; C1 = C2 = 20 pF	5	6.5	8	MHz
CPU Clock Frequency		–	0.032	6.0	8	MHz

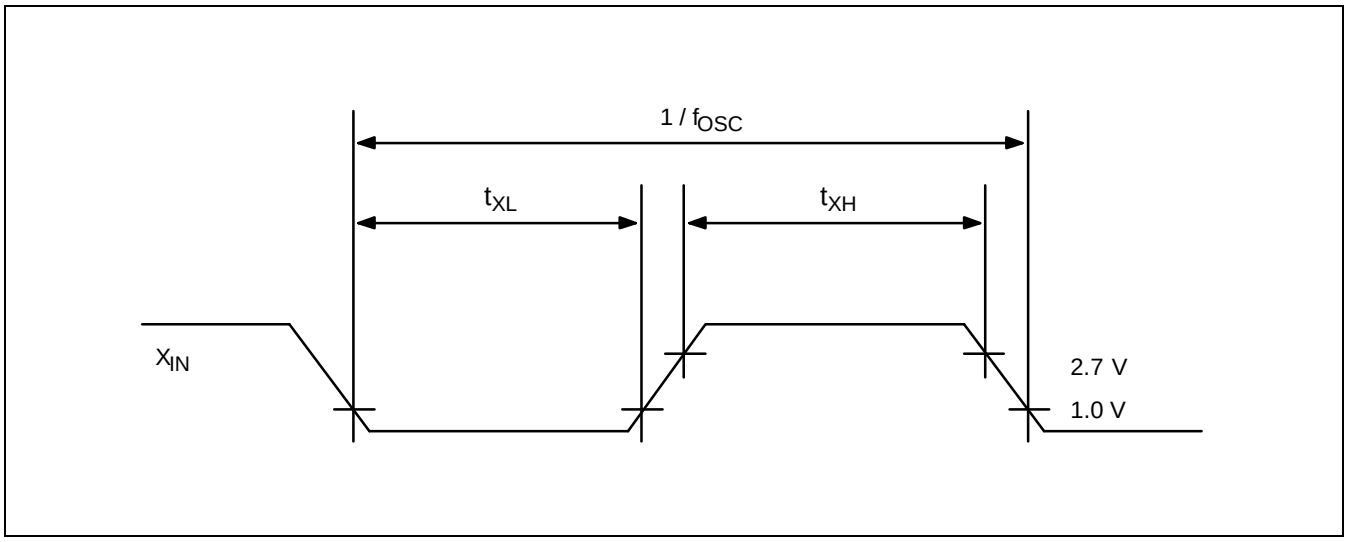


Figure 15-3. Clock Timing Measurement Points for X_{IN}

Table 15-7. Main Oscillator Clock Stabilization Time

(T_A = – 20 °C + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal	–	V_{DD} = 4.5 V to 6.0 V	–	–	20	ms
Ceramic		(Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.)			10	
External Clock		X_{IN} input High and Low level width (t_{XH}, t_{XL})	65	–	100	ns
Release Signal Setup Time	t_{SREL}	Normal operation	–	1000	–	ns
Oscillation Stabilization Wait Time (1)	t_{WAIT}	CPU clock = 8 MHz; Stop mode released by RESET	–	8.3	–	ms
		CPU clock = 8 MHz; Stop mode released by an interrupt		(2)		

NOTES:
1. Oscillation stabilization time is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is released.
2. The oscillation stabilization interval is determined by the basic timer (BT) input clock setting.

Table 15-8. A/D Converter Electrical Characteristics

(T_A = – 20 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V, V_{SS} = 0 V)

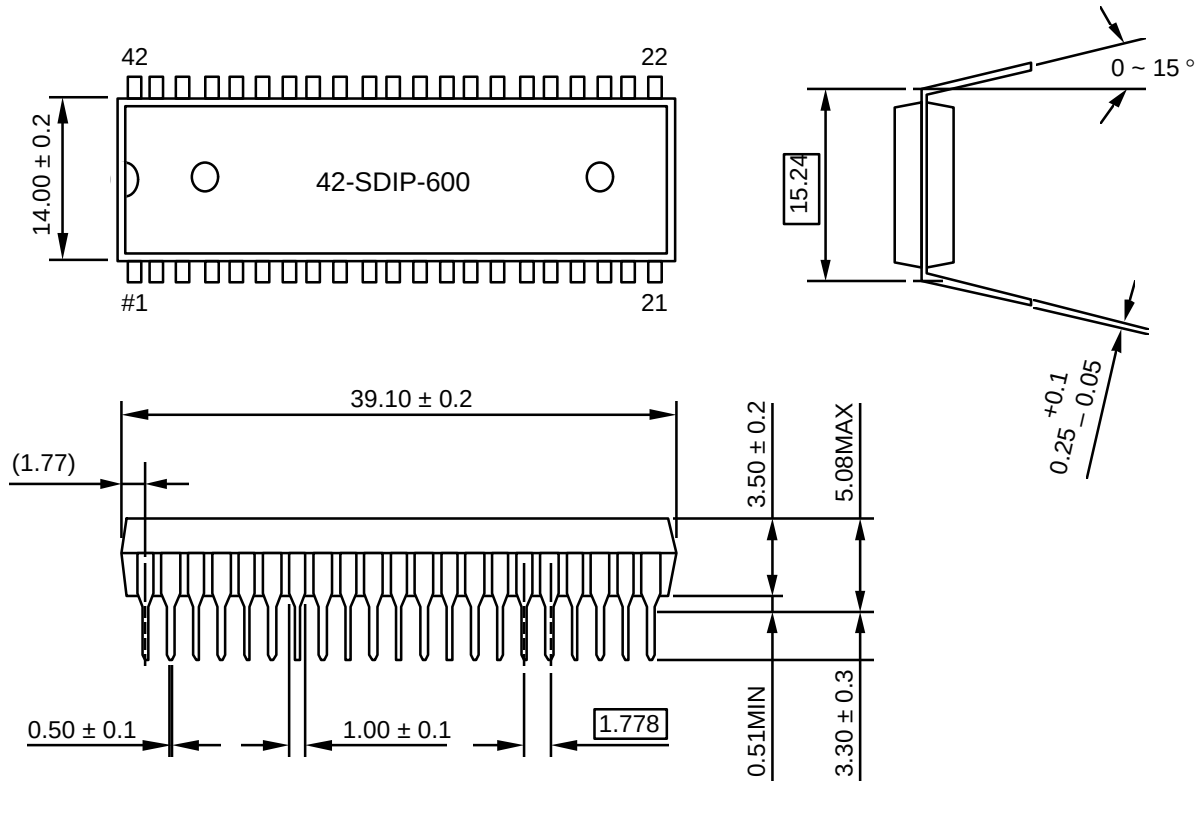
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Absolute Accuracy (1)	–	CPU clock = 8 MHz	–	–	± 0.5	LSB
Conversion Time (2)	t_{CON}		$t_{CPU} \times 25$ (3)	–		µs
Analog Input Voltage	V_{IAN}	–	V_{SS}	–	V_{DD}	V
Analog Input Impedance	R_{AN}	–	2		–	MΩ

NOTES:
1. Excluding quantization error, absolute accuracy values are within ± 1/2 LSB.
2. 'Conversion time' is the time required from the moment a conversion operation starts until it ends.
3. The unit t_{CPU} means one CPU clock period.

16 MECHANICAL DATA

OVERVIEW

The S3C8847 and the S3C8849 microcontrollers are available in 42-pin SIP package (42-SDIP-600).



NOTE: Package dimensions are in millimeters.

Figure 16-1. 42-Pin SDIP Package Mechanical Data (42-SDIP-600)

17 S3P8849 OTP

OVERVIEW

The S3P8849 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8847/C8849microcontroller. It has an on-chip OTP ROM instead of a masked ROM. The EPROM is accessed by serial data format.

The S3P8849 is fully compatible with the S3C8847/C8849, both in function and pin configuration. The simple programming requirements of the S3P8849 make the device ideal for use as an evaluation chip for the S3C8847/C8849.

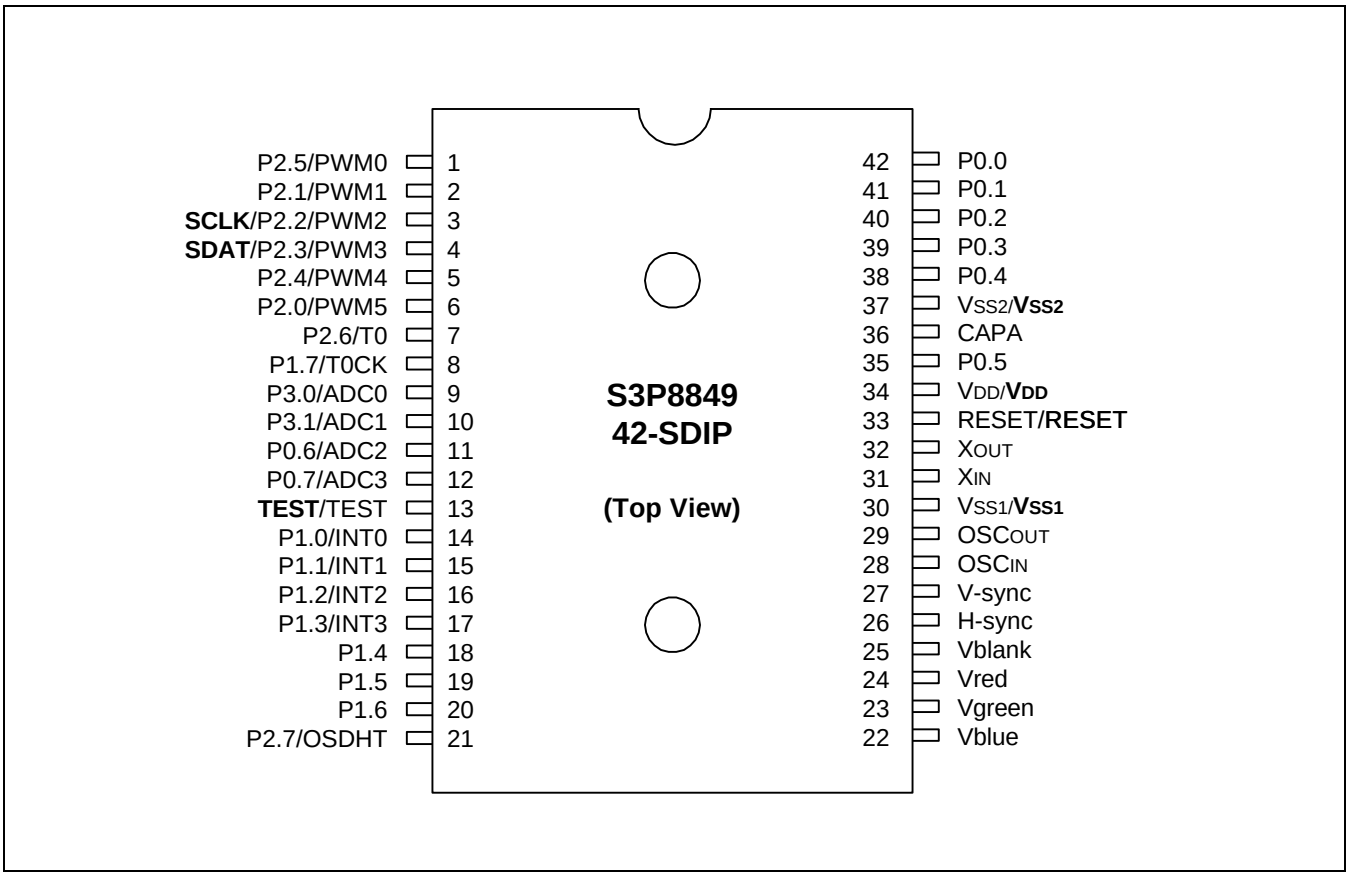


Figure 17-1. S3P8849 Pin Assignment (42-SDIP)

Table 17-1. Descriptions of Pins Used to Read/Write the EPROM (S3P8849)

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P2.3 (Pin 4)	SDAT	4	I/O	Serial data pin (output when reading, Input when writing) Input and push-pull output port can be assigned
P2.2 (Pin 3)	SCLK	3	I/O	Serial clock pin (Input only pin)
TEST	V_{PP} (TEST)	13	I	0 V: operating mode 5 V: test mode 12.5 V: OTP mode
RESET	RESET	33	I	5 V: operating mode, 0 V: OTP mode
V_{DD}/V_{SS}	V_{DD}/V_{SS}	34/30, 37	I	Logic power supply pin.

Table 17-2. Comparison of S3P8849 and S3C8847/C8849Features

Characteristic	S3P8849	S3C8847/C8849
Program Memory	32-K byte EPROM	24/32-K byte mask ROM
Operating Voltage (V_{DD})	4.5 V to 5.5 V	4.5 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, TEST V_{PP} = 12.5 V	–
Pin Configuration	42 SDIP	42 SDIP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the S3P8849, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 17-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/ MEM	ADDRESS (A15–A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.