Triple Analog Video Delay Line

The EL9115 is a triple analog delay line that allows skew compensation between any three signals. This part is perfect for compensating for the skew introduced by a typical CAT-5 cable with differing electrical lengths on each pair.

The EL9115 can be programmed in steps of 2ns up to 62ns total delay on each channel.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL9115IL	20-Pin QFN (5mm x 5mm)	-	MDP0046
EL9115IL-T7	20-Pin QFN (5mm x 5mm)	7”	MDP0046
EL9115IL-T13	20-Pin QFN (5mm x 5mm)	13”	MDP0046
EL9115ILZ (See Note)	20-Pin QFN (5mm x 5mm) (Pb-Free)	-	MDP0046
EL9115ILZ-T7 (See Note)	20-Pin QFN (5mm x 5mm) (Pb-Free)	7”	MDP0046
EL9115ILZ-T13 (See Note)	20-Pin QFN (5mm x 5mm) (Pb-Free)	13”	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

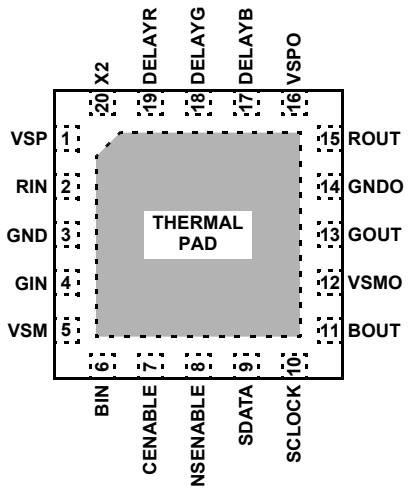
- 62ns total delay
- 2ns delay step increments
- Operates from ±5V supply
- Up to 122MHz bandwidth
- Low power consumption
- 20-pin QFN (5mm x 5mm) package
- Pb-Free plus anneal available (RoHS compliant)

Applications

- Skew control for RGB
- Analog beamforming

Pinout

EL9115
[20-PIN QFN (5MM X 5MM)]
TOP VIEW



EXPOSED DIEPLATE SHOULD BE CONNECTED TO -5V

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S+ to V_S-) 12V
Maximum Output Current. . . . . ±60mA
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+135°C
Ambient Operating Temperature . . . . . .-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_{SA}+ = V_A+ = +5V, V_{SA}- = V_A- = -5V, T_A = 25°C, exposed die plate = -5V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V+	Positive Supply Range		+4.5		+5.5	V
V-	Negative Supply Range		-4.5		-5.5	V
G_0	Gain Zero Delay	X2 = 5V, 150Ω load	1.81	1.89	2.04	
G_m	Gain Mid Delay		1.66	1.84	2.04	
G_f	Gain Full Delay		1.52	1.79	2.04	
DG_m0	Difference in Gain, 0 - Mid		-7.5	-2.5	2.5	%
DG_f0	Difference in Gain, 0 - Full		-13.5	-6.0	2.5	%
DG_fm	Difference in Gain, Mid - Full		-10.0	-2.6	4.0	%
V_{IN}	Input Voltage Range	Gain falls to 90% of nominal	-0.7		1.3	V
V_{OUT}	Output Voltage Range	X2 = +5V into 150Ω load	-5		1.6	V
I_B	Input Bias Current			1	5	µA
R_{IN}	Input Resistance			10		MΩ
V_{OS_0}	Output Offset 0 Delay	X2 = +5V, 75 + 75Ω load	-200	-150	60	mV
V_{OS_M}	Output Offset full Delay		-200	-140	60	mV
V_{OS_F}	Output Offset mid Delay		-200	-130	60	mV
Z_{OUT}	Output Impedance	Chip enable = +5V	4.5	4.8	5.1	Ω
		Chip enable = 0V		1		MΩ
+PSRR	Rejection of Positive Supply	X2 = +5V into 75 + 75Ω load		-38		dB
-PSRR	Rejection of Negative Supply	X2 = +5V into 75 + 75Ω load		-53		dB
I_{SP}	Supply Current (Note 1)	Chip enable = +5V current on V_{SP}	75	87	115	mA
I_{SM}	Supply Current (Note 1)	Chip enable = +5V current in V_{SM}	-10.5	-8.6	-7	mA
I_{SMO}	Supply Current (Note 1)	Chip enable = +5V current in V_{SMO}	-13	-11.6	-10	mA
I_{SPO}	Supply Current (Note 1)	Chip enable = +5V current in V_{SPO}	10	11.8	15.5	
ΔI_{SP}	Supply Current (Note 1)	Increase in I_{SP} per unit step in delay		0.9		mA
$I_{SP\ OFF}$	Supply Current (Note 1)	Chip enable = 0V current in V_{SP}		1.6		mA
I_{OUT}	Output Drive Current	10Ω load, 0.5V drive, X2 = 5V	30			mA
L_{HI}	Logic High	Switch high threshold		1.25	1.6	V
L_{LO}	Logic Low	Switch low threshold	0.8	1.15		V

NOTE:

1. All supply currents measured withe Delay R = 0ns, G = mid delay, B = full delay.

AC Electrical Specifications

$V_{SA}+ = V_A+ = +5V$, $V_{SA}- = V_A- = -5V$, $T_A = 25°C$, exposed die plate = -5V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
BW -3dB	3 dB Bandwidth	0ns Delay Time		122		MHz
BW 0.1dB	0.1dB Bandwidth	0ns Delay Time		60		MHz
SR	Slew Rate	0ns Delay Time		400		V/µs
$T_R - T_F$	Transient Response Time	20% - 80%, for all delays, 1V step		2.5		ns
V_{OVER}	Voltage Overshoot	for any delay, response to 1V step input		5	10	%
Glitch	Switching Glitch	Time for o/p to settle after last s_clock edge		100		ns
THD	Total Harmonic Distortion	$1V_{P-P}$ 10MHz sinewave, offset by +0.2V at mid delay setting		-50	-40	dB
X_T	Hostile Crosstalk	Stimulate G, measure R/B at 1MHz		-80		dB
V_N	Output Noise	Gain X2, measured at 75Ω load		2.5		mV rms
d_T	Delay Increment		1.75	2	2.25	ns
T_{MAX}	Maximum Delay		55	62	70	ns
D_{ELDT}	Delay Diff Between Channels			1.6		%
t_{PD}	Propagation Delay	Measured input to output	8.5	9.8	11	ns
T_{MAX}	Max s_clock Frequency	Maximum programming clock speed			10	MHz
T_en_ck	Minimum Separation Between Serial Enable and Clock .	Check enable low edge can occur after T_en_ck of previous (igored) clock and up to before T_en_ck of next (wanted) clock. Clock edges occurring within T_en_ck of the enable edge will have ncertain effect.		10		ns

Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VSP	+5V for delay circuitry and input amp
2	RIN	Red channel input, ref GND
3	GND	0V for delay circuitry supply
4	GIN	Green channel input, ref GND
5	VSM	-5V for input amp
6	BIN	Blue channel input, ref GND
7	CENABLE	Chip enable logical +5V enables chip
8	NSENABLE	$\overline{\text{ENABLE}}$ for serial input; enable on low
9	SDATA	Data into registers; logic threshold 1.2V
10	SCLOCK	Clock to enter data; logical; data written on negative edge
11	BOUT	Blue channel output, ref GND_O
12	VSMO	-5V for output buffers
13	GOUT	Green channel output, ref GND_O
14	GNDO	0V reference for input and output buffers
15	ROUT	Red channel output, ref GND_O
16	VSPO	+5V for output buffers
17	TESTB	Blue channel phase detector output
18	TESTG	Green channel phase detector output
19	TESTR	Red channel phase detector output
20	X2	Sets gain to 2X if input high; X1 otherwise
Thermal Pad		Must be connected to -5V

Typical Performance Curves

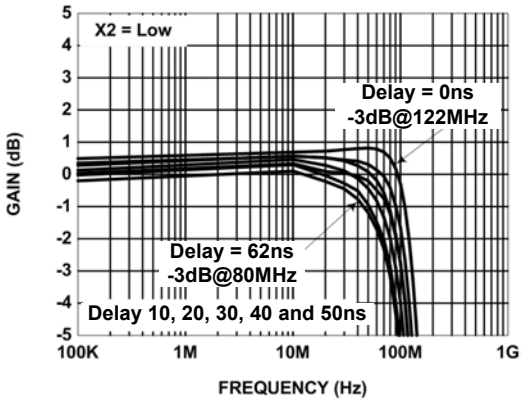


FIGURE 1. GAIN vs FREQUENCY

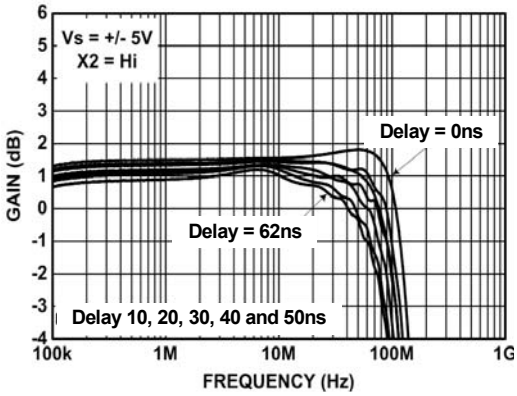


FIGURE 2. GAIN vs FREQUENCY

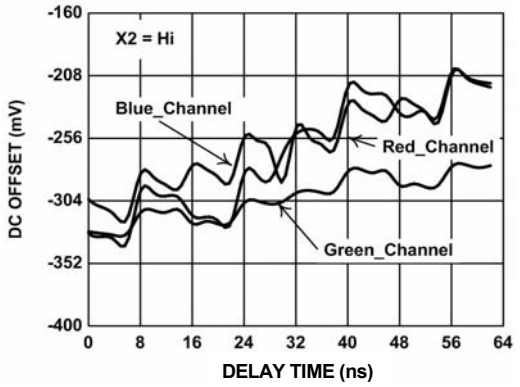


FIGURE 3. TYPICAL DC OFFSET vs DELAY TIME (X2 = Hi)

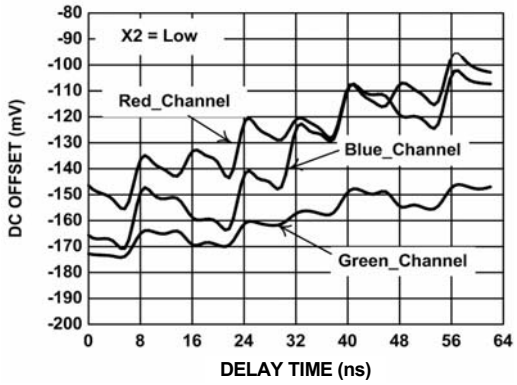


FIGURE 4. TYPICAL DC OFFSET vs DELAY TIME (X2 = Low)

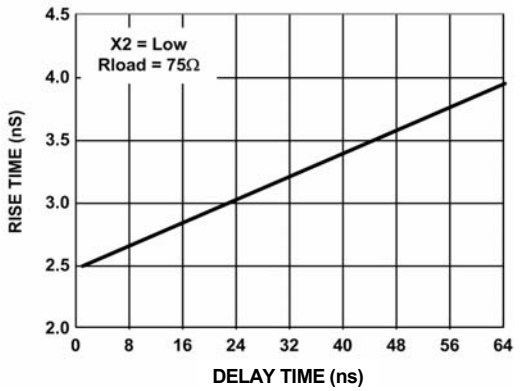


FIGURE 5. RISE TIME vs DELAY TIME

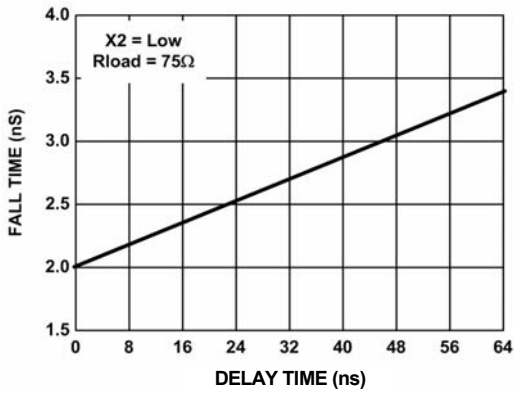


FIGURE 6. FALL TIME vs DELAY TIME

Typical Performance Curves

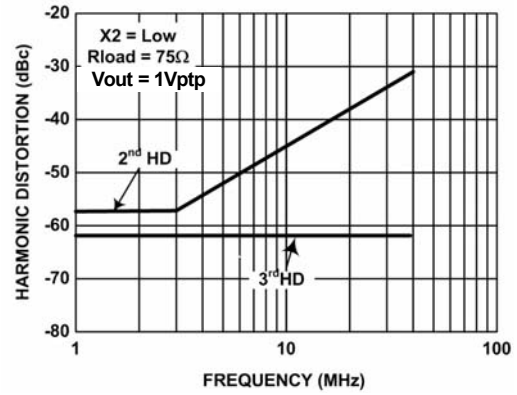


FIGURE 7. DISTORTION vs FREQUENCY

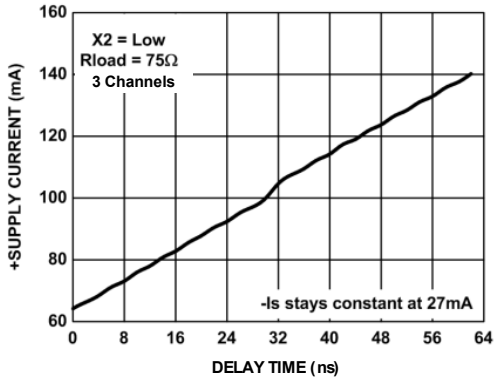


FIGURE 8. POSITVE SUPPLY CURRENT vs DELAY TIME

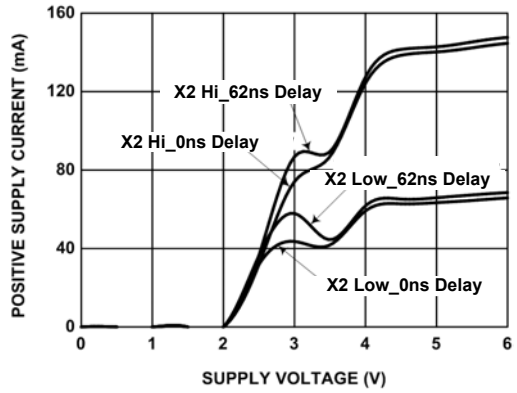


FIGURE 9. $I_{SUPPLY}+$ vs $V_{SUPPLY}+$

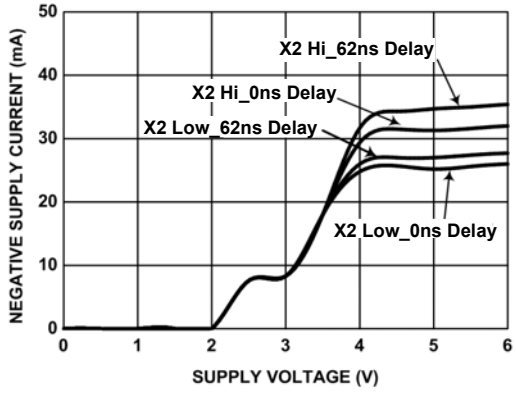


FIGURE 10. $I_{SUPPLY}-$ vs $V_{SUPPLY}-$

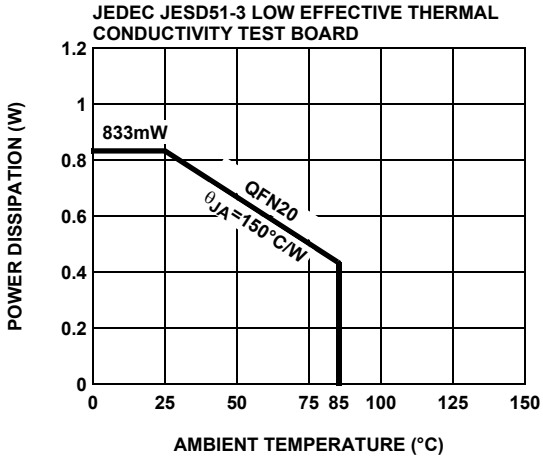


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

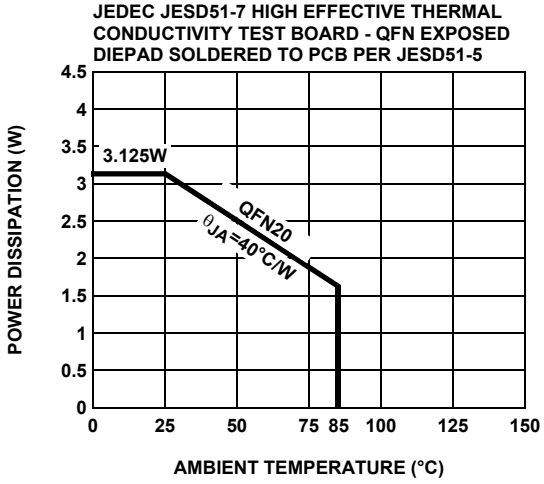


FIGURE 12. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

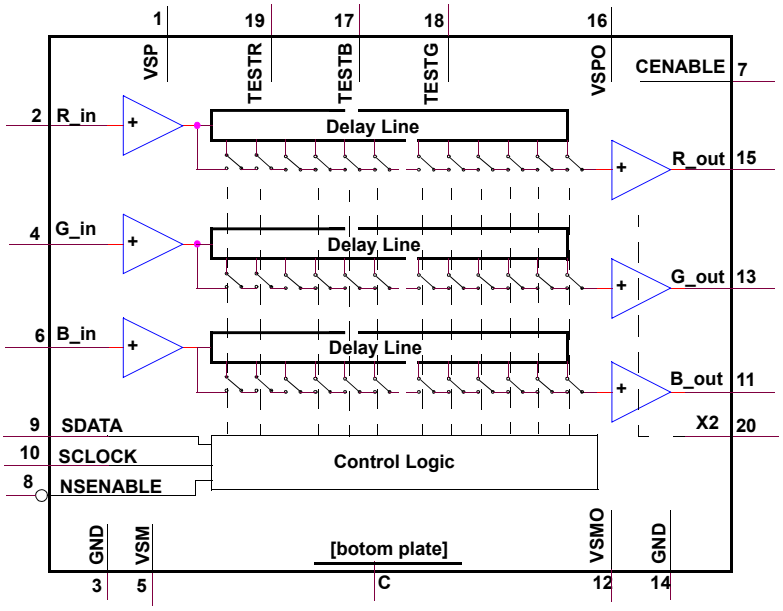


FIGURE 13. EL9115 BLOCK DIAGRAM

Applications Information:

EL9115 is a triple analog delay line receiver that allows skew compensation between any three high frequency signals. This part compensates for time skew introduced by a typical CAT-5 cable with differing electrical lengths on each pair. The EL9115 can be independently programmed via SPI interface in steps of 2ns up to 62ns total delay on each channel while achieving over 80MHz bandwidth.

Figure 13 shows the EL9115 block diagram. The 3 analog inputs are ground reference single ended signals. After the signal is received, the delay is introduced by switching filter blocks into the signal path. Each filter block is an all-pass filter introducing 2ns delay. In additional to time delay, each filter block also introduces some low pass filtering. As a result, the bandwidth of the signal path decrease from 120MHz at 0ns delay setting to 80MHz at the maximum delay setting as shown in the frequency response curve in the typical performance curves section.

In addition to delay, the extra amplifiers in the signal path also introduce offset voltage. The output offset voltage can shift by 100mV for X2 high setting and 50mV for X2 low.

In operation, it is best to allocate the most delayed signal 0ns delay then increase the delay on the other channels to bring them into line. This will result in the lowest power and distortion solution to balancing delays.

Power Dissipation

As the delay setting increases additional filter blocks turn on and insert into the signal path. For each 2ns of delay per channel Vsp current increases by 0.9mA while Vsm does not change significantly. Under the extreme settings, the positive supply current reaches 140mA and the negative supply current can be 35mA. Operating at +/-5V power supply, the total power dissipation is:

PD = 5*140mA + 5*35mA = 875mW

θ_{JA} required for long term reliable operation can be calculated. This is done using the equation:

θ_{JA} = (Tj - Ta)/PD = 57C/W

Where

Tj is the maximum junction temperature (135°C)

Ta is the maximum ambient temperature (85°C)

For a QFN 20 package in a properly layout PCB heatsinking copper area, 40C/W θ_{JA} thermal resistance can be achieved. To disperse the heat, the bottom heatspeader must be soldered to the PCB. Heat flows through the heatspeader to the circuit board copper then spreads and convects to air. Thus the PCB copper plane becomes the headsink (see TB389). This has proven to be a very effective technique. A separate application note details the 20 pin QFN PCB design considerations is available.

TABLE 1. SERIAL BUS DATA

vwxyz	DELAY
00000	0
00001	2
00010	4
00011	6
00100	8
00101	10
00110	12
00111	14
01000	16
01001	18
01010	20
01011	22
01100	24
01101	26
01110	28
01111	30
10000	32
10001	34
10010	36
10011	38
10100	40
10101	42
10110	44
10111	46
11000	48

TABLE 1. SERIAL BUS DATA (Continued)

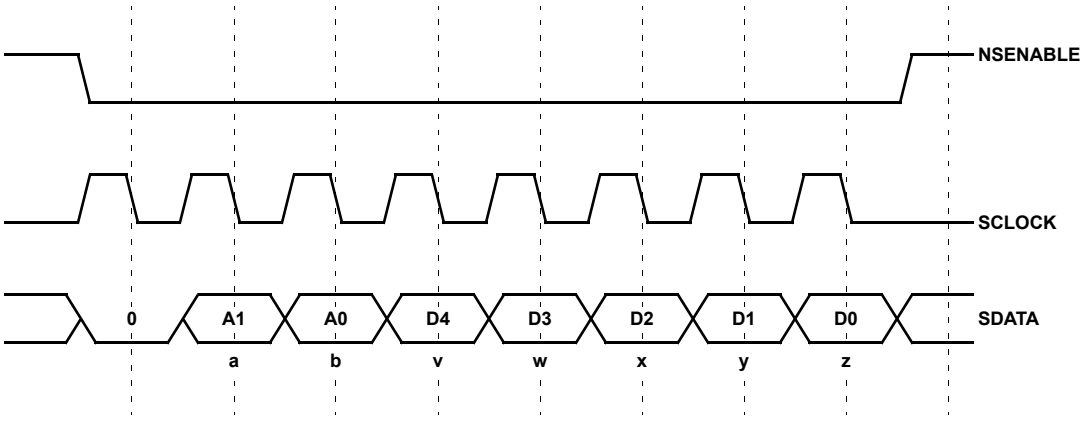
vwxyz	DELAY
11001	50
11010	52
11011	54
11100	56
11101	58
11110	60
11111	62

NOTES:

Delay register word = 0abvwxyz
Red register - ab = 01
Green register - ab = 10
Blue register - ab = 11
vwxyz selects delay

Serial Bus Operation

On the first negative clock edge after NSEnable goes low read input from DATA. This DATA level should be 0 (write into registers), READ is not supported. Read the next two data bits on subsequent negative edges and interpret them as the register to be filled. Reg 01 = R, 02 = G, 03 = B, 00 test use. Read the next five bits of data and send them to register. At the end of each block of 8 bits, any further data is treated as being a new word. Data entered is shifted directly to the final registers as it is clocked in. Initial value of all registers on power up is 0. It is the user's responsibility to send complete patterns of 8 clock cycles even if the first bit is set to 1. If less than 8 bits are sent, data will only be partially shifted through the registers. The pattern of 8 starts with NSEnable going low, so it is good practice to frame each word within an NS enable burst.



Test Pins

Three test pins are provided (Test R, Test G, Test B) during normal operation the test pins output pulses of current for a duration of the overlap between the inputs as shown in Figure 14:

Test_R pulse = Red out (A) wrt Green out (B)

Test_G pulse = Green out wrt Blue out

Test_B pulse = Blue out wrt Red out

Averaging the current gives a direct measure of the delay between the two edges. When A precedes B the current pulse is +50µA, and the output voltage goes up. When B precedes A the pulse is –50µA.

For the logic to work correctly A and B must have a period of overlap whilst they are high. I.e. a delay longer than the pulse width cannot be measured.

The signals A and B are derived from the video input by comparing the video signal with a slicing level which is set by an internal DAC. This enables the delay to be measured either from the rising edges of sync-like signals encoded on top of the video or from a dedicated set-up signal. The outputs can be used to set the correct delays for the signals received.

The DAC level is set through the serial input by bits 1-4 directed to the test register (00).

Test Mode

Bit zero of the test register is set to 0 for normal operation. If it is set to 1 then the device is in test mode. In Test Mode the DAC voltage is directed to the Green channel output whilst for the Red and Blue channels, the test outputs are now pulses of current which are generated by looking at the delay between the input and output of the channel. They thus enable the delay to be measured.

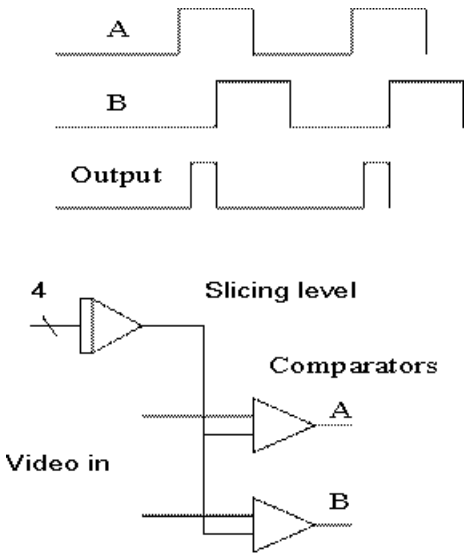


FIGURE 14. DELAY DETECTOR

TABLE 2.

wxyz	DAC/mV
1000	-400
1001	-350
1010	-300
1011	-250
1100	-200
1101	-150
1110	-100
1111	-50
0000	0
0001	50
0010	100
0011	150
0100	200
0101	250
0110	300
0111	350

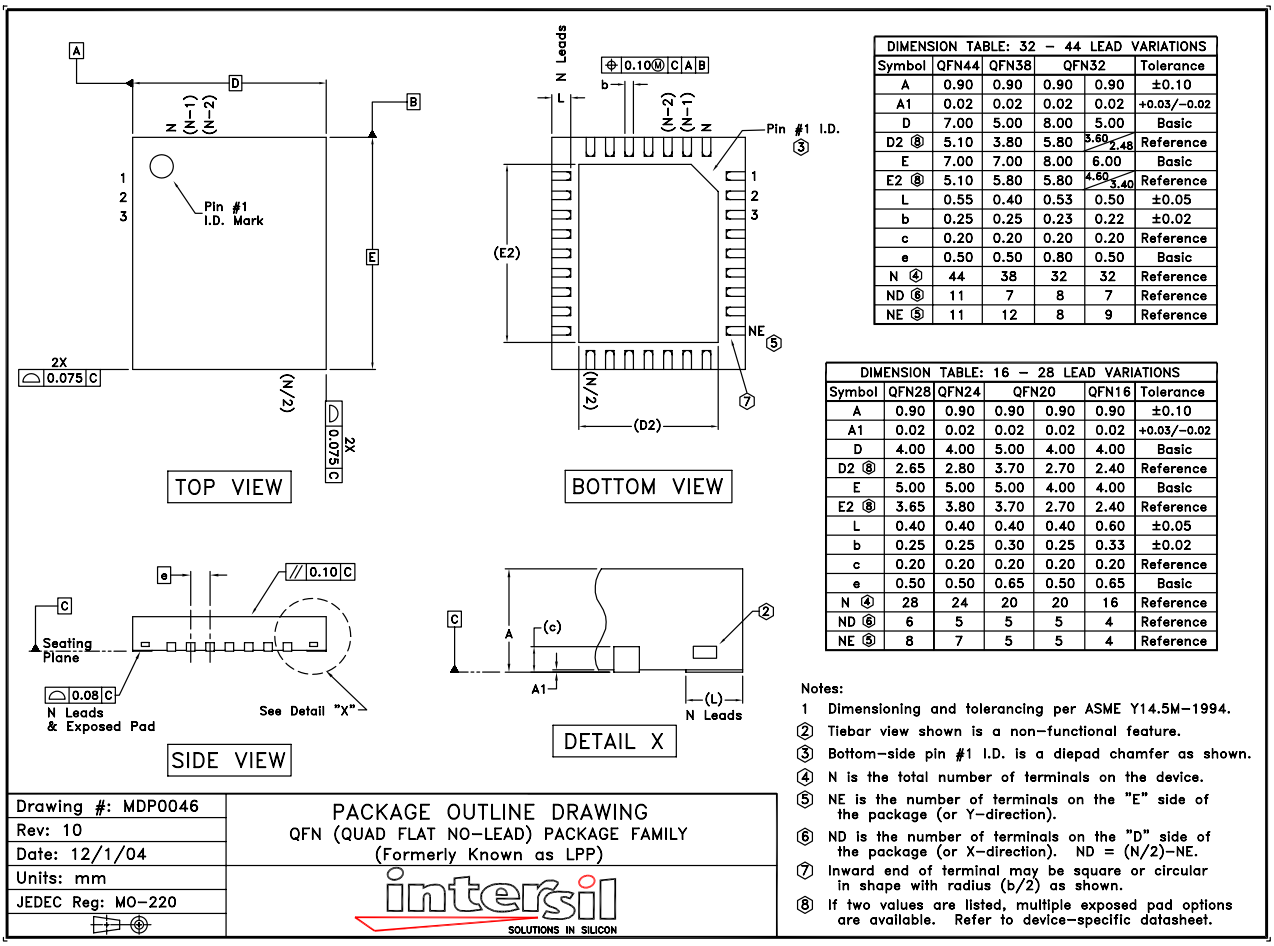
NOTES:

Test Register word = 000wxyzt

If t = 1 test mode else normal

wxyz fed to DAC. z is LSB

QFN Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	7.00	5.00	8.00	5.00	Basic
D2 ⑧	5.10	3.80	5.80	3.60 / 2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 ⑧	5.10	5.80	5.80	4.60 / 3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N ④	44	38	32	32	Reference
ND ⑥	11	7	8	7	Reference
NE ⑤	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS						
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/–0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 ⑧	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 ⑧	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N ④	28	24	20	20	16	Reference
ND ⑥	6	5	5	5	4	Reference
NE ⑤	8	7	5	5	4	Reference

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non–functional feature.
3. Bottom–side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y–direction).
6. ND is the number of terminals on the "D" side of the package (or X–direction). ND = (N/2)–NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device–specific datasheet.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

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