LD1072

16-CH LED DRIVER WITH DOT CORRECTION AND 12-BIT PWM CONTROL

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LDT Inc. does NOT assume any responsibility for use of circuits described.

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LD1072 Revision History

Version	Contents	Date
1.0	- First Release	2009.12.30

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DESCRIPTION

The LD1072 is a 16-channel, constant-current sink, LED driver. Each channel has a individually adjustable12- Bit PWM brightness control and a 64-step/256-step dot correction. The dot correction adjusts the brightness variations between LED channels and other LED Drivers. In 8-Bit Mode, LD1072 has 256-step Programmable Adjust Data Mode which controls 16 output current simultaneously. Both PWM control and dot correction are accessible via a serial interface. An external resistor sets the maximum current value of all 16 channels.

The LD1072 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an over temperature status.

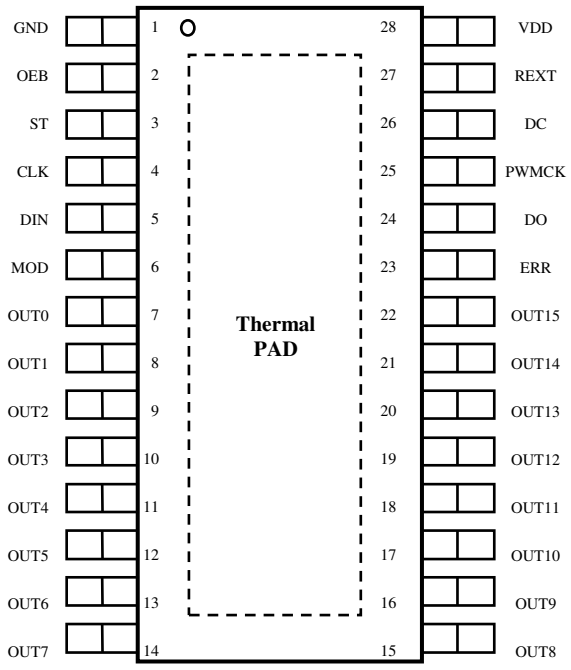
FEATURES

- 16 Channels
- 12-Bit (4096 Steps) Grayscale PWM Control
- Dot Correction
  - 6-Bit (64 Steps) / 8-Bit (256 Steps)(±33%)
- Programmable Adjust Output Current for 16Channel
  - 8-Bit (256 Steps)
- Drive Capability (Constant-Current Sink)
  - 0 mA to 80 mA (6-Bit)
  - 0 mA to 60 mA (8-Bit)
- LED Power Supply Voltage up to 17 V
- VDD = 3.0 V to 5.5 V
- Serial Data Interface
- Controlled In-Rush Current
- 30-MHz Data Transfer Rate
- CMOS Level I/O
- Error Information
  - LOD : LED Open Detection
  - TEF : Thermal Error Flag

Package : 28 Pin TSSOP

PIN CONFIGURATION

Thermal Exposed PACKAGE
(TOP VIEW)



ORDERING INFORMATION

PART NUMBER	PACKAGE	TA
LD1072-SS	28 TSSOP	-40℃ to 85 ℃

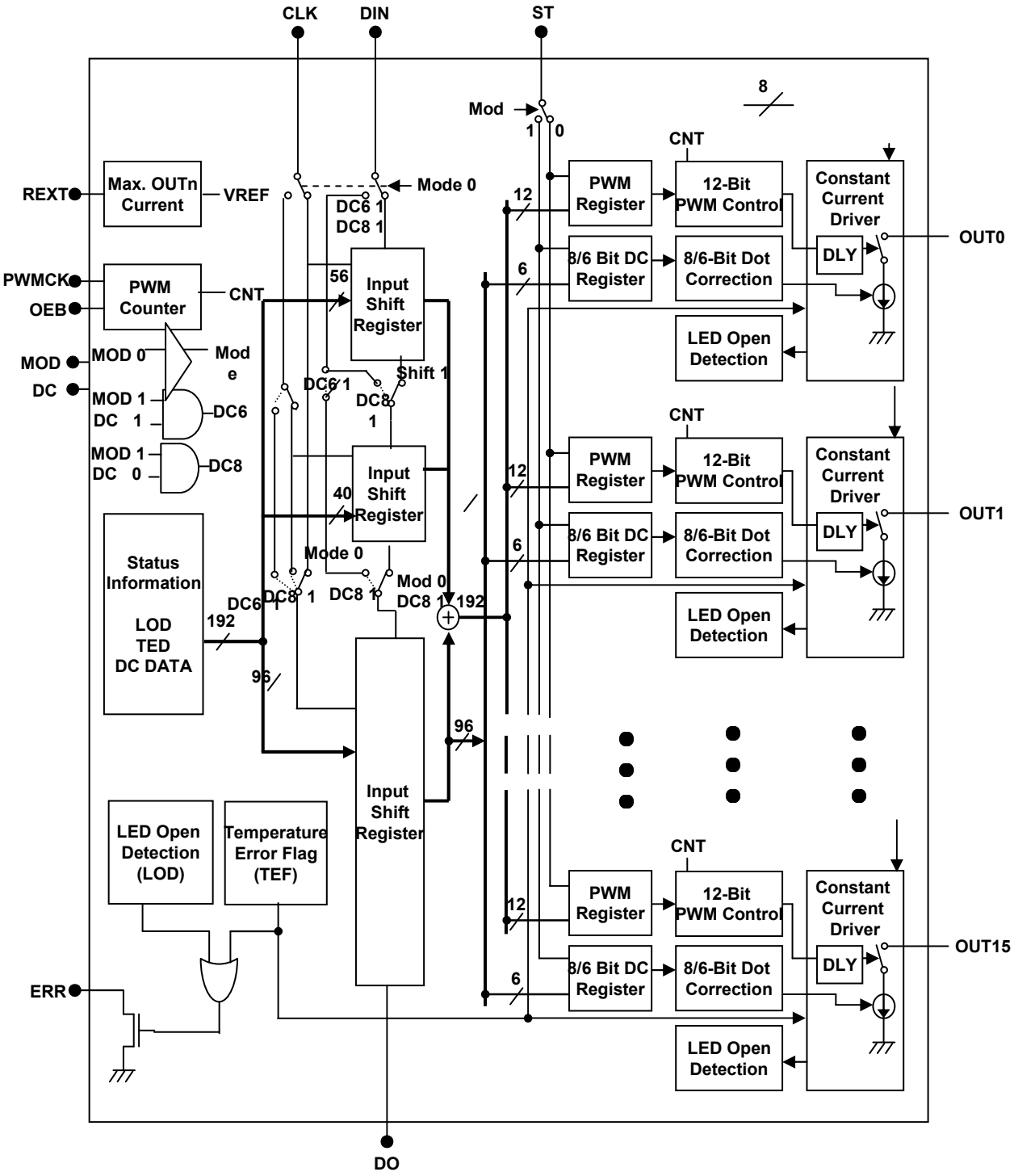
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PIN DESCRIPTION

TERMINAL		DESCRIPTION
NAME	NO.	
GND	1	Ground
OEB	2	Blank all outputs. When OEB = H, all OUTn outputs are forced OFF. PWM counter is also reset. When OEB = L, OUTn are controlled by grayscale PWM control.
ST	3	Level triggered latch signal. When ST = high, the LD1072 writes data from the input shift register to either PWM register (MOD = low) or DC register (MOD = high). When ST=low, the data in the PWM or DC registers is held constant and does not change.
CLK	4	Serial data shift clock
DIN	5	Serial data input
MOD	6	Input mode-change pin. When MOD = GND, the device is in PWM mode. When MOD = VDD, the device is in DC mode.
OUT <0 :15>	7-22	Constant-current output
ERR	23	Error output. ERR is an open-drain terminal. ERR goes L when LOD or TEF is detected.
DO	24	Serial data output.
PWMCK	25	Reference clock for grayscale PWM control
DC	26	When DC = VDD, the device is in 6-Bit Mode. when DC = GND, the device is in 8-Bit Mode and Programmable Adjust Mode.
REXT	27	Reference current terminal
VDD	28	Power supply voltage.

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0 ~ 7	V
Output Voltage	Vo	-0.5 ~ 18	V
Output current (dc)	I_O	90	mA
Input voltage range	V_I	-0.3 ~ V_{DD}+0.4	V
GND Terminal Current	I_{GND}	1440	mA
Power dissipation	TSSOP	1.4	W
Operating junction temperature	T_J(max)	150	℃
Storage temperature range	T_{STG}	-55 ~ 150	℃
Operating ambient temperature range	T_A	-40 ~ 85	℃

DC CHARACTERISTICS

CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}	3		5.5	V
Voltage applied to output (OUT0 - OUT15)		V_O			17	V
High-level input voltage		V_{IH}	0.8 VDD		VDD	V
Low-level input voltage		V_{IL}	GND		0.2 VDD	V
High-level output current	V_{DD} = 5 V at DO	I_{OH}			-1	mA
Low-level output current	V_{DD} = 5 V at DO, ERR	I_{OL}			1	mA
Constant output current	OUT0 to OUT15	I_{OLC}			80	mA
Operating junction temperature		T_J	-40		125	℃
Operating free-air temperature range		T_A	-40		85	℃

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AC CHRACTERISTICS

(V_{DD}=3V to 5.5V, T_A = -40℃ to 85℃) (unless otherwise noted)

CHARACTERISTICS	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data shift clock frequency	CLK	$f_{(CLK)}$			30	MHz
Grayscale clock frequency	PWMCK	$f_{(PWMCK)}$			33	MHz
CLK pulse duration	CLK = H/L (See Figure 14)	t_{wh0} / $_{wl0}$	10			ns
PWMCK pulse duration	PWMCK = H/L (See Figure 14)	t_{wh1} / $_{wl1}$	10			ns
ST pulse duration	ST = H (See Figure 14)	t_{wh2}	15			ns
OEB pulse duration	OEB = H (See Figure 14)	t_{wh3}	15			ns
Setup time	DIN - CLK↑ (See Figure 14)	t_{su0}	5			ns
	CLK↓ - ST↑ (See Figure 14)	t_{su1}	10			
	MOD↑↓ - ST↑ (See Figure 14)	t_{su2}	10			
	OEB↓ - PWMCK↑ (See Figure 14)`	t_{su3}	10			
	ST↑ - PWMCK↑ (See Figure 14)	t_{su4}	10			
Hold time	CLK↑ - DIN (See Figure 14)	t_{h0}	10			ns
	ST↓ - CLK↑ (See Figure 14)	t_{h1}	10			
	CLK↑ - MOD↑↓ (See Figure 14)	t_{h2}	10			
	ST↓ - MOD↑↓ (See Figure 14)	t_{h3}	10			
	PWMCK↑ - OEB↑ (See Figure 14)	t_{h4}	10			

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ELECTRICAL CHARACTERISTICS

(V_{DD}=3V to 5.5V, T_A = -40°C to 85°C) (unless otherwise noted)

PARAMETER	SYM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High-level Output Voltage	V_{OH}	I_{OH} = -1 mA, DO	V_{DD}* 0.8		V_{DD}	V
Low-level Output Voltage	V_{OL}	I_{OL} = 1 mA, DO	0		V_{DD}* 0.2	V
Input Current	I_I	V_I = V_{DD} or GND; OEB, DC, PWMCK, CLK, DIN, ST pin	-0.5		0.5	uA
		V_I = GND; MOD pin	-0.5		0.5	
		V_I = VDD; MOD pin	15		30	
Supply Current	I_{DD}	No data transfer, all output OFF, V_O = 1 V, $R_{(REXT)}$ = 10 kΩ	3		11	mA
		No data transfer, all output OFF, V_O = 1 V, $R_{(REXT)}$ = 1.3 kΩ	3		11	
		Data transfer 30 MHz,, all output ON, V_O = 1 V, $R_{(REXT)}$ = 1.3 kΩ	3		11	
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(REXT)}$ = 640Ω	5		11	
Constant Output Current	$I_{O(LC)}$	All output ON,V_O = 1 V, $R_{(REXT)}$ = 640Ω	10.0	10.4	10.7	
Leakage Output Current	I_{lkg}	All output OFF, V_O = 15 V, $R_{(REXT)}$ = 640Ω, OUT0 to OUT15	-0.1		0.1	uA
Constant Sink Current Error	$\Delta I_{O(LC0)}$	All output ON, V_O = 1 V, IOUT = 10mA, OUT0 to OUT15, –20℃ to 85℃ *(1)		± 1	± 4	%
		All output ON, V_O = 1 V, IOUT = 10mA, OUT0 to OUT15		± 1	± 8	
		All output ON, V_O = 1 V, IOUT=40mA, OUT0 to OUT15, –20℃ to 85℃		± 1	± 6	
		All output ON, V_O = 1 V, IOUT=40mA, OUT0 to OUT15		± 1	± 8	
Constant Sink Current Error	$\Delta I_{O(LC1)}$	Device to device, averaged current from OUT0 to OUT15, IOUT = 10mA *(2)		± 3	± 6	%
Constant Sink Current Error	$\Delta I_{O(LC2)}$	Device to device, averaged current from OUT0 to OUT15, IOUT=40mA *(2)		± 4	± 6	%
Line Regulation	$\Delta I_{O(LC3)}$	All output ON, V_O = 1 V, IOUT = 10mA OUT0 to OUT15, VDD = 3 V to 5.5 V *(3)		± 1	± 4	%/V
		All output ON, V_O = 1 V, IOUT = 40mA OUT0 to OUT15, VDD = 3 V to 5.5 V (3)				
Load Regulation	$\Delta_{IO(LC40)}$	All output ON, V_O = 1 V to 3 V, IOUT = 10mA, OUT0 to OUT15 (4)		± 2	± 6	%/V
		All output ON, V_O = 1 V to 3 V, IOUT = 40mA, OUT0 to OUT15 (4)		± 2	± 8	

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ELECTRICAL CHARACTERISTICS

(VDD=3V to 5.5V, TA = -40oC to 85) (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Thermal error flag threshold	$T_{(TEF)}$	Junction temperature *(5)	150		170	℃
LED open detection threshold	$V_{(LED)}$		-	0.3	0.4	V

(1) The deviation of each output from the average of OUT0-15 constant current. It is calculated by Equation 1 in Table 1.

(2) The deviation of average of OUT1-15 constant current from the ideal constant-current value.

It is calculated by Equation 2 in Table 1. The ideal current is calculated by Equation 3 in Table 1.

(3) The line regulation is calculated by Equation 4 in Table 1.

(4) The load regulation is calculated by Equation 5 in Table 1.

(5) Not tested. Specified by design.

Table 1. Test Parameter Equations

$\triangle(\%) = \frac{I_{OUTn} - I_{OUTavg_0\text{-}15}}{I_{OUTavg_0\text{-}15}} \times 100$	(1)
$\triangle(\%) = \frac{I_{OUTavgn} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \times 100$	(2)
$I_{OUT(IDEAL)} = 35 \times \frac{1.18V}{(40+R_{REXT})}$	(3)
$\triangle(\%/V) = \frac{(I_{OUTn} \text{ at } V_{DD} = 5.5V) - (I_{OUTn} \text{ at } V_{DD} = 3.0V)}{(I_{OUTn} \text{ at } V_{DD} = 3.0V)} \times \frac{100}{2.5}$	(4)
$\triangle(\%/V) = \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0V) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1.0V)} \times \frac{100}{2.0}$	(5)

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SWITCHING CHARACTERISTICS

(V_{DD} = 3V to 5.5V, C_L = 15pF,T_A = -40 ℃to 85℃ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Rise time	t_{r0}	DO			16	ns
	t_{r1}	OUTn, V_{DD} = 5 V, T_A = 60℃, DCn = 3Fh		10	30	
Fall time	T_{f0}	DO			16	ns
	t_{f1}	OUTn, V_{DD} = 5 V, T_A = 60 ℃, DCn = 3Fh		10	30	
Propagation delay time	t_{pd0}	CLK - DO (see Figure 12)			30	ns
	t_{pd1}	OEB - OUT0 (see Figure 12)			60	
	t_{pd2}	OUTn - ERR (see Figure 12)			1000	ns
	t_{pd3}	PWMCK - OUT0 (see Figure 12)			60	ns
	t_{pd4}	ST - IOUT (dot correction) (see Figure 12)			1000	ns
Output delay time	t_d	OUTn - OUT(n+1) (see Figure 12)		2	4	ns
Output on-time error	t_{on_err}	t_{outon} - T_{pwmck} (see Figure 12), PWMn = 01h, PWMCK = 11MHz	10	-20	-50	ns

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EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

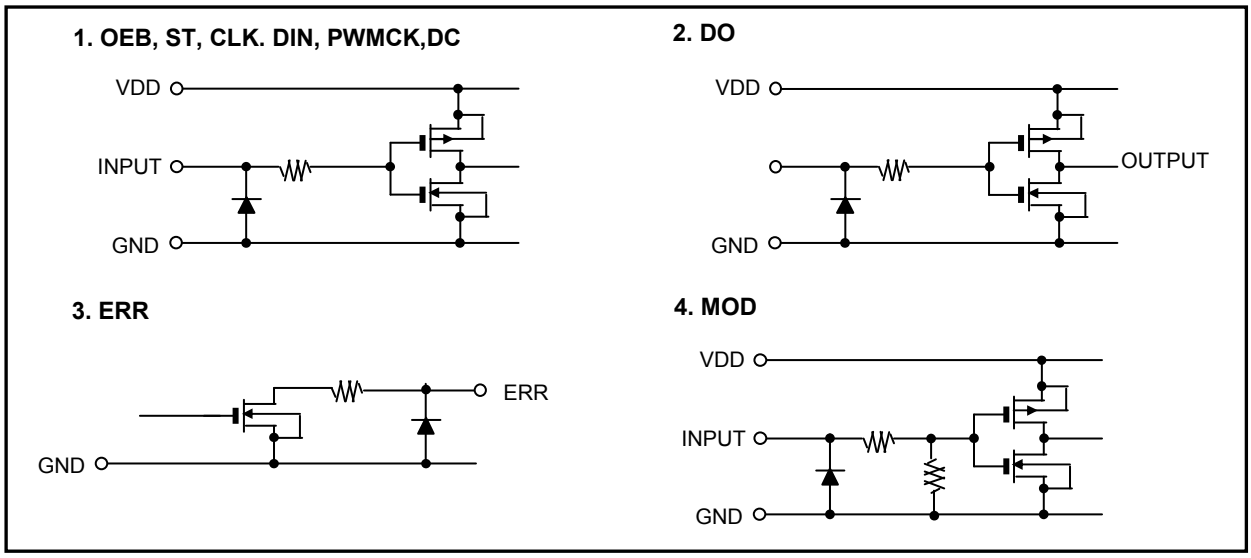


Figure 1. Input Output Equivalent Circuits

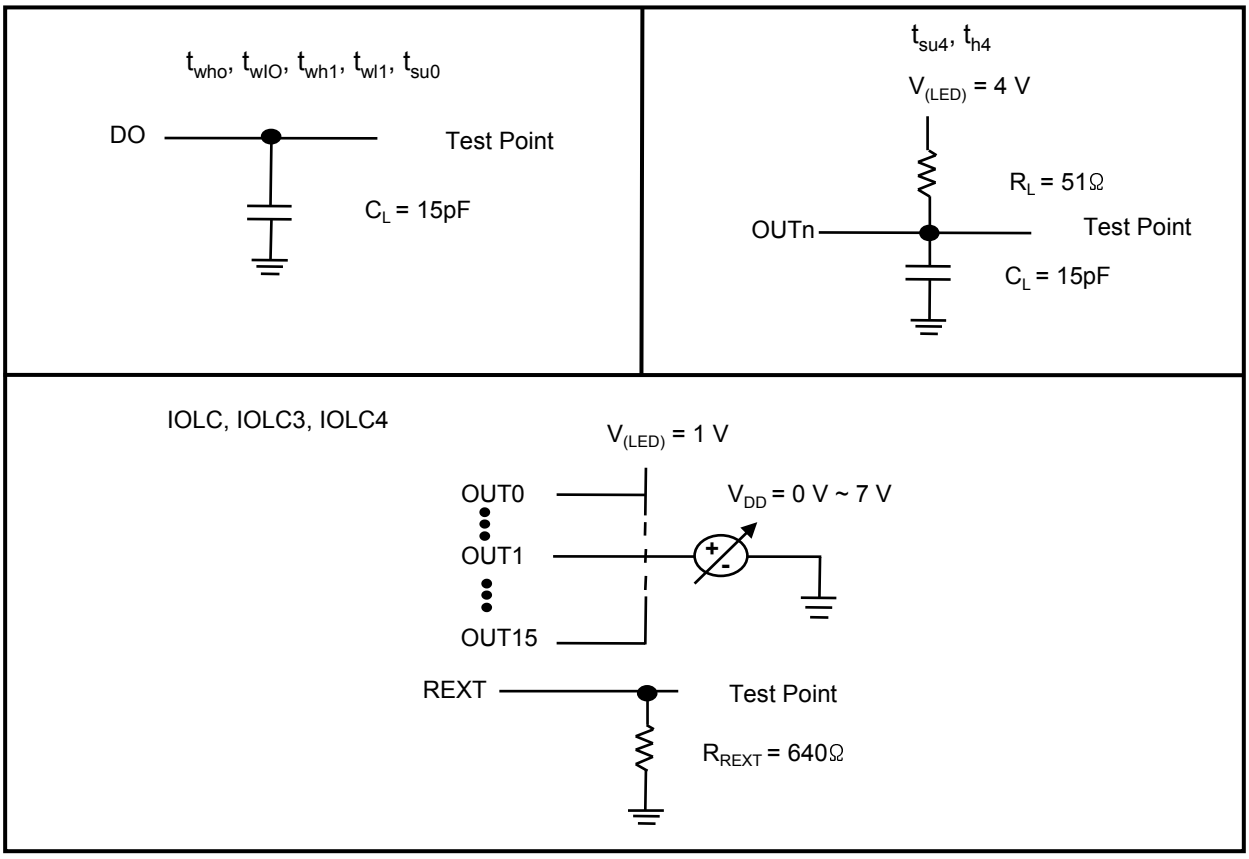
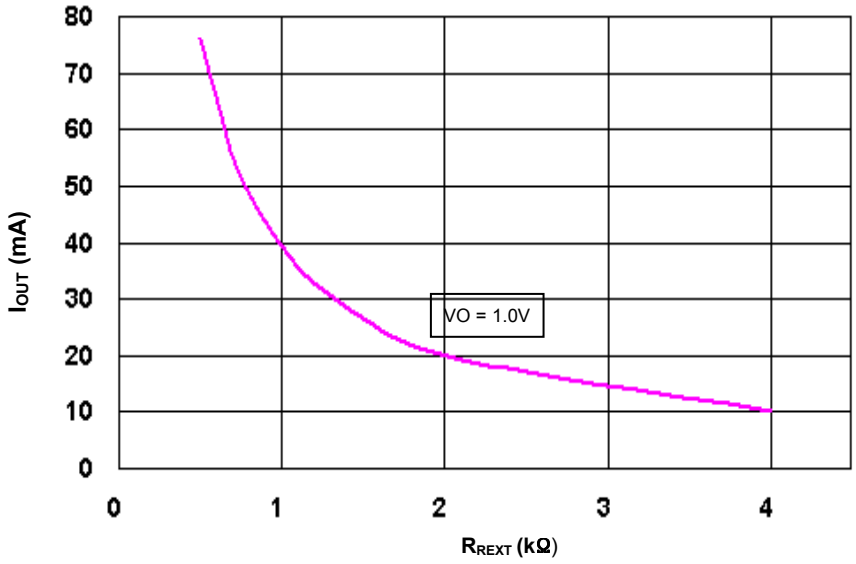


Figure 2. Parameter Measurement Circuits

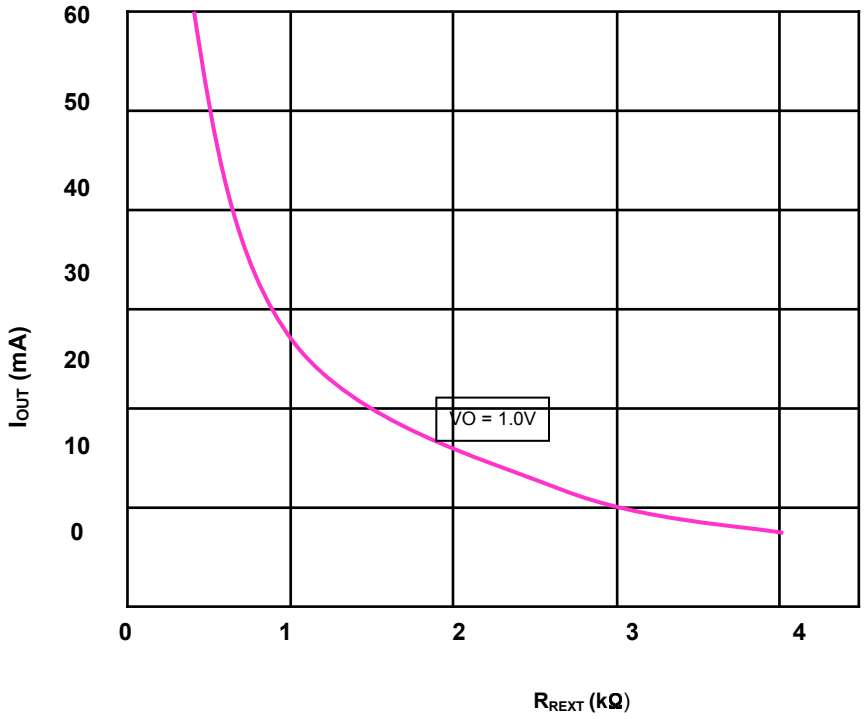
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Typical Characteristics



R_{REXT}	I_{OUT}
0.50 kΩ	76mA
0.72kΩ	54mA
0.99 kΩ	40mA
1.28 kΩ	31mA
1.97 kΩ	20mA
4.00 kΩ	10mA

Figure 3. R_{REXT} vs. I_{OUT} for DC Mode = 6Bit @V_{DD}=5.5V



R_{REXT}	I_{OUT}
0.48 kΩ	60mA
0.55 kΩ	52.5mA
0.64 kΩ	45mA
0.79 kΩ	37.5mA
0.96 kΩ	30mA
1.28 kΩ	22.5mA
1.92 kΩ	15mA
3.84 kΩ	7.5mA

Default Value

Figure 4. R_{REXT} vs. I_{OUT} for DC Mode = 8Bit @V_{DD}=5.5V

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Typical Characteristics (continued)

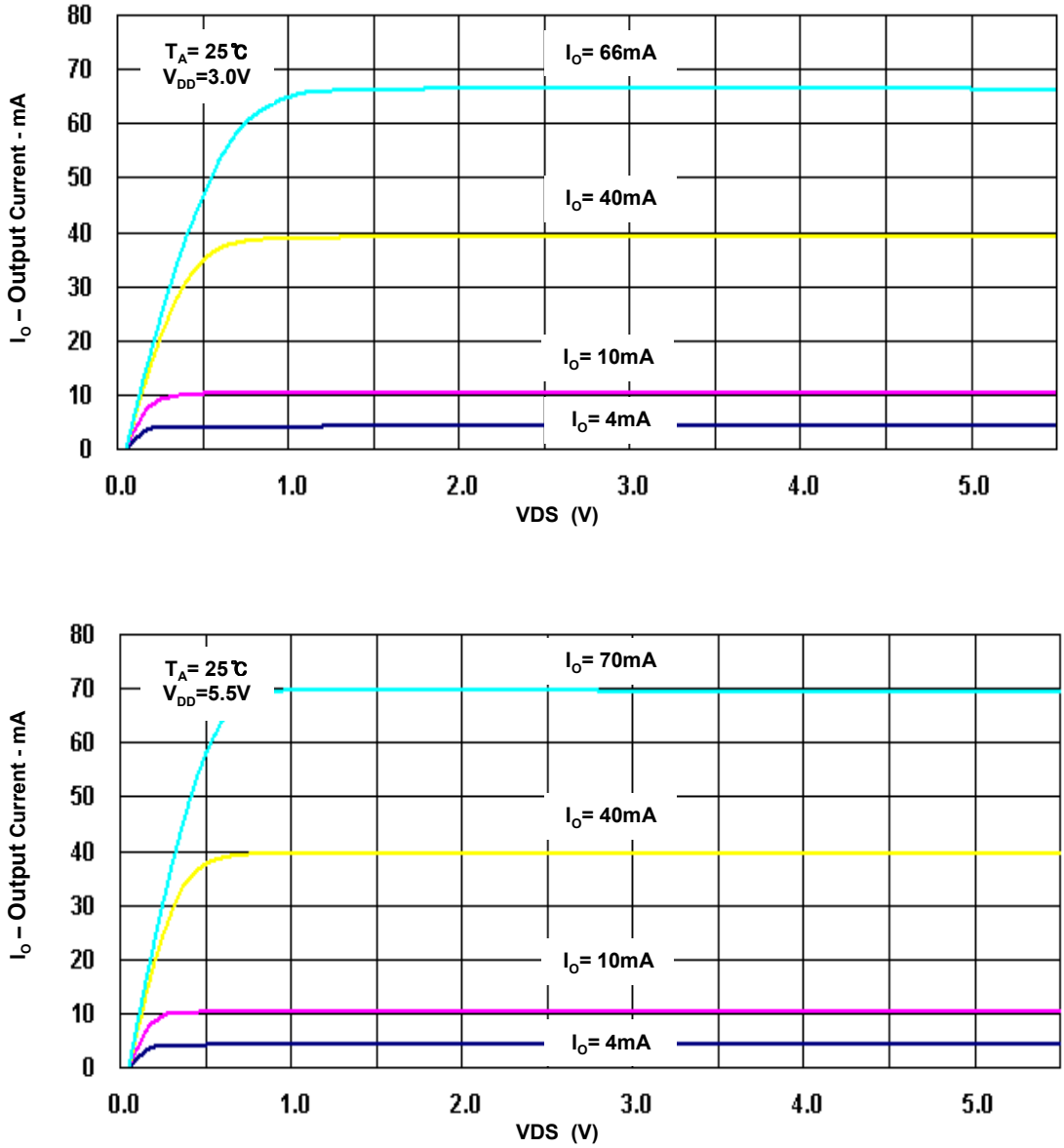


Figure 5. V_{DS} vs. I_{OUT} for DC Mode = 6Bit

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Typical Characteristics (continued)

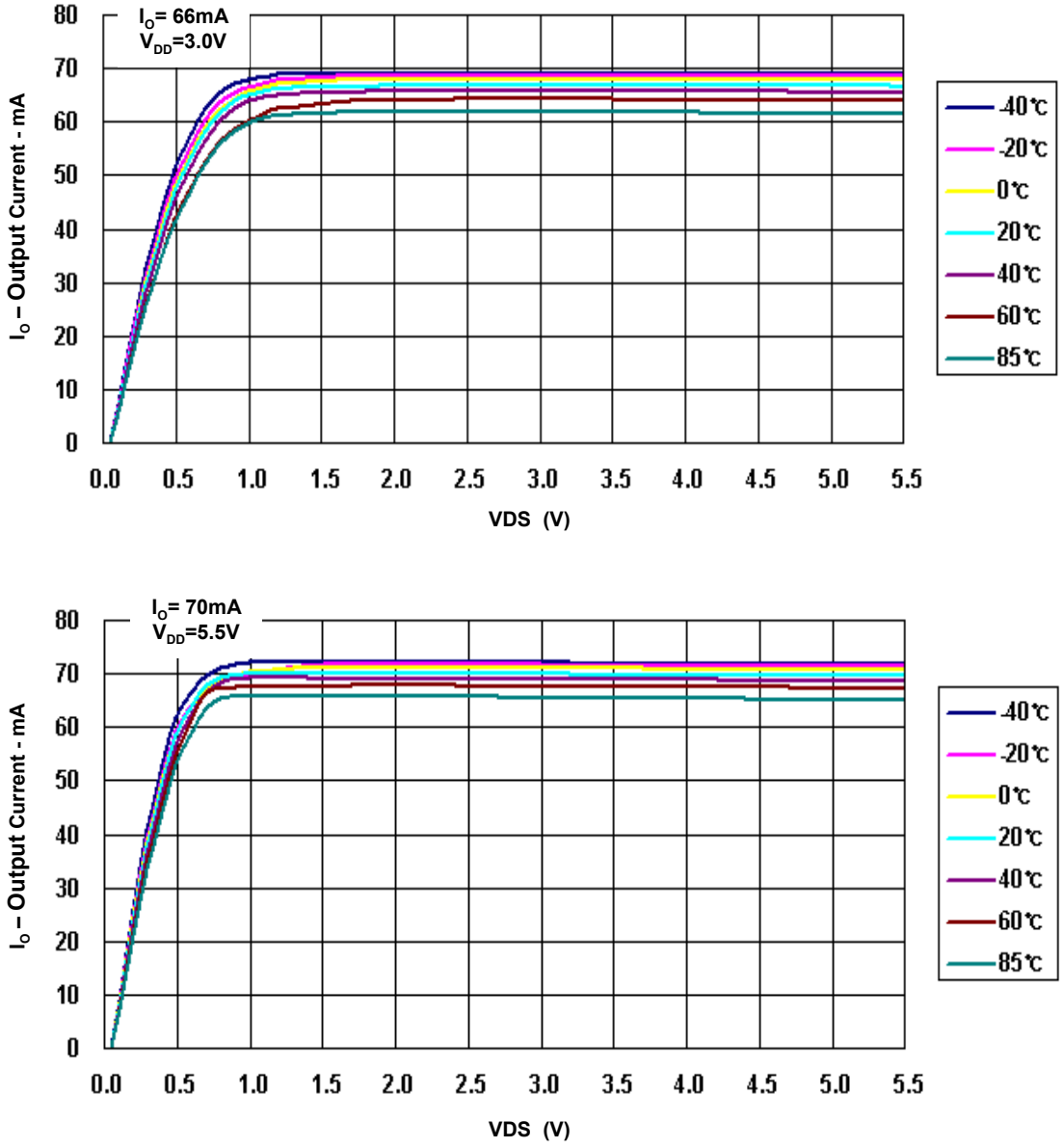
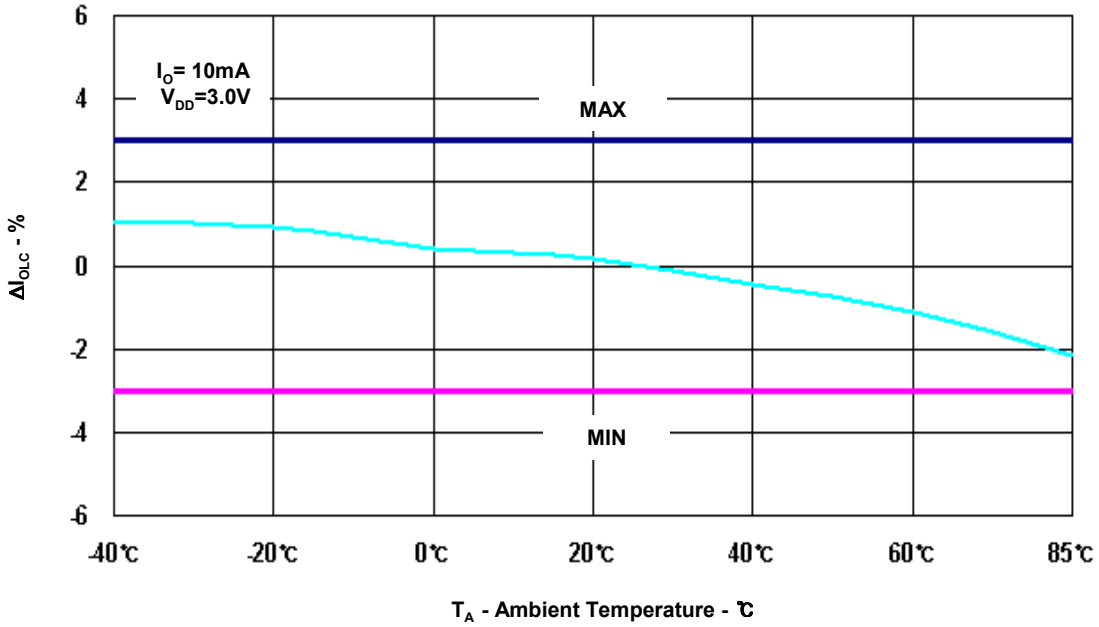


Figure 6. V_{DS} vs. I_{OUT} for DC Mode = 6Bit by Temp.

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Typical Characteristics (continued)



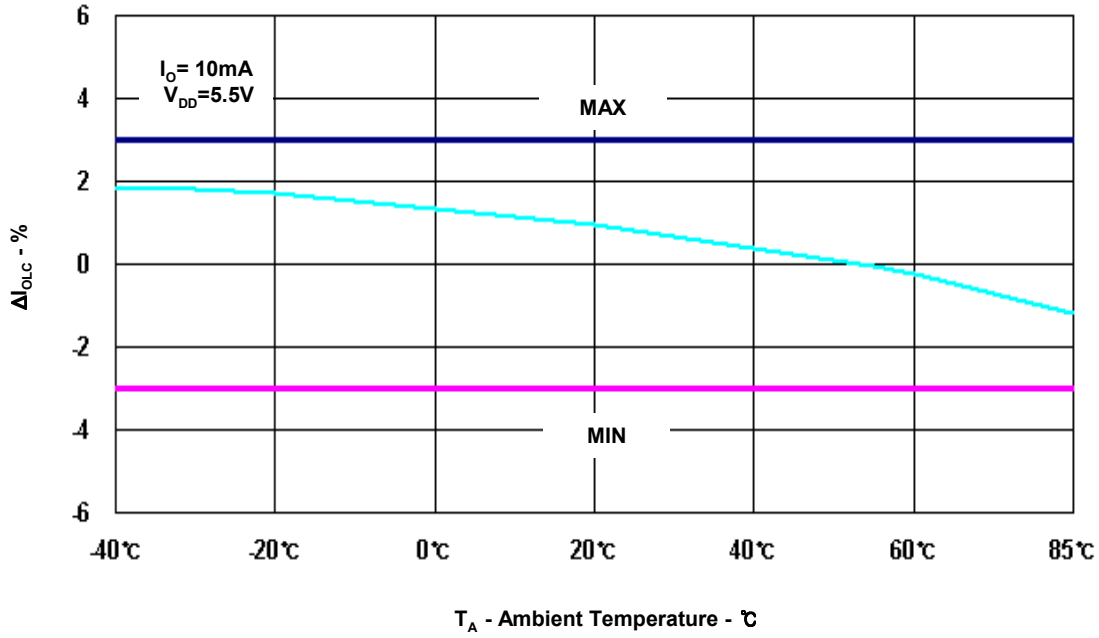


Figure 7-1. DELTA OUTPUT CURRENT VS FREE AIR TEMPERATURE (10mA)

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Typical Characteristics (continued)

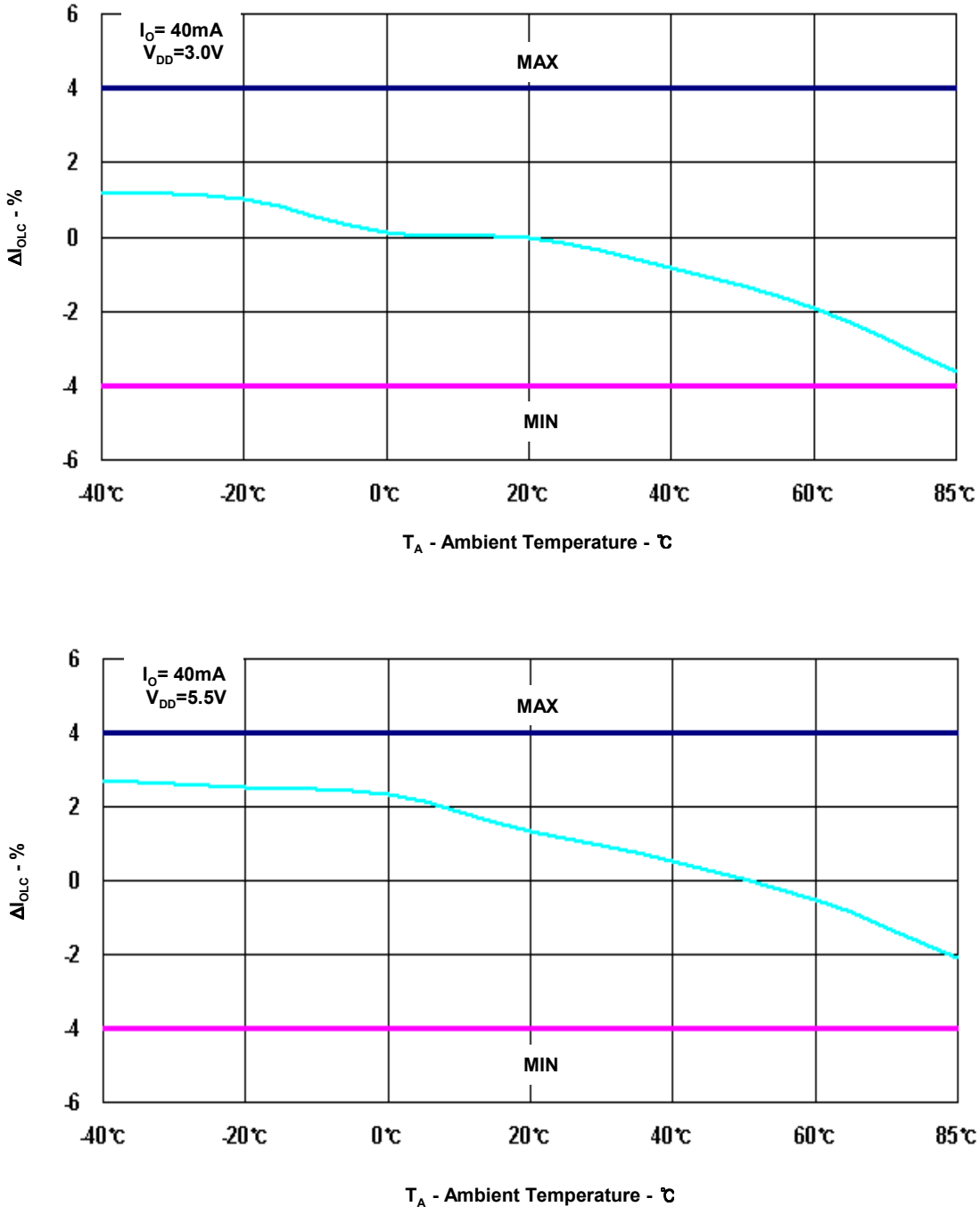


Figure 7-2. DELTA OUTPUT CURRENT VS FREE AIR TEMPERATURE (40mA)

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Typical Characteristics (continued)

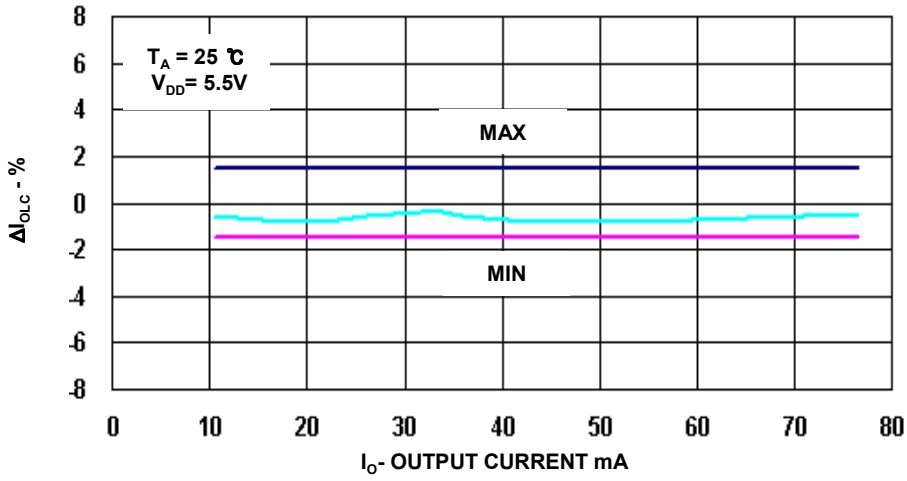


Figure 8. DELTA OUTPUT CURRENT VS OUTPUT CURRENT

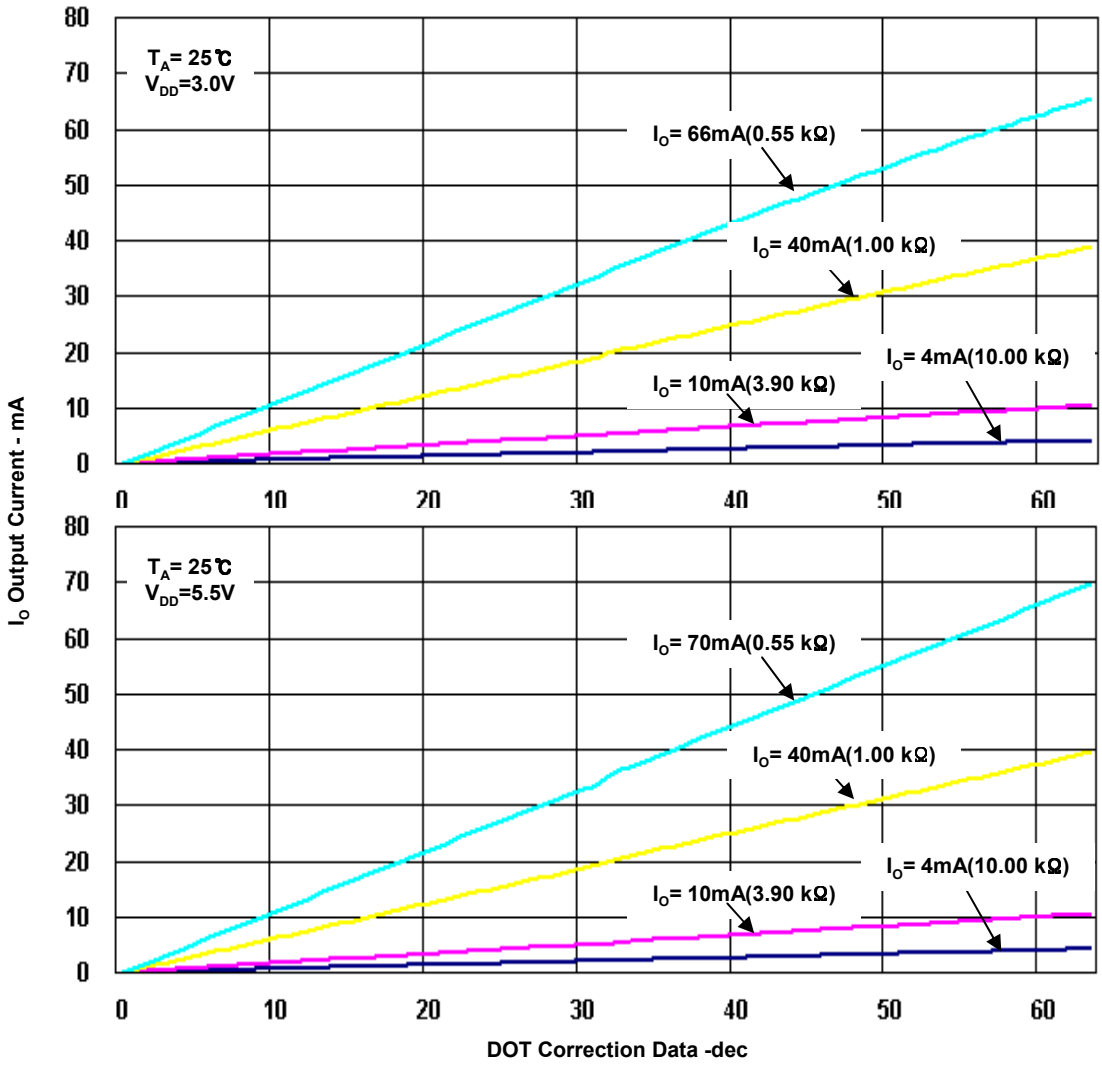
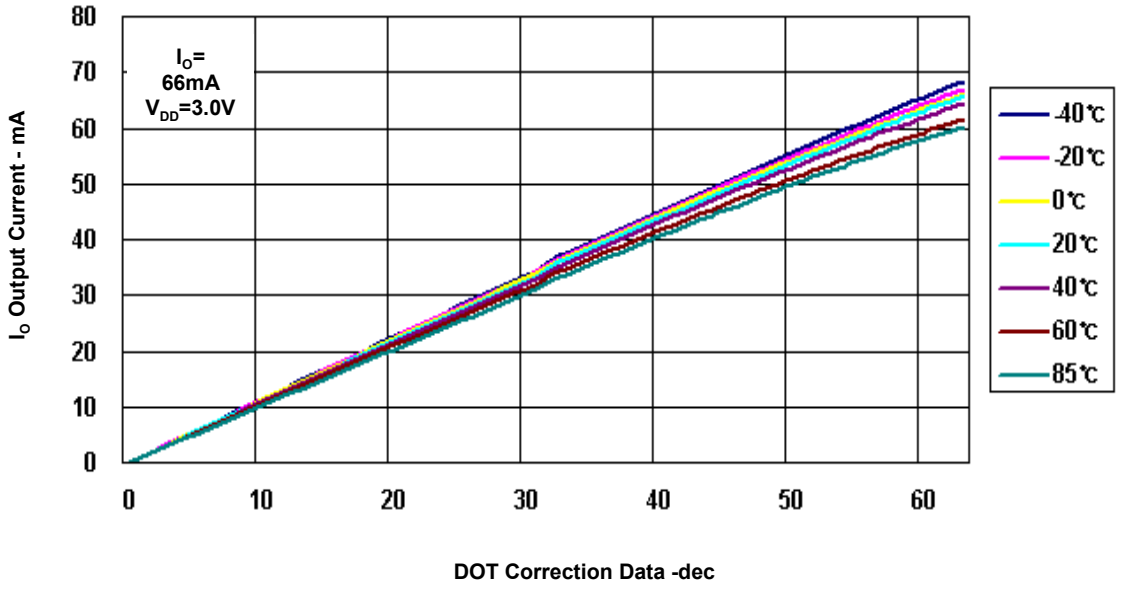


Figure 9. DOT CORRECTION LINEARITY (ABS Value) @DC Mode = 6Bit

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Typical Characteristics (continued)



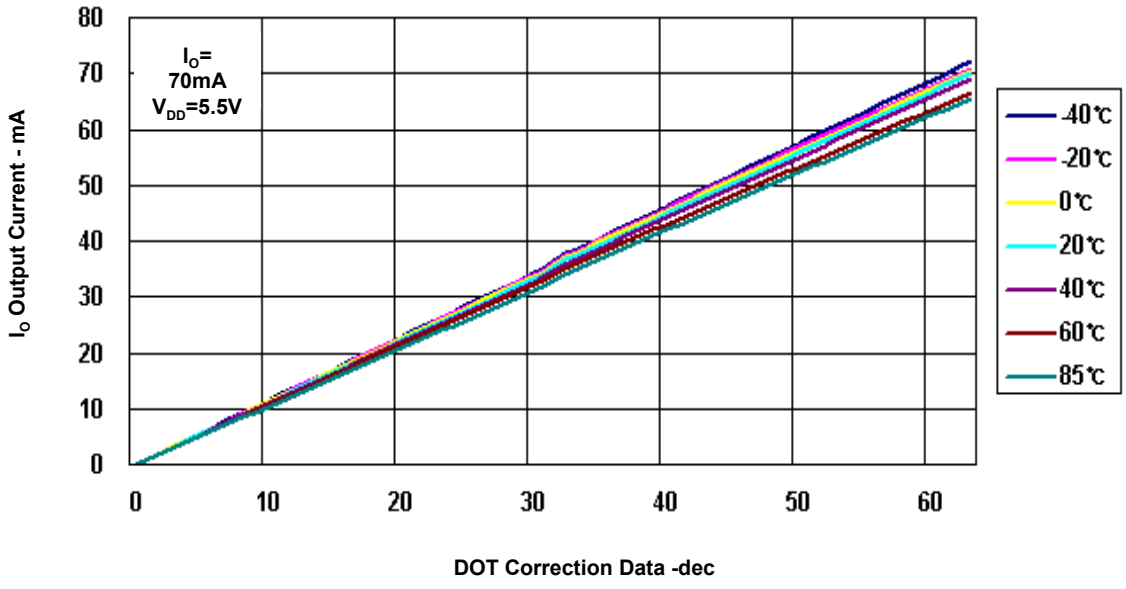


Figure 10. DOT CORRECTION LINEARITY (ABS Value) @DC Mode = 6Bit

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Typical Characteristics (continued)

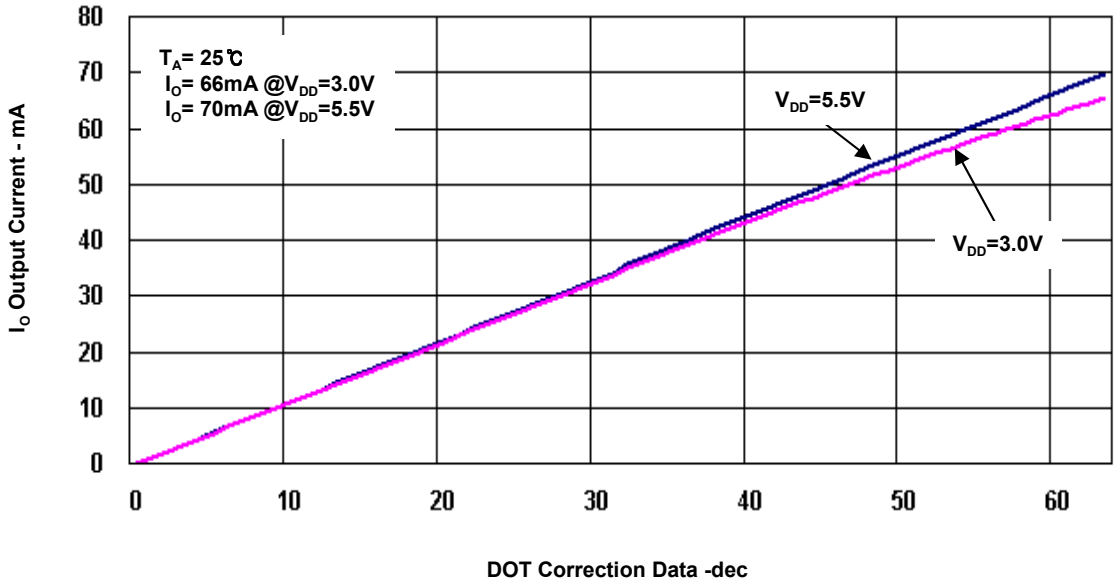


Figure 11. DOT CORRECTION LINEARITY (ABS Value)

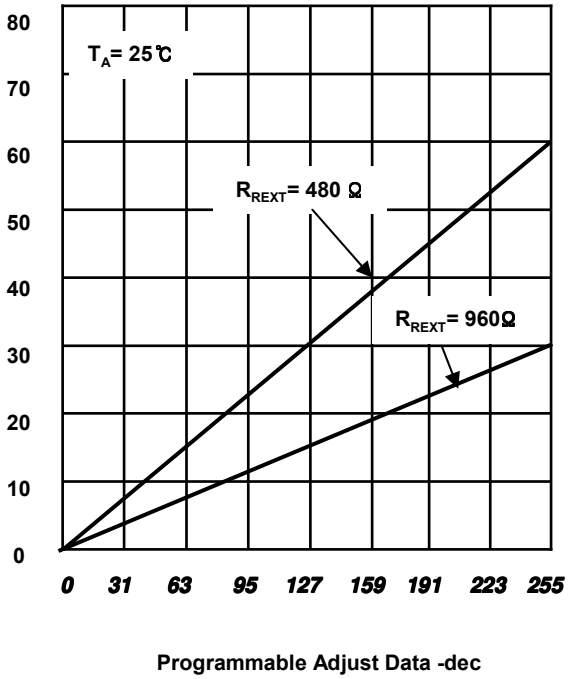


Figure 12. PROGRAMMABLE ADJUST DATAINEARITY (ABS Value)

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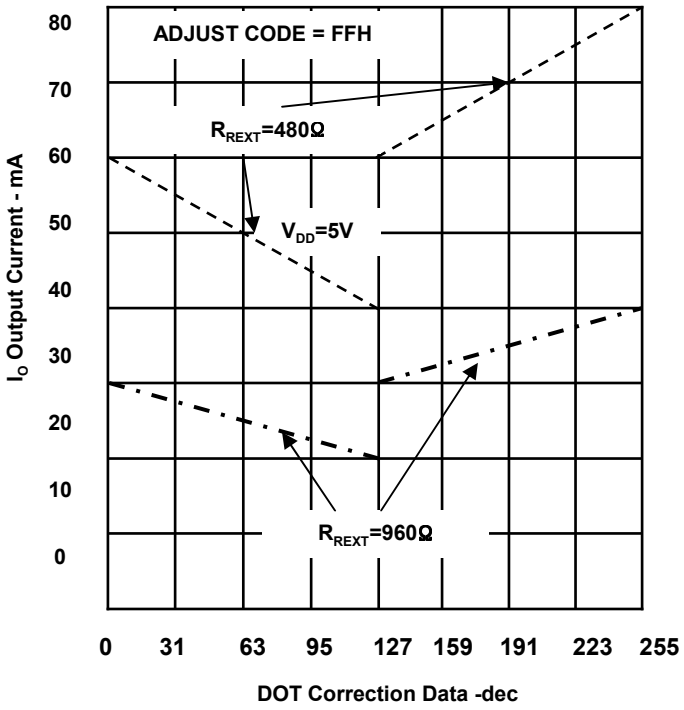


Figure 13. ADJUST Data (R_{REXT}=480K, ADUST Code =FFh)
&
DOT CORRECTION LINEARITY (ABS Value)

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PRINCIPLES OF OPERATION

SERIAL INTERFACE

The LD1072 has a serial interface, which can be connected to microcontrollers or digital signal processors. Only 3 pins are needed to input data into the device. The rising edge of CLK signal shifts the data from the DIN pin to the internal register. After all data is clocked in, a high-level pulse of ST signal latches the serial data to the internal registers. The internal registers are level-triggered latches of ST signal. All data are clocked in with the MSB first. The length of serial data is 96 bit or 192 bit, depending on the programming mode. PWM data and dot correction data can be entered during a PWM cycle. Although new PWM data can be clocked in during a PWM cycle, the ST signal should only latch the PWM data at the end of the PWM cycle. Latching in new PWM data immediately overwrites the existing PWM data. Figure 14 shows the timing chart. More than two LD1072s can be connected in series by connecting an DO pin from one device to the DIN pin of the next device. An example of cascading two LD1072s is shown in Figure 14. The DO pin can also be connected to the controller to receive status information from LD1072 as shown in Figure 29.

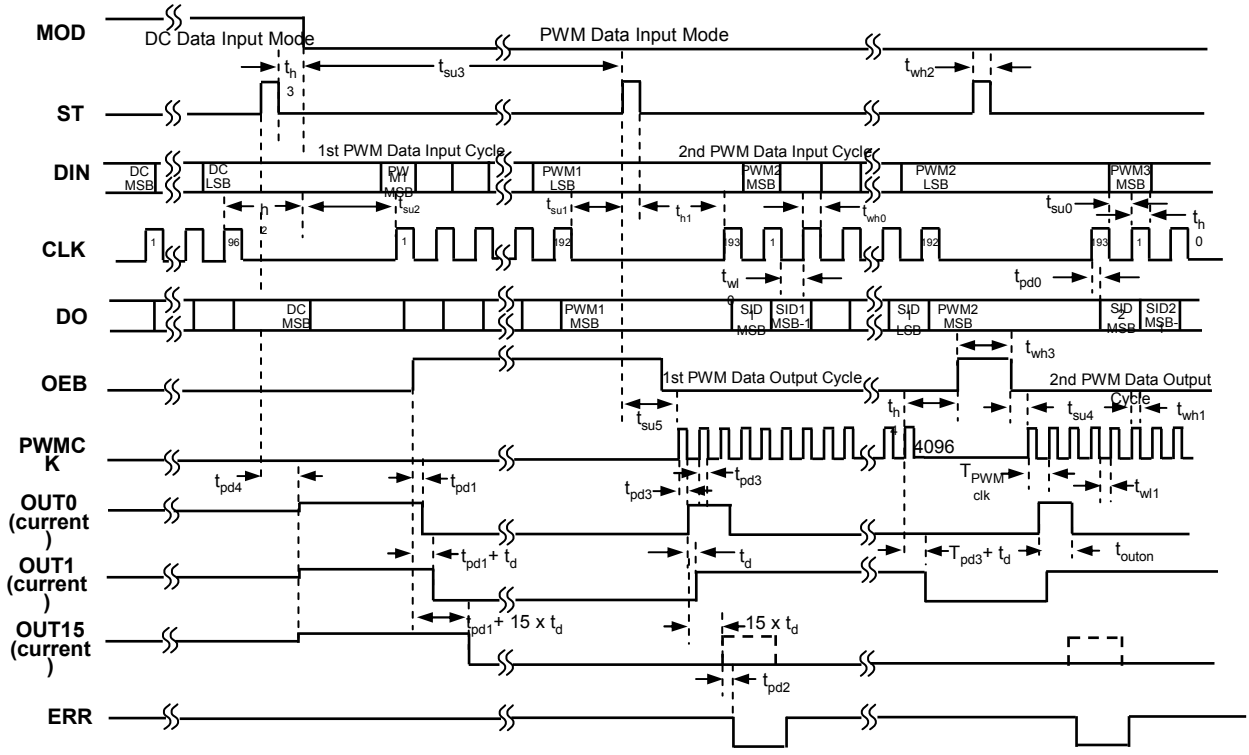


Figure 14. Serial Data Input Timing Chart

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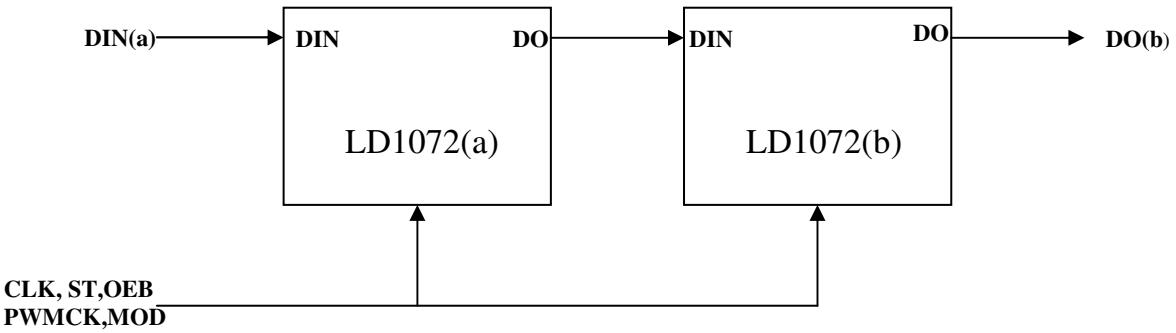


Figure 15. Cascading Two LD1072 Devices

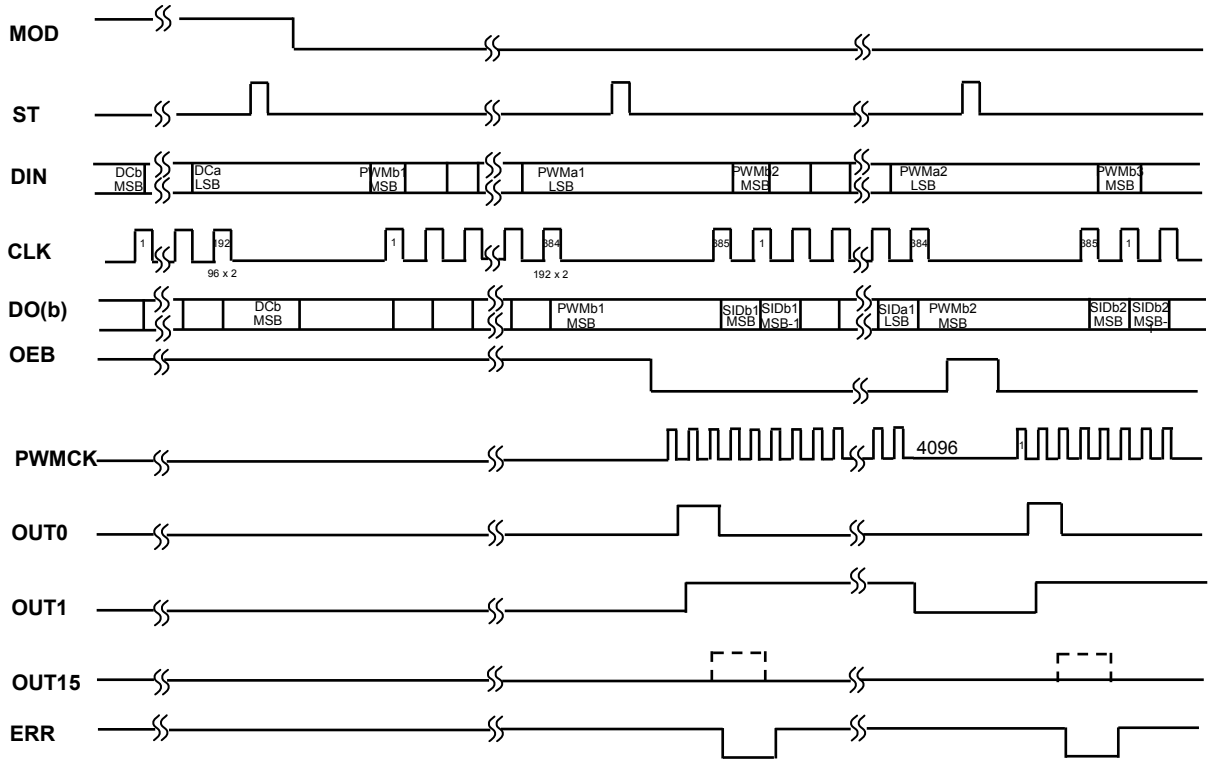


Figure 16. Timing Chart for Two Cascaded LD1072 Devices

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ERROR INFORMATION OUTPUT

The open-drain output ERR is used to report both of the LD1072 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the ERR pin is turned off. The voltage on ERR is pulled up to VDD through an external pull up resistor. If TEF or LOD is detected, the internal transistor is turned on, and ERR is pulled to GND. Because ERR is an open-drain output, multiple ICs can be ORed together and pulled up to VDD with a single pull up resistor. This reduces the number of signals needed to report a system error (see Figure 28)

To differentiate LOD and TEF signal from ERR pin, LOD can be masked out with OEB = HIGH.

Table 2. ERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUTn VOLTAGE	TEF	LOD	OEB	ERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	OUTn > $V_{(LED)}$	L	L	L	H
	OUTn < $V_{(LED)}$	L	H		L
$T_J > T_{(TEF)}$	OUTn > $V_{(LED)}$	H	L		L
	OUTn < $V_{(LED)}$	H	H		L

TEF : THERMAL ERROR FLAG

The LD1072 provides a temperature error flag (TEF) circuit to indicate an over temperature condition of the IC. If the junction temperature exceeds the threshold temperature (160C typical), TEF becomes H and ERR pin goes to low level and COUT Current reduced to about 50%. When the junction temperature becomes lower than the threshold temperature, TEF becomes L and ERR pin becomes high impedance and Cout current is increased to 100%. TEF status can also be read out from the LD1072 status register.

LOD : LED OPEN DETECTION

The LD1072 has an LED-open detection circuit that detects broken or disconnected LED's. The LED open detector pulls the ERR pin to GND when an open LED is detected. ERR and the corresponding error bit in the Status Information Data is only active under the following open LED conditions.

1. OUTn is on and the time tpd2 (1ms typical) has passed.
2. The voltage of OUTn is < 0.3V (typical)

The LOD status of each output can be also read out from the DO pin. See the STATUS INFORMATION OUTPUT section for details. The LOD error bits are latched into the Status Information Data when ST returns to a low after a high. Therefore, the ST pin must be pulsed high then low while ERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

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DELAY BETWEEN OUTPUTS

The LD1072 has graduated delay circuits between outputs. These circuits can be found in the constant current driver block of the device (see the functional block diagram). The fixed-delay time is 2ns (typical), OUT0 has no delay, OUT1 has 2ns delay, and OUT2 has 4ns delay, etc. The maximum delay is 30ns from OUT0 to OUT15. The delay works during switch on and switch off of each output channel. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

OUTPUT ENABLE

All OUTn channels of the LD1072 can be switched off with one signal. When OEB is set high, all OUTn channels are disabled, regardless of logic operations of the device. The PWM counter is also reset. When OEB is set low, all OUTn channels work under normal conditions. If OEB goes low and then back high again in less than 30ns, all outputs programmed to turn on still turn on for either the programmed number of PWM clocks, or the length of time that the OEB signal was low, which ever is lower. For example, if all outputs are programmed to turn on for 1ms, but the OEB signal is only low for 200ns, all outputs still turn on for 200ns, even though some outputs are turning on after the OEB signal has already gone high.

Table 3. OEB Signal Truth Table

OEB	OUT0 - OUT15
LOW	OUTn are controlled by PWM clock
HIGH	Disabled

SETTING MAXIMUM CHANNEL CURRENT

The maximum output current per channel is programmed by a single resistor, $R_{(REXT)}$, which is placed between REXT pin and GND pin. The voltage on REXT is set by an internal band gap $V_{(REXT)}$ with a typical value of 1.18 V. The maximum channel current is equivalent to the current flowing through $(40+R_{(REXT)})$ multiplied by a factor of 35. The maximum output current can be calculated by Equation 6:

$$I_{MAX}[A] = \{1.18/(40+R_{(REXT)})\} * 35 \quad (6)$$

- $V_{(REXT)}$ = 1.18 V
- $R_{(REXT)}$ = User-selected external resistor.

I_{MAX} must be set between 5mA and 80mA. The output current may be unstable if I_{MAX} is set lower than 5mA. Output currents lower than 5mA can be achieved by setting I_{MAX} to 5mA or higher and then using dot correction.

Figure 3 shows the maximum output current IO versus $R_{(REXT)}$. $R_{(REXT)}$ is the value of the resistor between REXT terminal to GND, and IO is the constant output current of OUT0 to OUT15. A variable power supply may be connected to the REXT pin through a resistor to change the maximum output current per channel. The maximum output current per channel is 35 times the current flowing out of the REXT pin.

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POWER DISSIPATION CALCULATION

The device power dissipation needs to be below the power dissipation rate of the device package to ensure correct operation. Equation 7 calculates the power dissipation of device:

$$P_D=(V_{DD} \text{ X } I_{DD}) + (V_{OUT} \text{ X } I_{MAX} \text{ X N X } DC_n/63 \text{ x } d_{PWM} \text{)} \quad (7)$$

- V_{DD}: device supply voltage
- I_{DD}: device supply current
- V_{OUT}: LD1072 OUTn voltage when driving LED current
- I_{MAX}: LED current adjusted by $R_{(REXT)}$ Resistor
- DCn: maximum dot correction value for OUTn
- N: number of OUTn driving LED at the same time
- d_{PWM}: duty cycle defined by OEB pin or PWM value

OPERATING MODES

The LD1072 has two operating modes defined by MOD as shown in Table 4. The PWM and DC registers are set to random values that are not known just after power on. The PWM and DC values must be programmed before turning on the outputs. Please note that when initially setting PWM and DC data after power on, the PWM data must be set before the DC data is set. Failure to set PWM data before DC data may result in the first bit of PWM data being lost. ST must be low when the MOD pin goes high-to-low or low-to-high to change back and forth between PWM mode and DC mode.

Table 4. LD1072 Operating Modes Truth Table

MOD	DC	INPUT SHIFT REGISTER	OPERATING MODE
LOW	-	192bit	Grayscale PWM Mode
HIGH	VDD	96bit	6-Bit Dot Correction Data Input Mode
	GND	128bit + 8Bit	8-Bit Dot Correction Data & Programmable Adjust Data Input Mode

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SETTING DOT CORRECTION

The LD1072 has the capability to fine-adjust the output current of each channel (OUT0 to OUT15) independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current Imax. The DC pin must be connected to VDD to ensure proper operation of the dot correction circuitry. Equation 8 determines the output current for each output n:

$$I_{OUTn} = I_{max} \text{ X } DCn/63 \text{ (n= 0 to 15)} \quad (8)$$

- **Imax = the maximum programmable output current for each output.**
- **DCn = the programmed dot correction value for output n (DCn = 0 to 63)**

Figure 17 shows the dot correction data packet format which consists of 6 bits x 16 channel, total 96 bits. The MSB is transmitted first, followed by the MSB-1, etc. The DC 15.5 in Figure 17 stands for the 5th-most significant bit for output 15.

Figure 18 shows the dot correction data packet format which consists of 8 bits x 16 channel, total 128 bits. The MSB is transmitted first, followed by the MSB-1, etc. The DC 15.7 in Figure 18 stands for the 7th-most significant bit for output 15.

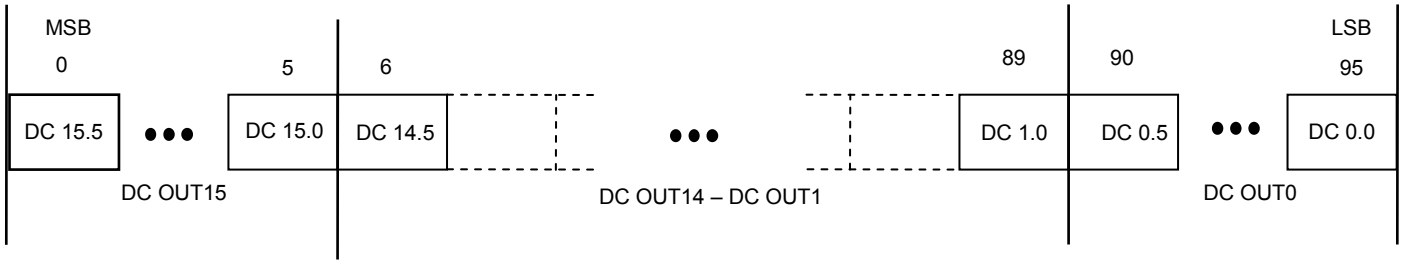


Figure 17. 6Bit Dot Correction Data Packet Format

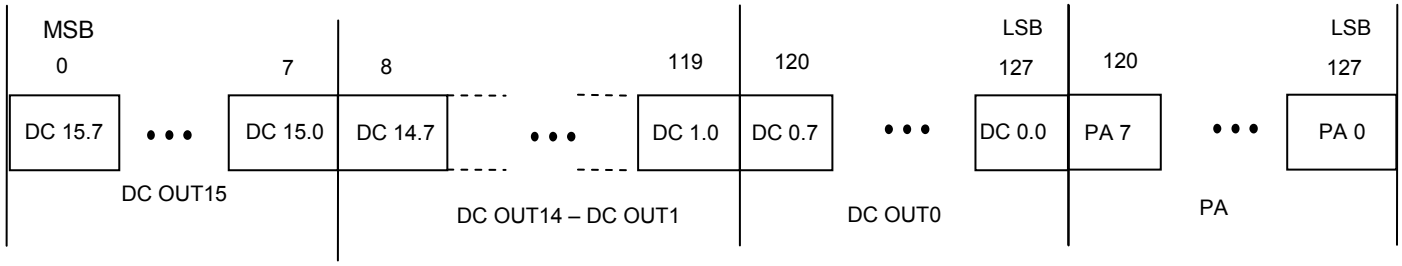


Figure 18. 8Bit Dot Correction Data & Programmable Adjust Data Packet Format

When MOD is set to VDD, the LD1072 enters the dot correction data input mode. The length of input shift register becomes 96bits when DC=VDD. The length of input shift register becomes 136bits when DC=GND. 8Bit of DC8 Bit is Programmable Adjust Data. After all serial data are shifted in, the LD1072 writes the data in the input shift register to DC register when ST is high, and holds the data in the DC register when ST is low. The DC register is a level triggered latch of ST signal. Since ST is a level-triggered signal, CLK and DIN must not be changed while ST is high. After ST goes low, data in the DC register is latched and does not change. OEB signal does not need to be high to latch in new data. When ST goes high, the new dot-correction data immediately becomes valid and changes the output currents if OEB is low. ST has setup time (tsu1) and hold time (th1) to CLK as shown in Figure 14.

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To input data into the dot correction register, MOD must be set to VDD. The internal input shift register is then set to 96-bit width when DC= VDD. The internal input shift register is then set to 128-bit width when DC= GND. After all serial data are clocked in, a rising edge of ST is used to latch the data into the dot correction register. Figure 19 shows the 6bit dc data input timing chart. Figure 20 shows the 8bit dc data input timing chart.

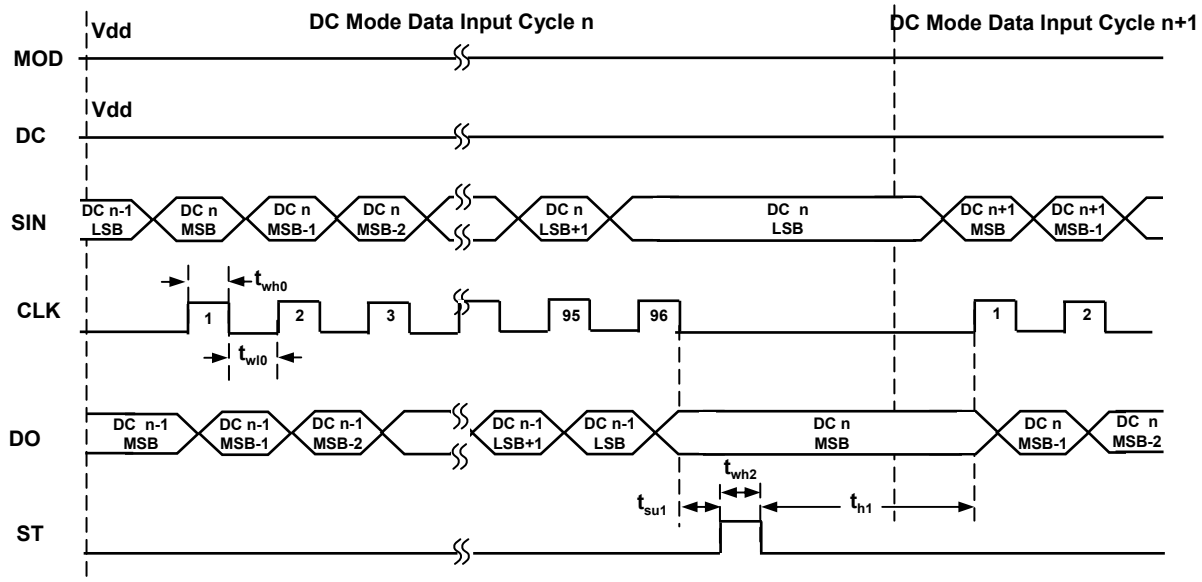


Figure 19. 6Bit Dot Correction Data Input Timing Chart

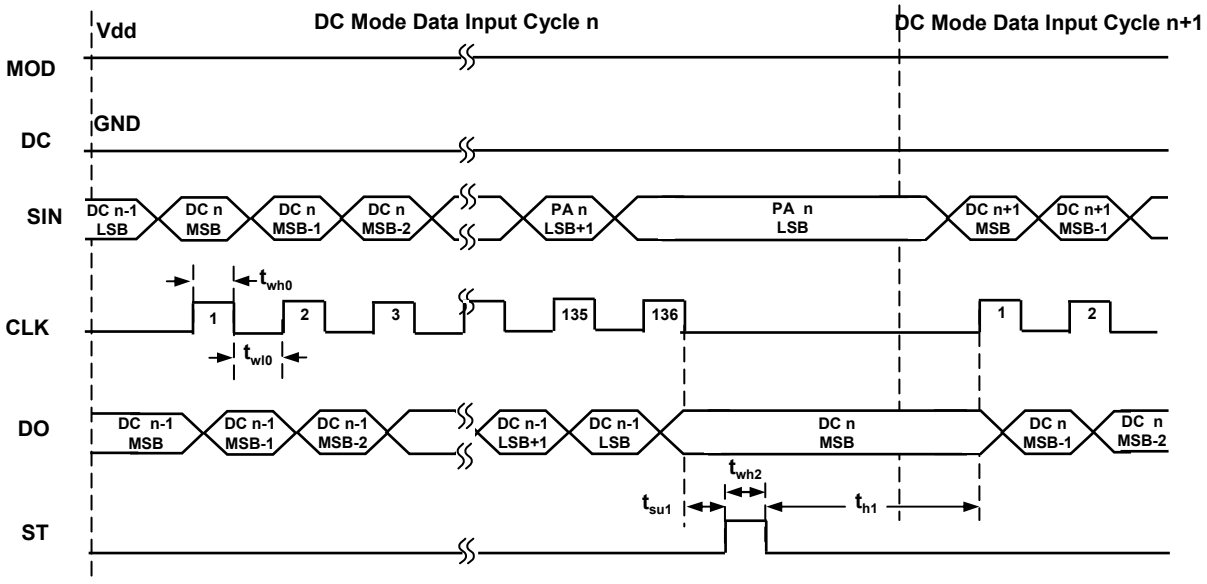


Figure 20. 8Bit Dot Correction Data & Programmable Adjust Data Input Timing Chart

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Table5. The relation 8-Bit DC Data and Output Current

DC[7:0]		OUT Current	DC[7:0]		OUT Current
DC[7]	DC[6:0]		DC[7]	DC[6:0]	
0	0	Setting Current* 100%	1	0	Setting Current * 100.27%
0	1	Setting Current * 99.73%	1	1	Setting Current * 100.54%
0	2	Setting Current* 99.46%	1	2	Setting Current * 100.81%
0	3	Setting Current * 99.19%	1	3	Setting Current * 101.08%
• •	• •	• •	• •	• •	• •
0	124	Setting Current * 66.52%	1	124	Setting Current* 133.75%
0	125	Setting Current *66.25%	1	125	Setting Current * 134.02%
0	126	Setting Current * 65.98%	1	126	Setting Current* 134.29%
0	127	Setting Current * 65.71%	1	127	Setting Current * 134.56%

PROGRAMABLE ADJUST MODE

The relation 8Bit Programmable Adjust Data and Output Current

$$I_{OUTn} = I_{max} \text{ X } PAn/255 \quad (9)$$

- **Imax = the maximum output current assigned by external resistor.**
- **PAn : Programmable Adjust Data (255 ~0)**

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SETTING PWM

The LD1072 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, from 0% to 100% brightness. Equation 9 determines the brightness level for each output n:

$$\text{Brightness in \%} = \text{PWMn}/4095 \times 100 \quad (10)$$

- PWMn = the programmed PWM value for output n (PWMn = 0 to 4095) n = 0 to 15
- PWM data for all OUTn

The input shift register enters PWM data into the PWM register for all channels simultaneously. The complete PWM data format consists of 16 x 12 bit words, which forms a 192-bit wide data packet (see Figure 19). The data packet must be clocked in with the MSB first.

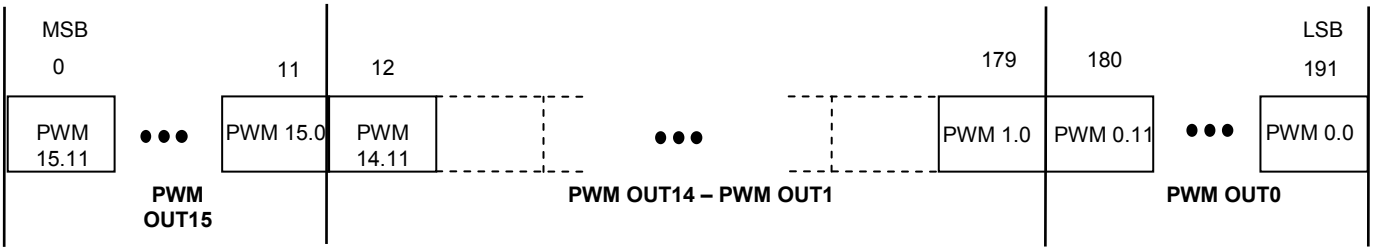


Figure 21. PWM Data Packet Format

When MOD is set to GND the LD1072 enters the PWM data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of the ST signal latches the data into the PWM register (see Figure 22). New PWM data immediately becomes valid at the rising edge of the ST signal; therefore, new PWM data should be latched at the end of a PWM cycle when OEB is high. The first PWM data input cycle after dot correction requires an additional CLK pulse after the ST signal to complete the PWM update cycle. All PWM data in the input shift register is replaced with status information data (SID) after updating the PWM register.

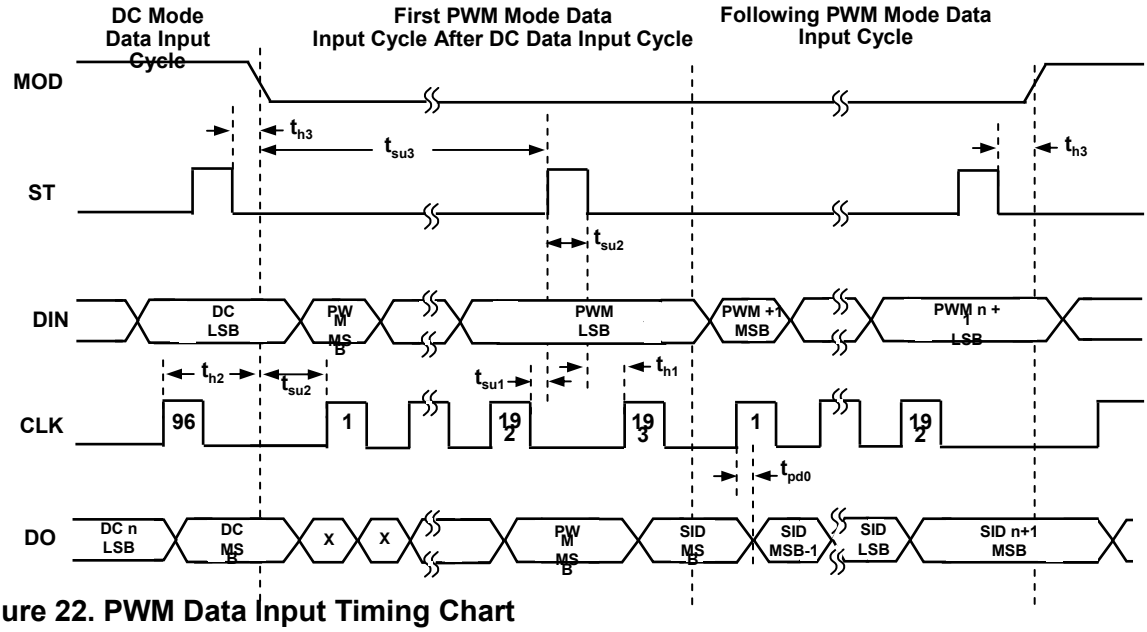


Figure 22. PWM Data Input Timing Chart

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STATUS INFORMATION OUTPUT

The LD1072 does have a status information register, which can be accessed in PWM mode (MOD = GND). After the ST signal latches the data into the PWM register, the input shift register data is replaced with status information data (SID) of the device (see Figure 21). LOD, TEF, and dot-correction register data can be read out at the DO pin. The status information data packet is 192 bits wide. Bits 0 - 15 contain the LOD status of each channel. Bit 16 contains the TEF status. Bits 24 - 119 contain the data of the dot-correction register. The remaining bits are reserved. The complete status information data packet is shown in Figure 23 an 24

DO outputs the MSB of the SID at the same time the SID are stored in the SID register, as shown in Figure 25. The next CLK pulse, which will be the clock for receiving the MSB of the next PWM data, transmits MSB-1 of SID. If output voltage is < 0.3 V (typical) when the output sink current turns on, LOD status flag becomes active. The LOD status flag is an internal signal which pulls ERR pin down to low when the LOD status flag becomes active. The delay time, tpd2 (1 us maximum), is from the time of turning on the output sink current to the time LOD status flag becomes valid. The timing for each channels LOD status to become valid is shifted by the 30-ns (maximum), channel-to-channel turn-on time. After the first PWMCK goes high, OUT0 LOD status is valid; tpd3 + tpd2 = 60 nS + 1 us = 1.06 us. OUT1 LOD status is valid; tpd3 + td + tpd2 = 60 ns + 2 ns + 1 us = 1.062us. OUT2 LOD status is valid; tpd3 + 2*td + tpd2 = 1.064us, and so on. It takes 1.51s maximum (tpd3 + 15*td + tpd2) from the first PWMCK rising edge until all LOD become valid; tsuLOD must be > 1.09us (see Figure 25) to ensure that all LOD data are valid.

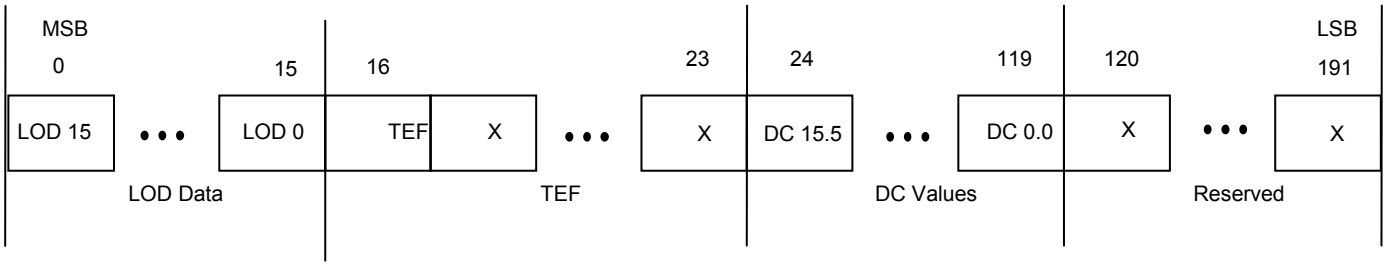


Figure 23. Status Information data packet is shown when DC 6Bit

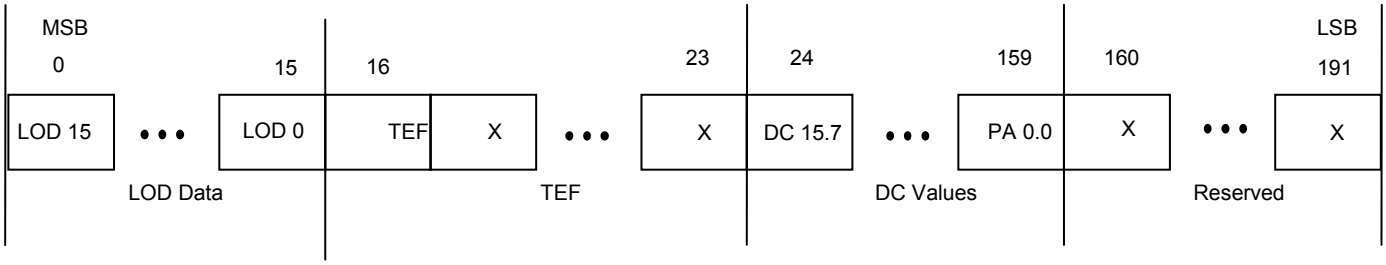


Figure 24. Status Information data packet is shown when DC 8Bit

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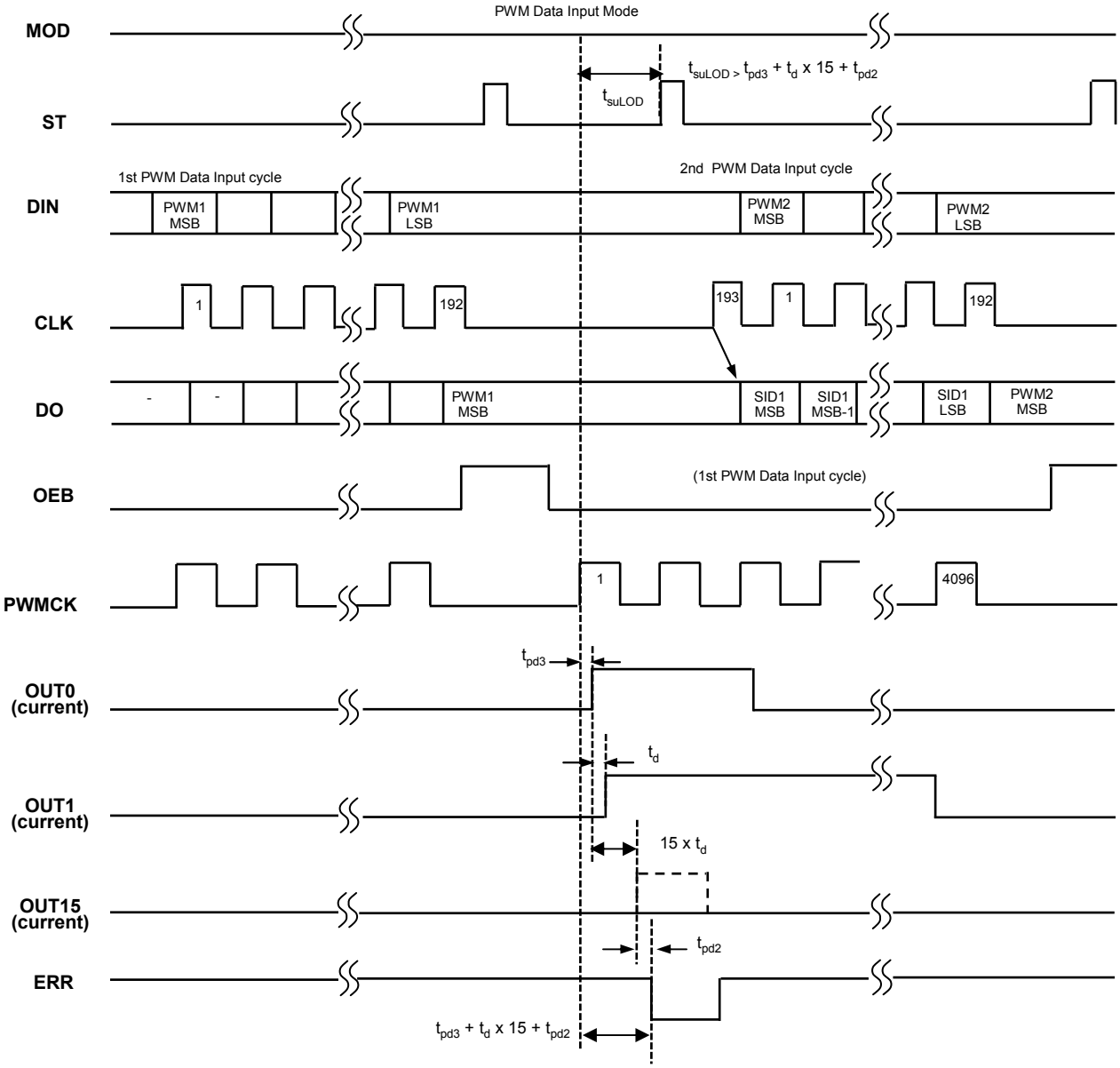


Figure 25. Readout Status Information Data (SID) Timing Chart

The LOD status of each output can be read out from the DO pin. The LOD error bits are latched into the Status Information Data when ST returns to a low after a high. Therefore, the ST pin must be pulsed high then low while ERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

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GRAYSCALE PWM OPERATION

The grayscale PWM cycle starts with the falling edge of OEB. The first PWMCLK pulse after OEB goes low increases the PWM counter by one and switches on all OUTn with PWM value not zero. Each following rising edge of PWMCLK increases the PWM counter by one. The LD1072 compares the PWM value of each output OUTn with the PWM counter value. All OUTn with PWM values equal to the counter values are switched off. A OEB=H signal after 4096 PWMCLK pulses resets the PWM counter to zero and completes the grayscale PWM cycle (see Figure 26). When the counter reaches a count of FFFh, the counter stops counting and all outputs turn off. Pulling OEB high before the counter reaches FFFh immediately resets the counter to zero.

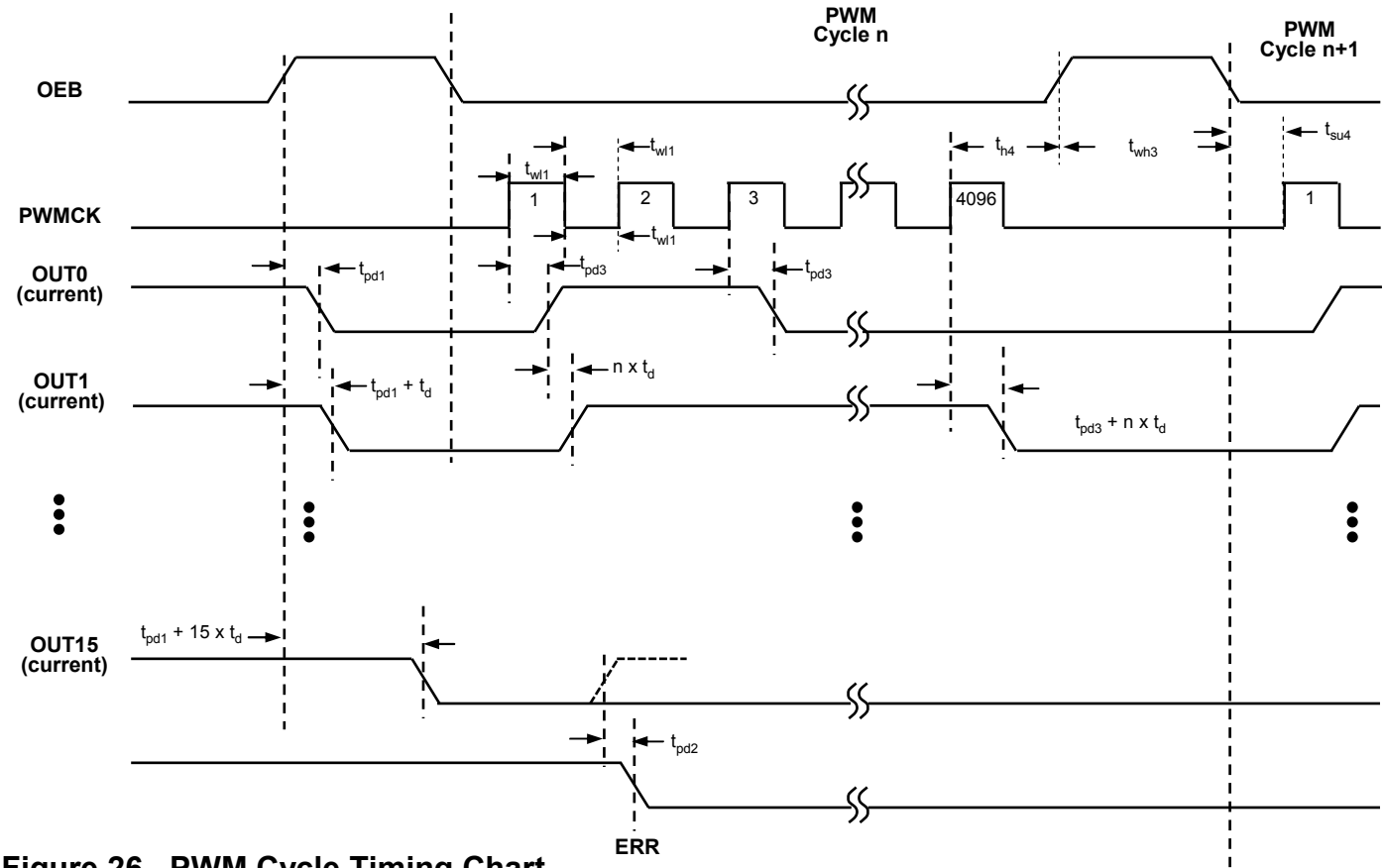


Figure 26. PWM Cycle Timing Chart

OUTPUT ON TIME

The amount of time that each output is turned on is a function of the PWM clock frequency and the programmed grayscale PWM value. The on-time of each output can be calculated using Equation 10.

$$T_on_n = PWMn/F(PWMCLK) + t_{on_err} \quad (11)$$

- T_onn is the time that OUTn turns on and sinks current
- PWMn is OUTn's programmed grayscale PWM value between 0 and 4095
- ton_err is the Output on time error defined in the Switching Characteristics Table

When using Equation 11 with very high PWMCLK frequencies and very low grayscale PWM values, the resulting T_on time may be negative. If T_on is negative, the output does not turn on. For example, using f(PWMCLK) = 30 MHz, PWMn = 1, and the typical ton_err = 50 nS, Equation 10 calculates that OUTn turns on for -16.6 nS. This output may not turn on under these conditions. Increasing the PWM value or reducing the PWMCLK clock frequency ensures turn-on.

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SERIAL DATA TRANSFER RATE

Figure 29 shows a cascading connection of n LD1072 devices connected to a controller, building a basic module of an LED display system. There is no LD1072 limitation to the maximum number of ICs that can be cascaded. The maximum number of cascading LD1072 devices depends on the application system and is in the range of 40 devices. Equation 12 calculates the minimum frequency needed:

$$f(PWMCK) = 4096 \times f(update) \qquad (12)$$

$$f(CLK) = 193 \times f(update) \times n$$

▪ f(PWMCK): minimum frequency needed for PWMCK f(CLK): minimum frequency needed for CLK and DIN f(update): update rate of whole cascading system n: number cascaded of LD1072 device

APPLICATION EXAMPLE

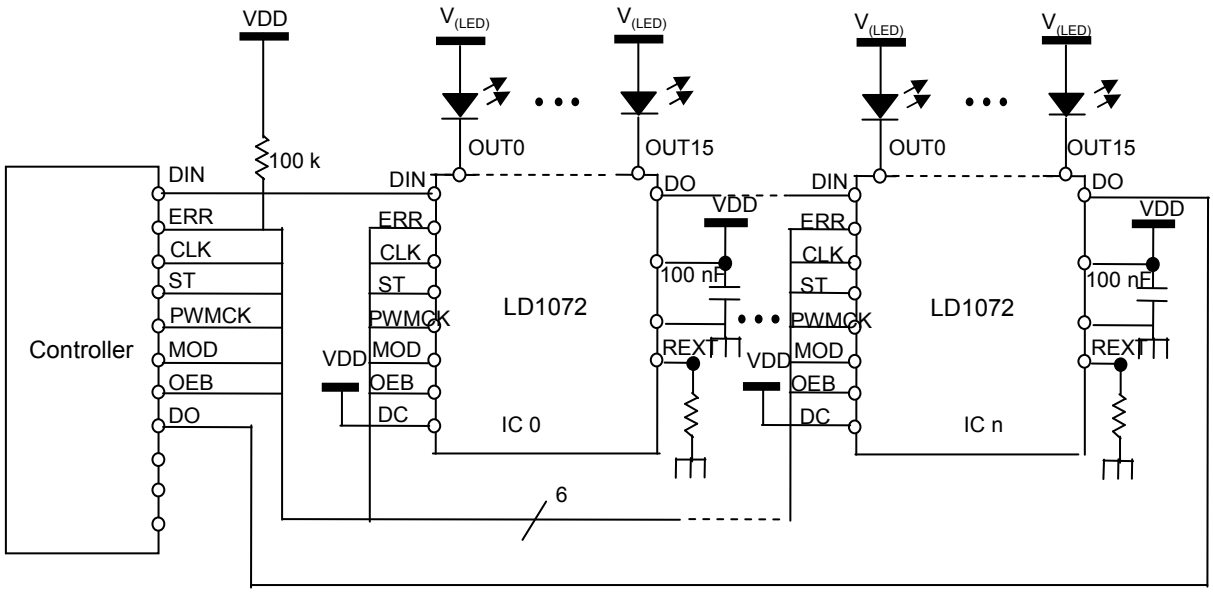
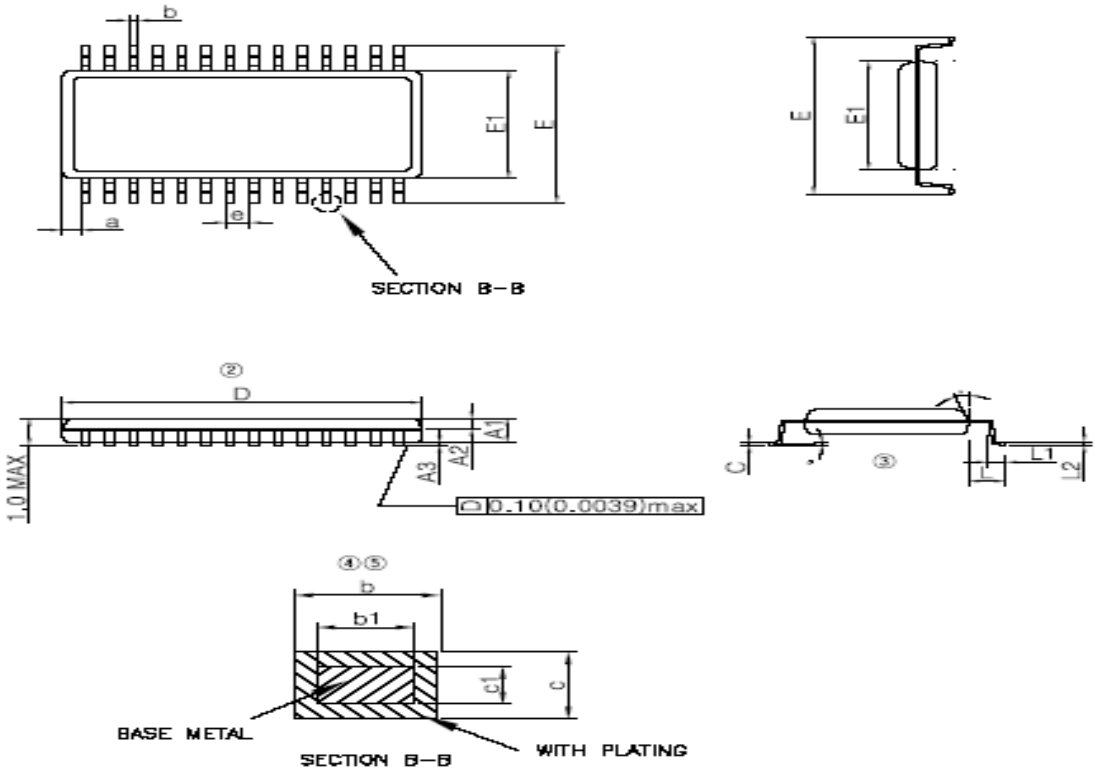


Figure 29. Cascading Devices

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PACKAGE INFORMATION

28 Pin TSSOP



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0.85	0.90	0.95
A2	–	–	0.43
A3	0.05	0.10	0.15
b	0.19	0.20	0.30
b1	–	–	0.22
c	0.09	–	0.20
c1	–	–	0.127
D	9.60	9.70	9.80
E	6.25	6.40	6.25
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.25	0.45	0.62
L1		1.0 REF	
a		0.50	
θ		12°REF	
θ 1		0° ~ 8°	

NOTES:

1. CONTROLLING DIMESION IN mm
②. DOES NOT INCLUDE MOLD FLASH, PROTRUSION
OR GATE BURRS MODE FLASH PROTURUSION
OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE
③. DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE
④. DOES NOT INCLUDE DAMBAR PROTRUSION
ALLOWBLE DAMBAR PROTRUSION SHALL BE 0.08mm.
⑤ CROSS SECTION B-B TO BE DETERMINED AT0.10 TO 0.25 mm FROM LEAD TIP
6. LEAD SPAN, STAND OFF HEIGHT, COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERSITIC
7. THIS OART COMPLIANT WITH JEDEC SPECFICATION MO-153 VARIATION AE

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