# WM8768

## 24-bit, 192kHz 8-Channel DAC

## DESCRIPTION

The WM8768 is a multi-channel audio DAC ideal for DVD and surround sound processing applications for home hi-fi, automotive and other audio visual equipment.

Four stereo 24-bit multi-bit sigma delta DACs are used with oversampling digital interpolation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 192kHz are supported. Each DAC channel has independent digital volume and mute control.

The audio data interface supports $I^2S$, left justified, right justified and DSP digital audio formats.

The device is controlled either via a 3 wire serial interface or directly using the hardware interface. These interfaces provide access to features including channel selection, volume controls, mutes, de-emphasis and power management facilities. The device is available in a 28-lead SSOP.

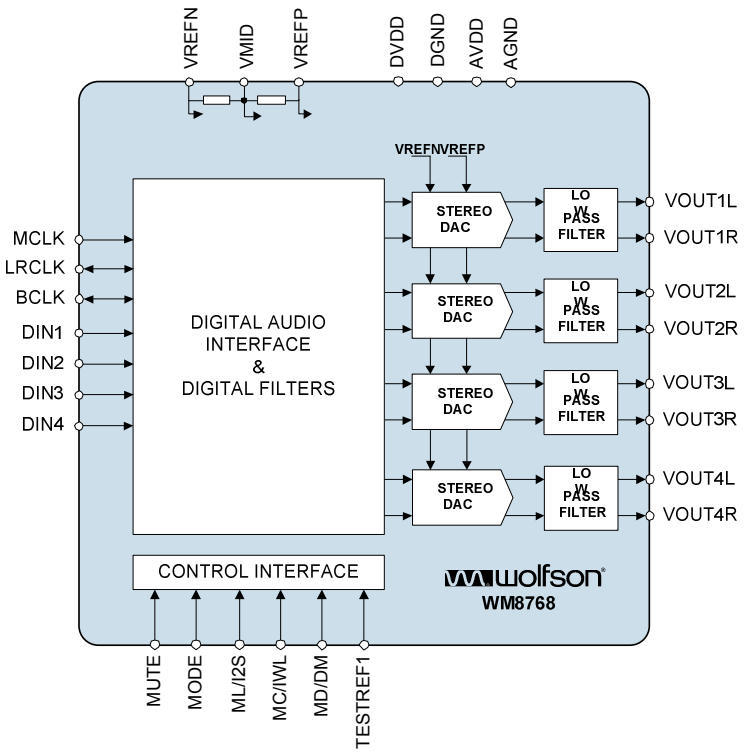
## FEATURES

- 8-Channel DAC with PCM.
- Audio Performance
  - 103dB SNR ('A' weighted @ 48kHz) DAC
- DAC Sampling Frequency: 8kHz – 192kHz
- 3-Wire SPI Serial or Hardware Control Interface
- Programmable Audio Data Interface Modes
  - $I^2S$, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Four Independent stereo DAC outputs with independent digital volume controls
- Master or Slave Audio Data Interface
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation
- 28 lead SSOP Package

## APPLICATIONS

- DVD Players
- Surround Sound AV Processors and Hi-Fi systems
- Automotive Audio

## BLOCK DIAGRAM







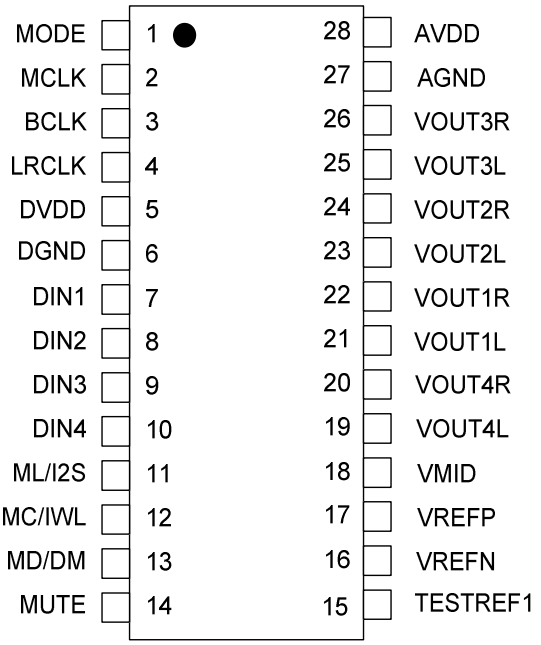
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## PIN CONFIGURATION 28 LEAD SSOP




## ORDERING INFORMATION

| DEVICE | TEMPERATURE RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---|---|---|---|---|
| WM8768GEDS/V | -25 to +85°C | 28-lead SSOP (Pb-free) | MSL3 | 260°C |
| WM8768GEDS/RV | -25 to +85°C | 28-lead SSOP (lPb-free, tape and reel) | MSL3 | 260°C |

**Note:**

Reel quantity = 2,000

## PIN DESCRIPTION – 28 LEAD SSOP

| PIN | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | MODE | Digital input | Control format selection<br>0 = Software control<br>1 = Hardware control |
| 2 | MCLK | Digital input | Master clock; 128, 192, 256, 384, 512, 768fs or 1152fs (fs = word clock frequency) |
| 3 | BCLK | Digital input/output | Audio interface bit clock |
| 4 | LRCLK | Digital input/output | Audio left/right word clock |
| 5 | DVDD | Supply | Digital positive supply |
| 6 | DGND | Supply | Digital negative supply |
| 7 | DIN1 | Digital input | DAC channel 1 data input |
| 8 | DIN2 | Digital input | DAC channel 2 data input |
| 9 | DIN3 | Digital input | DAC channel 3 data input |
| 10 | DIN4 | Digital input | DAC channel 4 data input |
| 11 | ML/I2S | Digital input | Software Mode: Serial interface Latch signal<br>Hardware Mode: Input Audio Data Format |
| 12 | MC/IWL | Digital input | Software Mode: Serial control interface clock<br>Hardware Mode: Audio data input word length |
| 13 | MD/DM | Digital input | Software Mode: Serial interface data<br>Hardware Mode: De-emphasis selection |
| 14 | MUTE | Digital input/output | DAC Zero Flag output or DAC mute input |
| 15 | TESTREF1 | Analogue output | Test Pin |
| 16 | VREFN | Analogue input | DAC negative reference supply |
| 17 | VREFP | Analogue input | DAC positive reference supply |
| 18 | VMID | Analogue output | Midrail divider decoupling pin; 10uF external decoupling |
| 19 | VOUT4L | Analogue output | DAC channel 4 left output |
| 20 | VOUT4R | Analogue output | DAC channel 4 right output |
| 21 | VOUT1L | Analogue output | DAC channel 1 left output |
| 22 | VOUT1R | Analogue output | DAC channel 1 right output |
| 23 | VOUT2L | Analogue output | DAC channel 2 left output |
| 24 | VOUT2R | Analogue output | DAC channel 2 right output |
| 25 | VOUT3L | Analogue output | DAC channel 3 left output |
| 26 | VOUT3R | Analogue output | DAC channel 3 right output |
| 27 | AGND | Supply | Analogue negative supply and substrate connection |
| 28 | AVDD | Supply | Analogue positive supply |

**Note** : Digital input pins have Schmitt trigger input buffers.

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|---|---|
| Digital supply voltage | -0.3V | +5V |
| Analogue supply voltage | -0.3V | +7V |
| Voltage range digital inputs | DGND -0.3V | DVDD +0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Master Clock Frequency | | 37MHz |
| Operating temperature range, $T_A$ | -25°C | +85°C |
| Storage temperature after soldering | -65°C | +150°C |

**Notes:**

1. Analogue and digital grounds must always be within 0.3V of each other for normal operation of the device.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Digital supply range | DVDD | | 2.7 | | 3.6 | V |
| Analogue reference supply | VREFP | | 2.7 | | 5.5 | V |
| Analogue supply range | AVDD | | 2.7 | | 5.5 | V |
| Ground | AGND, VREFN, DGND | | | 0 | | V |
| Difference DGND to AGND | | | -0.3 | 0 | +0.3 | V |

**Note:** Digital supply DVDD must never be more than 0.3V greater than AVDD for normal operation of the device.

## ELECTRICAL CHARACTERISTICS

**Test Conditions**

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, DGND = 0V, $T_A$ = +25°C, fs = 48kHz, MCLK = 256fs, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Digital Logic Levels (CMOS Levels)** | | | | | | |
| Input LOW level | $V_{IL}$ | | | | 0.3 x DVDD | V |
| Input HIGH level | $V_{IH}$ | | 0.7 x DVDD | | | V |
| Output LOW | $V_{OL}$ | $I_{OL}$=1mA | | | 0.1 x DVDD | V |
| Output HIGH | $V_{OH}$ | $I_{OH}$= -1mA | 0.9 x DVDD | | | V |
| **Analogue Reference Levels** | | | | | | |
| Reference voltage | $V_{VMID}$ | | | VREFP/2 | | V |
| Potential divider resistance | $R_{VMID}$ | VREFP to VMID and VMID to VREFN | | 100 | | kΩ |
| **DAC Performance (Load = 10kΩ, 50pF)** | | | | | | |
| 0dBFs Full scale output voltage | | | | 1.0 x VREFP/5 | | Vrms |
| SNR (Note 1,2,4) | | A-weighted, @ fs = 48kHz | 95 | 103 | | dB |
| SNR (Note 1,2,4) | | A-weighted @ fs = 96kHz | | 101 | | dB |
| SNR (Note 1,2,4) | | A-weighted @ fs = 192kHz | | 101 | | dB |
| SNR (Note 1,2,4) | | A-weighted @ fs = 48kHz, AVDD = 3.3V | | 101 | | dB |
| SNR (Note 1,2,4) | | A-weighted @ fs = 96kHz, AVDD = 3.3V | | 96 | | dB |
| Dynamic Range (Note 2,4) | DNR | A-weighted, -60dB full scale input | 95 | 103 | | dB |
| Total Harmonic Distortion (THD) (Note 4) | | 1kHz, 0dBFs | | -90 | -83 | dB |
| Mute Attenuation | | 1kHz Input, 0dB gain | | 100 | | dB |
| DAC channel separation | | | | 100 | | dB |
| Power Supply Rejection Ratio | PSRR | 1kHz 100mVpp | | 50 | | dB |
| | | 20Hz to 20kHz 100mVp-p | | 45 | | dB |
| **Supply Current** | | | | | | |
| Analogue supply current | | AVDD = 5V | | 18.4 | | mA |
| Digital Supply Current | | DVDD = 3.3V | | 14.6 | | mA |

**Notes:**

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
4. The performance of each DAC is measured separately

## TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio of the rms values of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as crosstalk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

## MASTER CLOCK TIMING

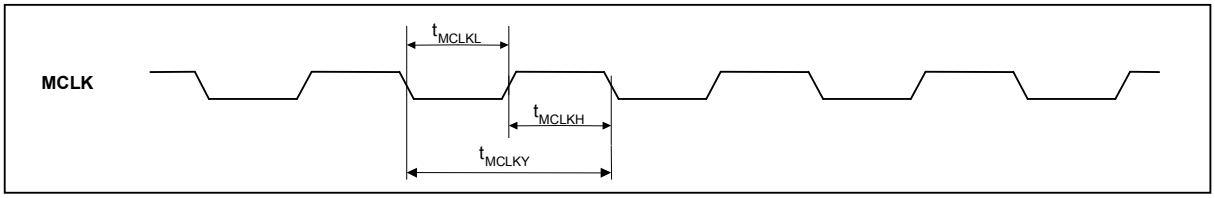



**Figure 1 DAC Master Clock Timing Requirements**

**Test Conditions**

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, DGND = 0V, $T_A$ = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **System Clock Timing Information** | | | | | | |
| MCLK System clock pulse width high | $t_{MCLKH}$ | | 11 | | | ns |
| MCLK System clock pulse width low | $t_{MCLKL}$ | | 11 | | | ns |
| MCLK System clock cycle time | $t_{MCLKY}$ | | 28 | | 1000 | ns |
| MCLK Duty cycle | | | 40:60 | | 60:40 | |
| Power-saving mode activated | | After MCLK stopped | 2 | | 10 | Us |
| Normal mode resumed | | After MCLK re-started | 0.5 | | 1 | MCLK cycle |

**Table 1 Master Clock Timing Requirements**

**Note:**

If MCLK period is longer than maximum specified above, power-saving mode is entered and DACs are powered down with internal digital audio filters being reset. In this power-saving mode, all registers will retain their values and can be accessed in the normal manner through the control interface. Once MCLK is restored, the DACs are automatically powered up, but a write to the volume update register bit is required to restore the correct volume settings.

## DIGITAL AUDIO INTERFACE – MASTER MODE

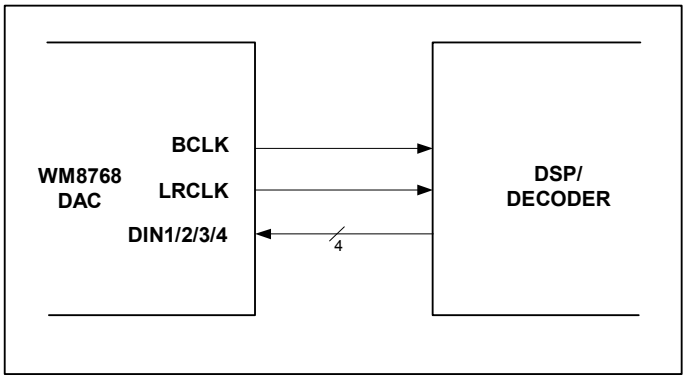



**Figure 2 Audio Interface - Master Mode**

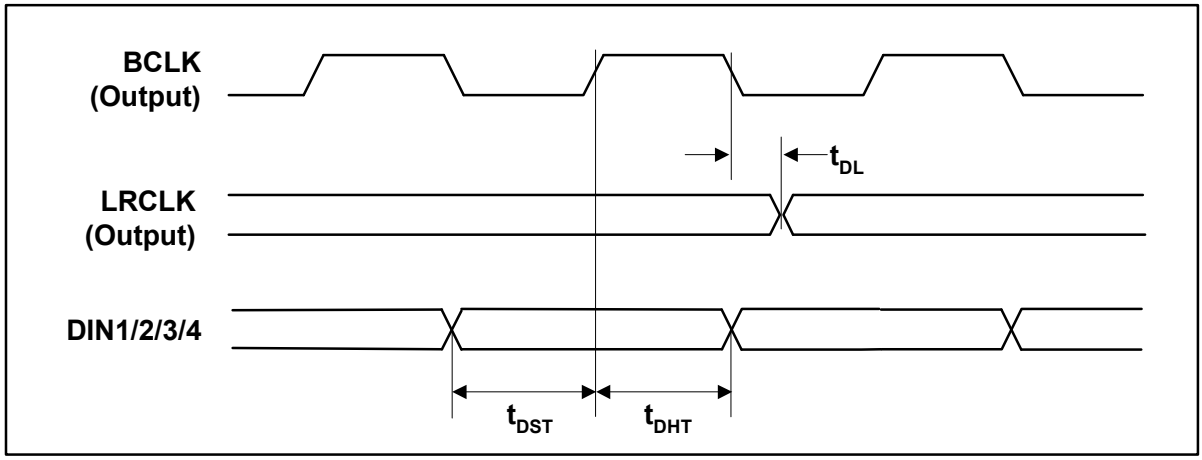



**Figure 3 Digital Audio Data Timing – Master Mode**

**Test Conditions**

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN, DGND = 0V, $T_A$ = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Audio Data Input Timing Information** | | | | | | |
| LRCLK propagation delay from BCLK falling edge | $t_{DL}$ | | 0 | | 10 | ns |
| DIN1/2/3/4 setup time to BCLK rising edge | $t_{DST}$ | | 10 | | | ns |
| DIN1/2/3/4 hold time from BCLK rising edge | $t_{DHT}$ | | 10 | | | ns |

**Table 2 Digital Audio Data Timing – Master Mode**

## DIGITAL AUDIO INTERFACE – SLAVE MODE

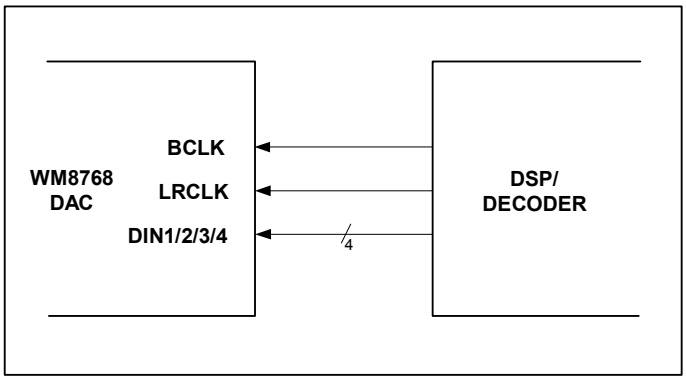



**Figure 4 Audio Interface – Slave Mode**

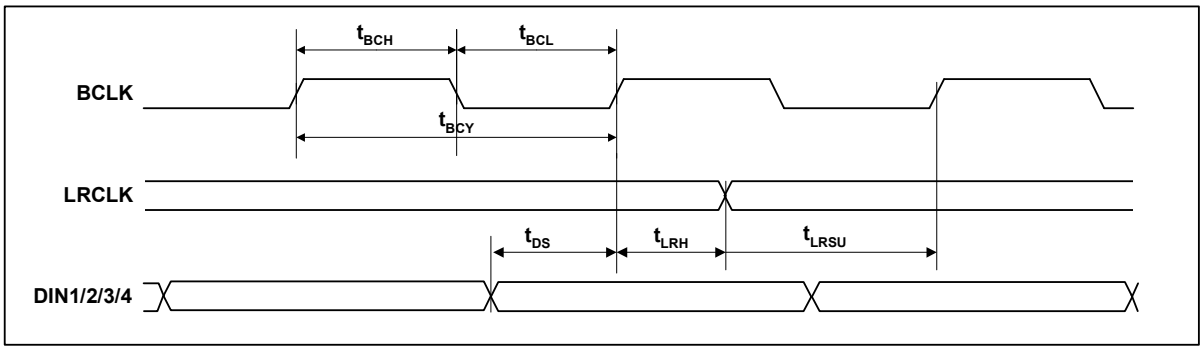



**Figure 5 Digital Audio Data Timing – Slave Mode**

**Test Conditions**

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, $T_A$ = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Audio Data Input Timing Information** | | | | | | |
| BCLK cycle time | $t_{BCY}$ | | 50 | | | ns |
| BCLK pulse width high | $t_{BCH}$ | | 20 | | | ns |
| BCLK pulse width low | $t_{BCL}$ | | 20 | | | ns |
| LRCLK set-up time to BCLK rising edge | $t_{LRSU}$ | | 10 | | | ns |
| LRCLK hold time from BCLK rising edge | $t_{LRH}$ | | 10 | | | ns |
| DIN1/2/3/4 set-up time to BCLK rising edge | $t_{DS}$ | | 10 | | | ns |
| DIN1/2/3/4 hold time from BCLK rising edge | $t_{DH}$ | | 10 | | | ns |

**Table 3 Digital Audio Data Timing – Slave Mode**

## MPU INTERFACE TIMING

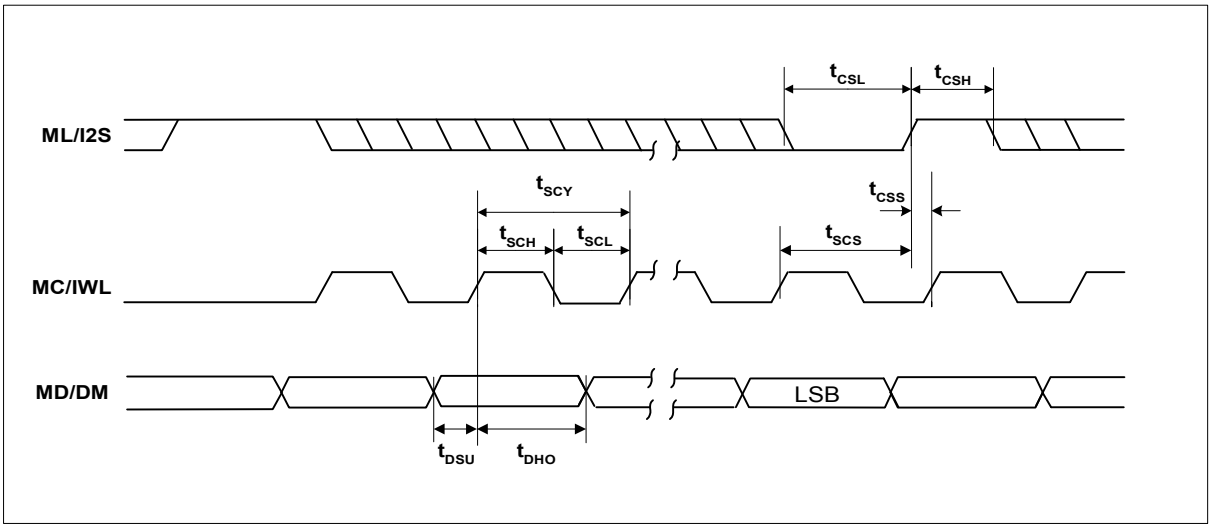



**Figure 6 SPI Compatible Control Interface Input Timing**

| **Test Conditions**<br>AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, $T_A$ = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNIT** |
| MC/IWL rising edge to ML/I2S rising edge | $t_{SCS}$ | 60 | | | ns |
| MC/IWL pulse cycle time | $t_{SCY}$ | 80 | | | ns |
| MC/IWL pulse width low | $t_{SCL}$ | 30 | | | ns |
| MC/IWL pulse width high | $t_{SCH}$ | 30 | | | ns |
| MD/DM to MC/IWL set-up time | $t_{DSU}$ | 20 | | | ns |
| MC/IWL to MD/DM hold time | $t_{DHO}$ | 20 | | | ns |
| ML/I2S pulse width low | $t_{CSL}$ | 20 | | | ns |
| ML/I2S pulse width high | $t_{CSH}$ | 20 | | | ns |
| ML/I2S rising to MC/IWL rising | $t_{CSS}$ | 20 | | | ns |

**Table 4 3-wire SPI Compatible Control Interface Input Timing Information**

## INTERNAL POWER ON RESET CIRCUIT

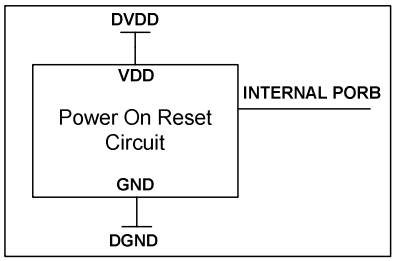



**Figure 7 Internal Power on Reset Circuit Schematic**

The WM8768 includes an internal Power-On-Reset Circuit, as shown in Figure 7, which is used reset the digital logic into a default state after power up. The POR circuit is powered from DVDD and monitors DVDD. It asserts PORB low if DVDD is below a minimum threshold.

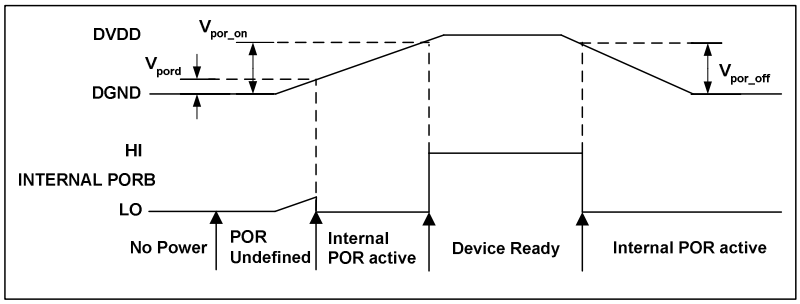



**Figure 8 Typical Power-Up Sequence**

Figure 8 shows a typical power-up sequence. When DVDD goes above the minimum threshold, Vpord, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DVDD rises to Vpor_on, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, PORB is asserted low whenever DVDD drops below the minimum threshold Vpor_off.

| SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $V_{pord}$ | 0.3 | 0.5 | 0.8 | V |
| $V_{por_on}$ | 1.3 | 1.7 | 2.0 | V |
| $V_{por_off}$ | 1.3 | 1.7 | 2.0 | V |

**Table 5 Typical POR Operation (typical values, not tested)**

# DEVICE DESCRIPTION

## INTRODUCTION

WM8768 is a complete 8-channel DAC including digital interpolation and decimation filters and switched capacitor multi-bit sigma delta DACs with digital volume controls on each channel and output smoothing filters.

The device is implemented as four separate stereo DACs in a single package and controlled by a single interface.

Each stereo DAC has its own data input DIN1/2/3/4. DAC word clock LRCLK, DAC bit clock BCLK and DAC master clock MCLK are shared between them.

The Audio Interface may be configured to operate in either master or slave mode. In Slave mode, LRCLK and BCLK are all inputs. In Master mode, LRCLK and BCLK are all outputs.

Each DAC has its own digital volume control that is adjustable in 0.5dB steps. The digital volume controls may be operated independently. In addition, a zero cross detect circuit is provided for each DAC for the digital volume controls. The digital volume control detects a transition through the zero point before updating the volume. This minimises audible clicks and 'zipper' noise as the gain values change.

Control of internal functionality of the device is by 3-wire serial or pin programmable control interface. The software control interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally.

Operation using master clocks of 128fs, 192fs, 256fs, 384fs, 512fs, 768fs or 1152fs is provided for the DAC In Slave mode selection between clock rates is automatically controlled. Audio sample rates (fs) from less than 8ks/s up to 192ks/s are allowed for the DAC, provided the appropriate master clock is input.

In PCM mode, the audio data interface supports right justified, left justified and $I^2S$ (Philips left justified, one bit delayed) interface formats along with a highly flexible DSP serial port interface.

## PCM AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the DAC MCLK input pin(s) with no software configuration necessary

The DAC master clock for WM8768 supports audio sampling rates from 128fs to 1152fs, where fs is the audio sampling frequency (LRCLK) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

In Slave mode the WM8768 has a master clock detection circuit that automatically determines the relationship between the system clock frequency and the sampling rate (to within +/- 32 master clocks). If there is a greater than 32 clocks error the interface defaults to 1152fs mode. The WM8768 is tolerant of phase variations or jitter on the master clock. Table 6 shows the typical master clock frequency inputs for the WM8768.

The signal processing for the WM8768 typically operates at an oversampling rate of 128fs. The exception to this is for operation with a 128/192fs system clock, e.g. for 192kHz operation, when the oversampling rate is 64fs.

| SAMPLING RATE (LRCLK) | SYSTEM CLOCK FREQUENCY (MHZ) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs | 1152fs |
| 32kHz | 4.096 | 6.144 | 8.192 | 12.288 | 16.384 | 24.576 | 36.864 |
| 44.1kHz | 5.6448 | 8.467 | 11.2896 | 16.9340 | 22.5792 | 33.8688 | Unavailable |
| 48kHz | 6.144 | 9.216 | 12.288 | 18.432 | 24.576 | 36.864 | Unavailable |
| 96kHz | 12.288 | 18.432 | 24.576 | 36.864 | Unavailable | Unavailable | Unavailable |
| 192kHz | 24.576 | 36.864 | Unavailable | Unavailable | Unavailable | Unavailable | Unavailable |

**Table 6 System Clock Frequencies Versus Sampling Rate**

## HARDWARE CONTROL MODES

When the MODE pin is held high, the following hardware modes of operation are available.

### MUTE AND AUTOMUTE OPERATION

In both hardware and software modes, the MUTE pin controls the selection of MUTE directly, and can be used to enable and disable the automute function. This pin becomes an output when left floating and indicates infinite zero detect (IZD) has been detected.

| | DESCRIPTION |
|---|---|
| 0 | Normal Operation |
| 1 | Mute DAC channels |
| Floating | Enable IZD, MUTE pin becomes an output to indicate when IZD occurs.<br>L=IZD not detected, H=IZD detected. |

**Table 7 Mute and Automute Control**

Figure 9 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards $V_{MID}$ with a time constant of approximately 64 input samples. When MUTE is de-asserted, the output will restart almost immediately from the current input sample.

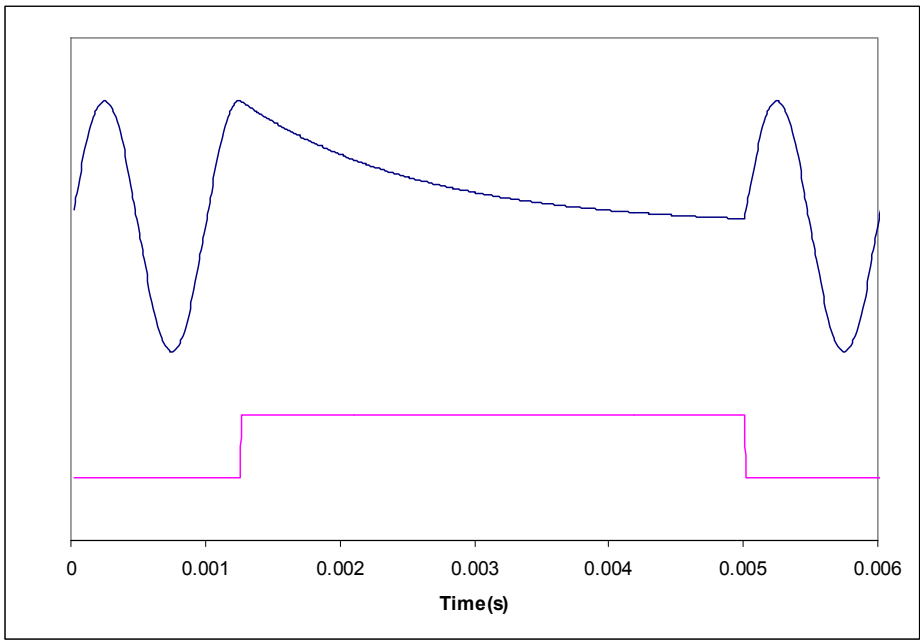



**Figure 9 Application and Release of Soft Mute**

In hardware mode (MODE pin set high) the MUTE pin becomes a bi-directional pin. Therefore if it is driven low the device will never softmute. If it is driven high then all channels will softmute immediately.

However if the pin is connected to a high impedance, or left floating, then when all four internal zero flags are raised. the WM8768 will also drive a weak logic high signal on the MUTE pin (output impedance 10kOhms) which can be used to drive an external device.

It is not possible to perform analogue mute in Hardware mode.

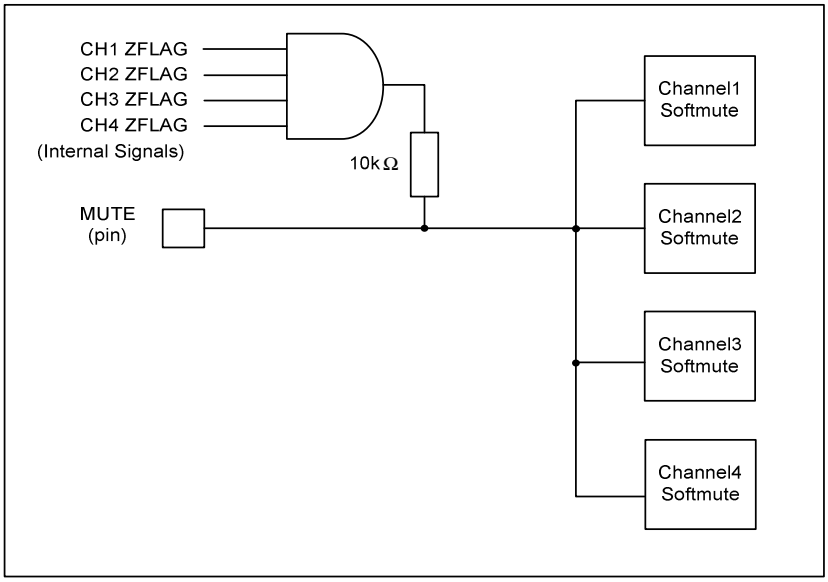



**Figure 10 MUTE Logic in Hardware Mode**

## INPUT FORMAT SELECTION

In hardware mode, ML/I2S and MC/IWL become input controls for selection of input data format type and input data word length for the DAC.

| ML/I2S | MC/IWL | INPUT DATA MODE |
|---|---|---|
| 0 | 0 | 24-bit right justified |
| 0 | 1 | 20-bit right justified |
| 1 | 0 | 16-bit $I^2S$ |
| 1 | 1 | 24-bit $I^2S$ |

**Table 8 Input Format Selection**

**Note:**

In 24 bit $I^2S$ mode, any width of 24 bits or less is supported provided that the left/right clocks (LRCLK) are high for a minimum of 24 bit clocks (BCLK) and low for a minimum of 24 bit clocks. If exactly 32 bit clocks occur in one left/right clock (16 high, 16 low) the chip will auto detect and run a 16 bit data mode.

## DE-EMPHASIS CONTROL

In hardware mode, the MD/DM pin becomes an input control for selection of de-emphasis filtering to be applied.

| MD/DM | DE-EMPHASIS |
|---|---|
| 0 | Off |
| 1 | On |

**Table 9 De-emphasis Control**

## DIGITAL AUDIO INTERFACE

### MASTER AND SLAVE MODES

The audio interface operates in either Slave or Master mode, selectable using the MS control bit. In both Master and Slave modes DIN1/2/3/4 are always inputs to the WM8768. The default is Slave mode.

In Slave mode, LRCLK and BCLK are inputs to the WM8768 (Figure 11). DIN1/2/3/4 and LRCLK are sampled by the WM8768 on the rising edge of BCLK.

By setting the control bit BCP the polarity of BCLK may be reversed so that DIN1/2/3/4 and LRCLK are sampled on the falling edge of BCLK .

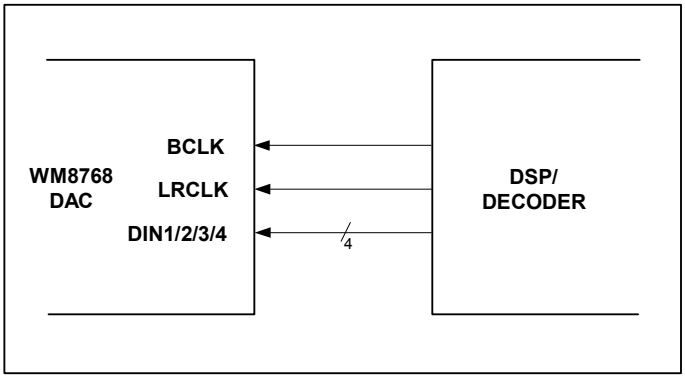



**Figure 11 Slave Mode**

In Master mode, LRCLK and BCLK are outputs from the WM8768 (Figure 12). LRCLK and BCLK are generated by the WM8768. DIN1/2/3/4 are sampled by the WM8768 on the rising edge of BCLK so the controller must output DAC data that changes on the falling edge of BCLK.

By setting control bit BCP the polarity of BCLK may be reversed so that DIN1/2/3/4 are sampled on the falling edge of BCLK..

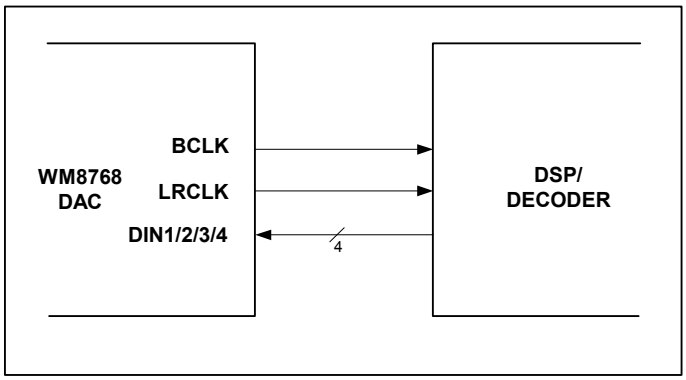



**Figure 12 Master Mode**

## AUDIO INTERFACE FORMATS

Audio data is applied to the internal DAC filters via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- $I^2S$ mode
- DSP mode A
- DSP mode B

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

In left justified, right justified and $I^2S$ modes, the digital audio interface receives DAC data on the DIN1/2/3/4 inputs. Audio data for each stereo channel is time multiplexed with LRCLK indicating whether the left or right channel is present. LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and $I^2S$ modes, the minimum number of BCLKs per LRCLK period is 2 times the selected word length. LRCLK must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on LRCLK is acceptable provided the above requirements are met.

In DSP modes A or B, all 8 DAC channels are time multiplexed onto DIN1. LRCLK is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCLKs per LRCLK period is 8 times the selected word length. Any mark to space ratio is acceptable on LRCLK provided the rising edge is correctly positioned.

## LEFT JUSTIFIED MODE

In left justified mode, the MSB of DIN1/2/3/4 is sampled by the WM8768 on the first rising edge of BCLK following a LRCLK transition. LRCLK is high during the left samples and low during the right samples (Figure 13).

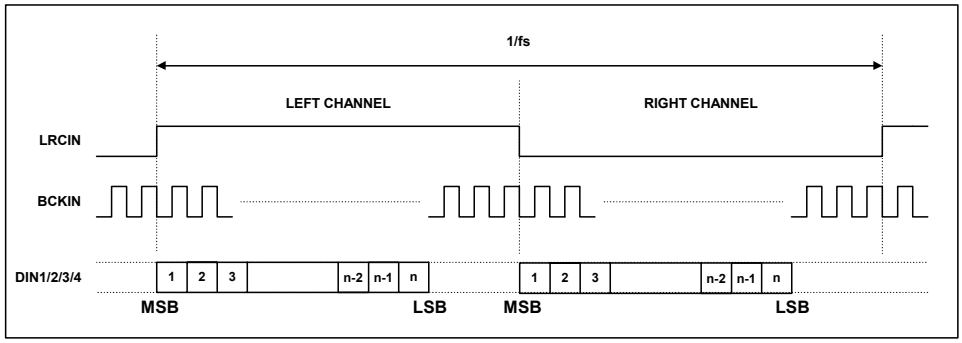



**Figure 13 Left Justified Mode Timing Diagram**

### RIGHT JUSTIFIED MODE

In right justified mode, the LSB of DIN1/2/3/4 is sampled by the WM8768 on the rising edge of BCLK preceding a LRCLK transition. LRCLK are high during the left samples and low during the right samples (Figure 14).

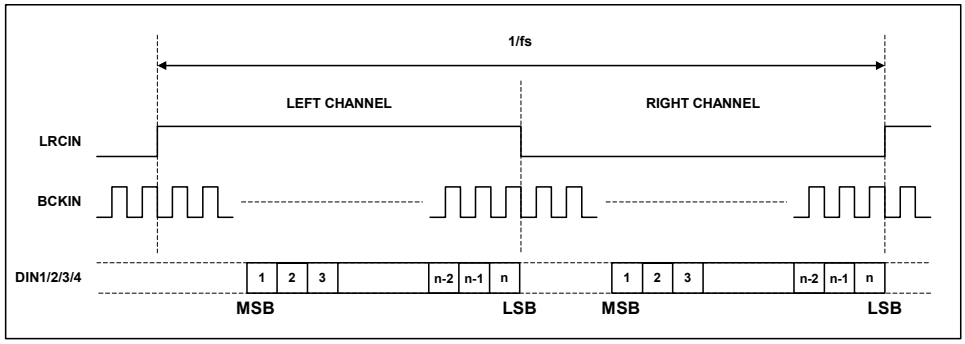



**Figure 14 Right Justified Mode Timing Diagram**

### I2S MODE

In $I^2S$ mode, the MSB of DIN1/2/3/4 is sampled by the WM8768 on the second rising edge of BCLK following a LRCLK transition. LRCLK are low during the left samples and high during the right samples.

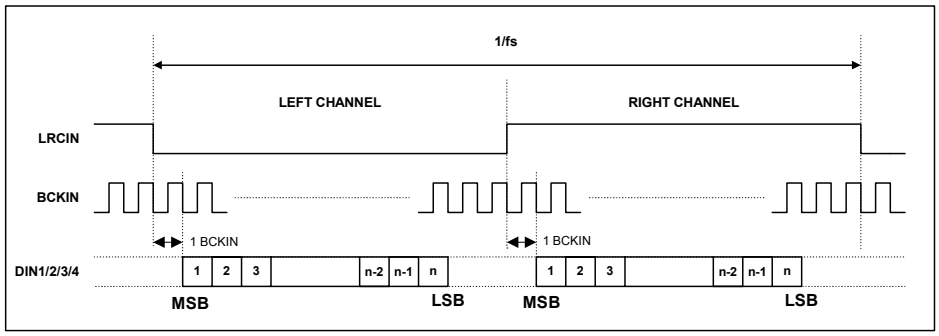



**Figure 15 $I^2S$ Mode Timing Diagram**

### DSP MODE A

In DSP mode A, the MSB of DAC channel 1 left data is sampled by the WM8768 on the second rising edge on BCLK following a LRCLK rising edge. DAC channel 1 right and DAC channels 2/3/4 data follow DAC channel 1 left data (Figure 16).

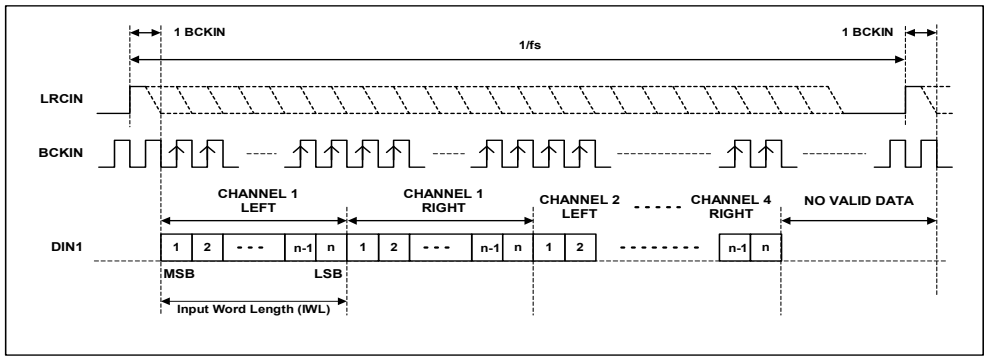



**Figure 16 DSP Mode A Timing Diagram – DAC data input**

### DSP MODE B

In DSP mode B, the MSB of DAC channel 1 left data is sampled by the WM8768 on the first BCLK rising edge following a LRCLK rising edge. DAC channel 1 right and DAC channels 2/3/4 data follow DAC channel 1 left data (Figure 17).

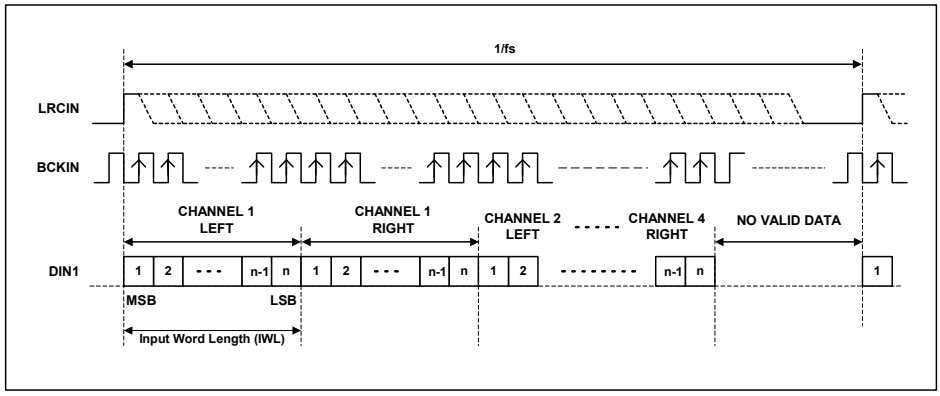



**Figure 17 DSP Mode B Timing Diagram – DAC data input**

In both DSP modes A and B, DACL1 is always sent first, followed immediately by DACR1 and the data words for the other 8 channels. No BCLK edges are allowed between the data words. The word order is DAC1 left, DAC1 right, DAC2 left, DAC2 right, DAC3 left, DAC3 right, DAC4 left, DAC4 right .

## POWERDOWN MODES

The WM8768 has powerdown control bits allowing specific parts of the WM8768 to be powered off when not being used. The four stereo DACs each have a separate powerdown control bit, DACD[2:0] & DACD4, allowing individual stereo DACs to be powered off when not in use. Setting DACD will power down everything except the reference VMID. This may be powered down by setting PDWN. Setting PDWN will override all other powerdown control bits. It is recommended that the DACs are powered down before setting PDWN.

## SOFTWARE CONTROL INTERFACE OPERATION

The WM8768 is controlled using a 3-wire serial interface in software mode or pin programmable in hardware mode.

The control mode is selected by the state of the MODE pin.

### 3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

MD/DM is used for the program data, MC/IWL is used to clock in the program data and ML/I2S is used to latch the program data. MD/DM is sampled on the rising edge of MC/IWL. The 3-wire interface protocol is shown in Figure 18.

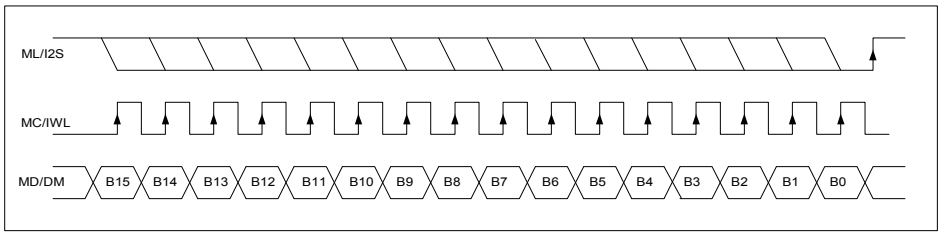



**Figure 18 3-wire SPI Compatible Interface**

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. ML/I2S is edge sensitive – the data is latched on the rising edge of ML/I2S.

## CONTROL INTERFACE REGISTERS

### ATTENUATOR CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both left and right channel DACs from the next audio input sample. No update to the attenuation registers is required for ATC to take effect.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000010<br>DAC Channel Control | 3 | ATC | 0 | Attenuator Control Mode:<br>0 : Right channels use Right attenuations<br>1: Right Channels use Left Attenuations |

### DAC OUTPUT CONTROL

The DAC output control word determines how the left and right inputs to the audio Interface are applied to the left and right DACs:

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | |
|---|---|---|---|---|---|---|
| 0000010 DAC Control | 8:5 | PL[3:0] | 1001 | PL[3:0] | Left Output | Right Output |
| | | | | 0000 | Mute | Mute |
| | | | | 0001 | Left | Mute |
| | | | | 0010 | Right | Mute |
| | | | | 0011 | (L+R)/2 | Mute |
| | | | | 0100 | Mute | Left |
| | | | | 0101 | Left | Left |
| | | | | 0110 | Right | Left |
| | | | | 0111 | (L+R)/2 | Left |
| | | | | 1000 | Mute | Right |
| | | | | 1001 | Left | Right |
| | | | | 1010 | Right | Right |
| | | | | 1011 | (L+R)/2 | Right |
| | | | | 1100 | Mute | (L+R)/2 |
| | | | | 1101 | Left | (L+R)/2 |
| | | | | 1110 | Right | (L+R)/2 |
| | | | | 1111 | (L+R)/2 | (L+R)/2 |

### DAC DIGITAL AUDIO INTERFACE CONTROL REGISTER

Interface format is selected via the FMT[1:0] register bits:

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000011 Interface Control | 1:0 | FMT [1:0] | 00 | Interface format Select<br>00 : right justified mode<br>01: left justified mode<br>10: $I^2S$ mode<br>11: DSP Modes A or B |

In left justified, right justified or $I^2S$ modes, the LRP register bit controls the polarity of LRCLK. If this bit is set high, the expected polarity of LRCLK will be the opposite of that shown Figure 13, Figure 14 and Figure 15. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced. In DSP modes, the LRP register bit is used to select between modes A and B.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000011 Interface Control | 2 | LRP | 0 | In left/right/$I^2S$ modes:<br>LRCLK Polarity (normal)<br>0 : normal LRCLK polarity<br>1: inverted LRCLK polarity |
| | | | | In DSP mode:<br>0 : DSP mode A<br>1: DSP mode B |

By default, LRCLK and DIN1/2/3/4 are sampled on the rising edge of BCLK and should ideally change on the falling edge. Data sources that change LRCLK and DIN1/2/3/4 on the rising edge of BCLK can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCLK to the inverse of that shown in Figure 13, Figure 14, Figure 15, Figure 16, Figure 17 and Figure 18.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000011<br>Interface Control | 3 | BCP | 0 | BCLK Polarity<br>0 : normal BCLK polarity<br>1: inverted BCLK polarity |

The IWL[1:0] bits are used to control the input word length.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000011<br>Interface Control | 5:4 | IWL<br>[1:0] | 00 | Input Word Length<br>00 : 16 bit data<br>01: 20 bit data<br>10: 24 bit data<br>11: 32 bit data |

**Note:** If 32-bit mode is selected in right justified mode, the WM8768 defaults to 24 bits.

In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8768 pads the unused LSBs with zeros. If the DAC is programmed into 32 bit mode, the 8 LSBs are ignored.

**Note:** In 24 bit $I^2S$ mode, any width of 24 bits or less is supported provided that LRCLK is high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs. If exactly 32 bit clocks occur in one left/right clock (16 high, 16 low) the chip will auto detect and run a 16 bit data mode.

A number of options are available to control how data from the Digital Audio Interface is applied to the DAC channels.

### DAC OUTPUT PHASE

The DAC phase control word determines whether the output of each DAC is non-inverted or inverted

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | | |
|---|---|---|---|---|---|---|
| 0000011<br>DAC Phase | 8:6 | PHASE<br>[2:0] | 000 | Bit | DAC | Phase |
| | | | | 0 | DAC1L/R | 1 = invert |
| | | | | 1 | DAC2L/R | 1 = invert |
| | | | | 2 | DAC3L/R | 1 = invert |
| 0001111<br>DAC4 Control | 3 | PHASE4 | 0 | N/A | DAC4L/R | 1 = invert |

### DIGITAL ZERO CROSS-DETECT

The digital volume control also incorporates a zero cross detect circuit which detects a transition through the zero point before updating the digital volume control with the new volume. This is enabled by control bit DZCEN.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0001001<br>DAC Control | 0 | DZCEN | 0 | DAC Digital Volume Zero Cross Enable:<br>0: Zero cross detect enabled<br>1: Zero cross detect disabled |

### SOFTMUTE

The digital muting function used in Software and Hardware mode applies a softmute with the operating characteristics shown in Figure 19.

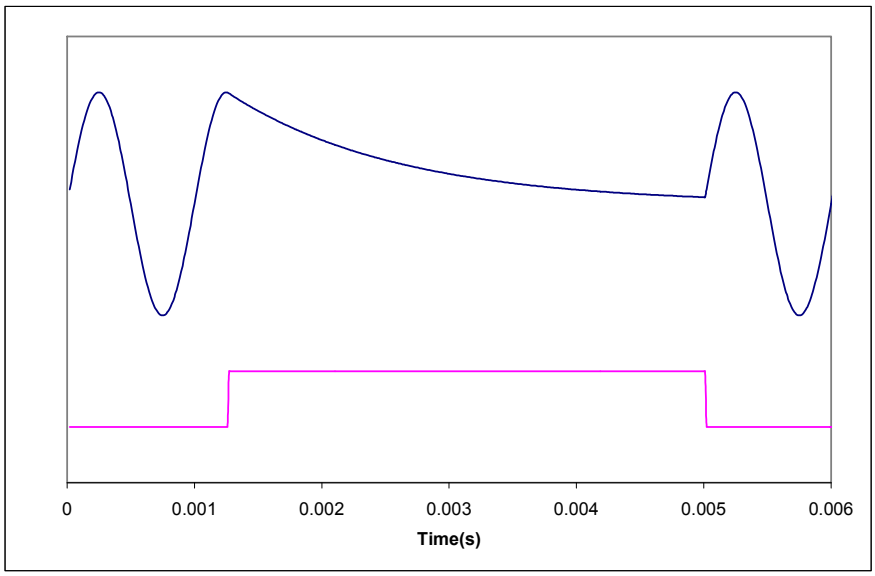



**Figure 19 Soft Mute Operation**

When the softmute is applied the output of the device will decay towards $V_{MID}$ with a time constant of approximately 64 input samples. When the mute is released, either manually or automatically by the chip, the output will restart immediately from the current input sample.

### ANALOGUE MUTE

Analogue mute can only be used in software mode and will cause the output of the selected DAC to perform an analogue mute that clamps the output of the DAC to VMID. This function is dependent in the IZD bit which is described in section INFINITE ZERO DETECT, later.

## SOFTWARE MUTE MODES

The WM8768 can be muted in a number of different ways when in software mode (MODE pin pulled low). Refer to Figure 20 which shows a representation of the interaction between functions described below.

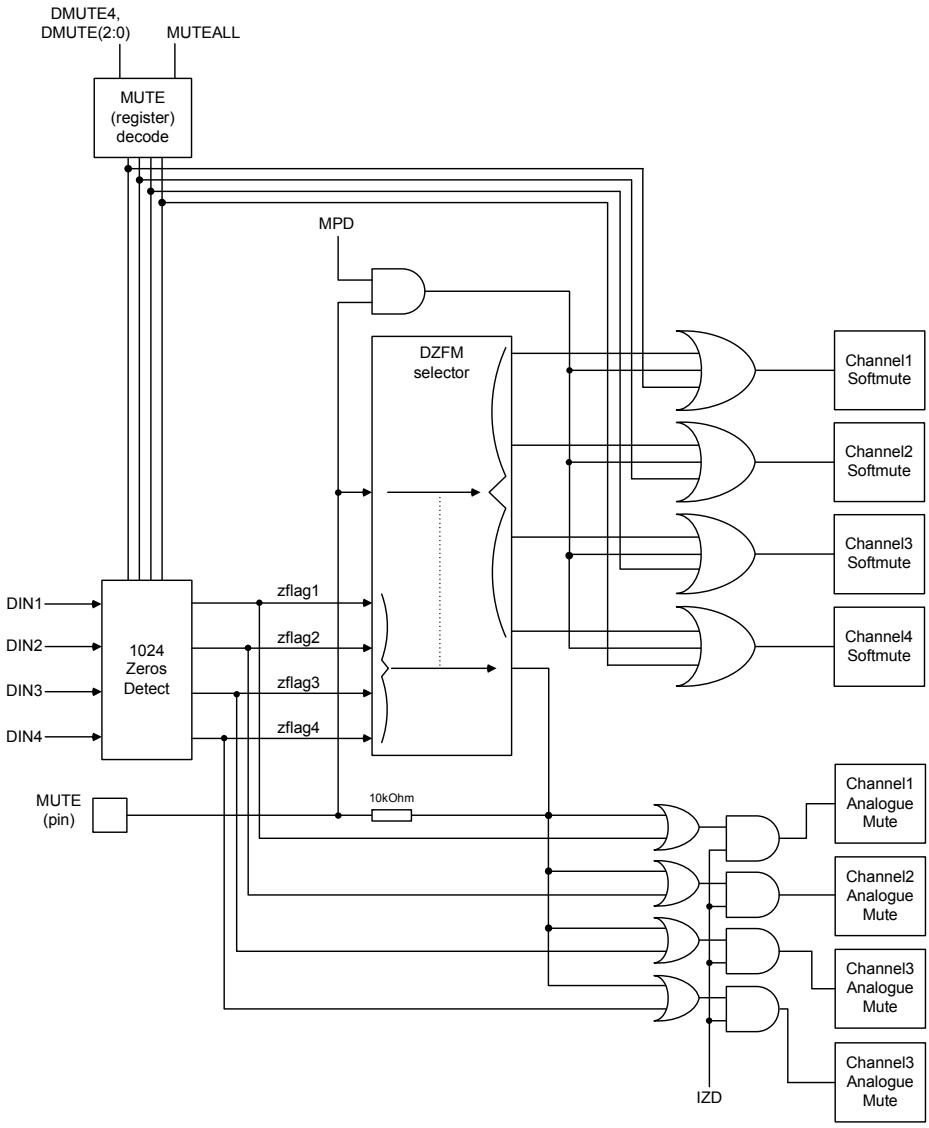



**Figure 20 Internal Mute Logic**

### DMUTE AND MUTEALL

The WM8768 can be directly muted using the DMUTE and DMUTE4 register bits to control which channels are muted. The mute happens as soon as the serial write is performed.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0001001<br>DAC Mute | 5:3 | DMUTE [2:0] | 000 | DAC 3,2 and 1 Soft Mute select |
| 0001111<br>DAC4 Control | 2 | DMUTE4 | 0 | DAC 4 Soft Mute select |

| {DMUTE4,DMUTE [2:0]} | DAC CHANNEL 4 | DAC CHANNEL 3 | DAC CHANNEL 2 | DAC CHANNEL 1 |
|---|---|---|---|---|
| 0000 | Not MUTE | Not MUTE | Not MUTE | Not MUTE |
| 0001 | Not MUTE | Not MUTE | Not MUTE | MUTE |
| 0010 | Not MUTE | Not MUTE | MUTE | Not MUTE |
| 0011 | Not MUTE | Not MUTE | MUTE | MUTE |
| 0100 | Not MUTE | MUTE | Not MUTE | Not MUTE |
| 0101 | Not MUTE | MUTE | Not MUTE | MUTE |
| 0110 | Not MUTE | MUTE | MUTE | Not MUTE |
| 0111 | Not MUTE | MUTE | MUTE | MUTE |
| 1000 | MUTE | Not MUTE | Not MUTE | Not MUTE |
| 1001 | MUTE | Not MUTE | Not MUTE | MUTE |
| 1010 | MUTE | Not MUTE | MUTE | Not MUTE |
| 1011 | MUTE | Not MUTE | MUTE | MUTE |
| 1100 | MUTE | MUTE | Not MUTE | Not MUTE |
| 1101 | MUTE | MUTE | Not MUTE | MUTE |
| 1110 | MUTE | MUTE | MUTE | Not MUTE |
| 1111 | MUTE | MUTE | MUTE | MUTE |

**Table 10 DAC Mute Control**

An overall MUTE to all channels can be applied by using the MUTEALL register.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000010<br>DAC Mute | 0 | MUTEALL | 0 | Soft Mute Select:<br>0 : Normal operation<br>1: Soft mute all channels |

### MUTE PIN AS INPUT

The WM8768 can be muted externally by driving the MUTE pin high. When the MUTE pin is driven low the device will never automute, although direct mutes can still be applied via the DMUTE or MUTEALL registers.

The DZFM bits are used to decode the operation of a MUTE pin (decides which channels will be affected by the logic level present on the MUTE pin). MPD (Mute Pin Decode) is used to enable the DZFM operation. If MPD is set, the selection made by the DZFM bits will be ignored and all channels will be muted when the pin is driven high.

Table 11 below describes which channels will be softmuted when the MUTE pin is driven high depending on the MPD and DZFM bits.

| MPD | {DZFM4,DZFM [1:0]} | CHANNELS MUTED WHEN MUTE PIN HIGH |
|---|---|---|
| 0 | 000 | All Channels |
| 0 | 001 | CH1 |
| 0 | 010 | CH2 |
| 0 | 011 | CH3 |
| 0 | 100 | CH4 |
| 0 | 101 | CH1 and CH2 |
| 0 | 110 | CH1, CH2 and CH3 |
| 0 | 111 | CH3 and CH4 |
| 1 | 000 | All Channels |
| 1 | 001 | All Channels |
| 1 | 010 | All Channels |
| 1 | 011 | All Channels |
| 1 | 100 | All Channels |
| 1 | 101 | All Channels |
| 1 | 110 | All Channels |
| 1 | 111 | All Channels |

**Table 11 Mute Pin Decode when Mute Pin as Input**

### AUTOMUTE

The WM8768 can automute by counting zero samples on the DIN1/2/3/4 inputs. When 1024 zero samples are counted on one channel, one of four internal zero flags (zflag1/2/3/4 shown in figure 2) is raised. Depending on the external hardware and settings of DZFM, MPD and IZD, different automute operations are possible.

### MUTE PIN AS OUTPUT

If the MUTE pin is connected to a high impedance (input to external mute circuitry for example) or left floating, zflag1/2/3/4 will be output on the Mute pin dependent on DZFM settings. This is described in Table 12 below. The output impedance of the MUTE pin is 10kOhms

| {DZFM4,DZFM [1:0]} | CONDITION UNDER WHICH MUTE PIN DRIVEN HIGH |
|---|---|
| 000 | Zflag1, 2, 3 and 4 all high |
| 001 | Zflag1 high |
| 010 | Zflag2 high |
| 011 | Zflag3 high |
| 100 | Zflag4 high |
| 101 | Zflag1 and 2 high |
| 110 | Zflag1, 2 and 3 high |
| 111 | Zflag3 and 4 high |

**Table 12 Effect of DZFM on Mute Pin Output**

When the Mute pin is used as an output, its logic level remains connected to the DZFM selector inside the chip (see figure 1). So, when the WM8768 drives the Mute pin high, the output DACs will also softmute as described by Table 13.

| MPD | {DZFM4,DZFM [1:0]} | CHANNELS MUTED WHEN MUTE PIN DRIVEN HIGH |
|---|---|---|
| 0 | 000 | All Channels |
| 0 | 001 | CH1 |
| 0 | 010 | CH2 |
| 0 | 011 | CH3 |
| 0 | 100 | CH4 |
| 0 | 101 | CH1 and CH2 |
| 0 | 110 | CH1, CH2 and CH3 |
| 0 | 111 | CH3 and CH4 |
| 1 | 000 | All Channels |
| 1 | 001 | All Channels |
| 1 | 010 | All Channels |
| 1 | 011 | All Channels |
| 1 | 100 | All Channels |
| 1 | 101 | All Channels |
| 1 | 110 | All Channels |
| 1 | 111 | All Channels |

**Table 13 Mute Pin Decode when Mute Pin as Output**

### INFINITE ZERO DETECT

When it is set, the IZD register causes an analogue mute of the DAC channel output amplifier both when there are 1024 zeros on that channel's DIN pin or when it is manually muted by DMUTE or MUTEALL.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000010<br>DAC Channel Control | 4 | IZD | 0 | IZD Enable<br>0 : Disable infinite zero mute<br>1: Enable infinite zero mute |

This operation is only available in software mode and can sometimes create a very small click at the output of the device.

### DE-EMPHASIS MODE

Each stereo DAC channel has an individual de-emphasis control bit:

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0001001<br>DAC De-emphahsis Control | [8:6] | DEEMPH [2:0] | 000 | DAC 3, 2 and 1 De-emphasis channel selection select: |
| 0001111<br>DAC4 Control | 4 | DEEMPH4 | 0 | DAC 4 De-emphasis channel selection select: |

| {DEEMPH4,DEEMPH [2:0]} | DAC CHANNEL 4 | DAC CHANNEL 3 | DAC CHANNEL 2 | DAC CHANNEL 1 |
|---|---|---|---|---|
| 0000 | Not-DEEMPH | Not-DEEMPH | Not-DEEMPH | Not-DEEMPH |
| 0001 | Not-DEEMPH | Not-DEEMPH | Not-DEEMPH | DEEMPH |
| 0010 | Not-DEEMPH | Not-DEEMPH | DEEMPH | Not-DEEMPH |
| 0011 | Not-DEEMPH | Not-DEEMPH | DEEMPH | DEEMPH |
| 0100 | Not-DEEMPH | DEEMPH | Not-DEEMPH | Not-DEEMPH |
| 0101 | Not-DEEMPH | DEEMPH | Not-DEEMPH | DEEMPH |
| 0110 | Not-DEEMPH | DEEMPH | DEEMPH | Not-DEEMPH |
| 0111 | Not-DEEMPH | DEEMPH | DEEMPH | DEEMPH |
| 1000 | DEEMPH | Not-DEEMPH | Not-DEEMPH | Not-DEEMPH |
| 1001 | DEEMPH | Not-DEEMPH | Not-DEEMPH | DEEMPH |
| 1010 | DEEMPH | Not-DEEMPH | DEEMPH | Not-DEEMPH |
| 1011 | DEEMPH | Not-DEEMPH | DEEMPH | DEEMPH |
| 1100 | DEEMPH | DEEMPH | Not-DEEMPH | Not-DEEMPH |
| 1101 | DEEMPH | DEEMPH | Not-DEEMPH | DEEMPH |
| 1110 | DEEMPH | DEEMPH | DEEMPH | DEEMPH |
| 1111 | DEEMPH | DEEMPH | DEEMPH | DEEMPH |

**Table 14 De-emphasis Control**

Refer to Figure 25, Figure 26, Figure 27, Figure 28, Figure 29 and Figure 30 for details of the De-Emphasis performance at different sample rates.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000010<br>DAC DEEMPH | 1 | DEEMP ALL | 0 | DEEMPH Select:<br>0 : Normal Operation<br>1: De-emphasis all channels |

## POWERDOWN MODE AND DAC DISABLE

Setting the PDWN register bit immediately powers down the DACs on the WM8768, overriding the DACD powerdown bits control bits. All trace of the previous input samples is removed, but all control register settings are preserved. When PDWN is cleared the digital filters will be reinitialised

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000010<br>Powerdown Control | 2 | PDWN | 0 | Power Down all DAC's Select:<br>0: All DACs enabled<br>1: All DACs disabled |

The DACs may also be powered down individually by setting the DACPD disable bits. Each Stereo DAC channel has a separate disable DACPD[2:0]. Setting DACPD for a channel will disable the DACs and select a low power mode.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0001010<br>Powerdown Control | 3:1 | DACD[2:0] | 000 | DAC Disable |
| 0001111<br>DAC4 Control | 1 | DACD4 | 0 | DAC 4 Powerdown |

| {DACD4,DACD [2:0]} | DAC CHANNEL 4 | DAC CHANNEL 3 | DAC CHANNEL 2 | DAC CHANNEL 1 |
|---|---|---|---|---|
| 0000 | Active | Active | Active | Active |
| 0001 | Active | Active | Active | DISABLE |
| 0010 | Active | Active | DISABLE | Active |
| 0011 | Active | Active | DISABLE | DISABLE |
| 0100 | Active | DISABLE | Active | Active |
| 0101 | Active | DISABLE | Active | DISABLE |
| 0110 | Active | DISABLE | DISABLE | Active |
| 0111 | Active | DISABLE | DISABLE | DISABLE |
| 1000 | DISABLE | Active | Active | Active |
| 1001 | DISABLE | Active | Active | DISABLE |
| 1010 | DISABLE | Active | DISABLE | Active |
| 1011 | DISABLE | Active | DISABLE | DISABLE |
| 1100 | DISABLE | DISABLE | Active | Active |
| 1101 | DISABLE | DISABLE | Active | DISABLE |
| 1110 | DISABLE | DISABLE | DISABLE | Active |
| 1111 | DISABLE | DISABLE | DISABLE | DISABLE |

**Table 15 DAC Disable Control**

## MASTER POWERDOWN

Control bit PWRDNALL overrides the {DACD4,DACD[2:0]} bits and powers everything down including the reference VMID. It is recommended that the DACs are powered down first before setting this bit.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0001010<br>Interface Control | 4 | PWRDNALL | 0 | Master Power down bit<br>0: Not powered down<br>1: Powered down |

### MASTER MODE SELECT

Control bit MS selects between audio interface Master and Slave Modes. In Master mode LRCLK and BCLK are outputs and are generated by the WM8768. In Slave mode LRCLK and BCLK are inputs to WM8768.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0001010<br>Interface Control | 5 | MS | 0 | Audio Interface Master/Slave Mode select:<br>0: Slave Mode<br>1: Master Mode |

### MASTER MODE LRCLK FREQUENCY SELECT

In Master mode the WM8768 generates LRC and BCLK. These clocks are derived from the master clock and the ratio of MCLK to LRCK is set by RATE.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0001010<br>Interface Control | 8:6 | RATE[2:0] | 010 | Master Mode MCLK: LRCLK ratio select:<br>000: 128fs<br>001: 192fs<br>010: 256fs<br>011: 384fs<br>100: 512fs<br>101: 768fs |

### MUTE PIN DECODE

The MUTE pin can either be used as an output or an input. When used as an input the MUTE pins action can be controlled by setting the DZFM and DZFM4 bit to select the corresponding DAC for applying the MUTE to. As an output its meaning is selected by the DZFM and DZFM4 control bits. By default selecting the MUTE pin to represent if DAC1 has received more than 1024 midrail samples will cause the MUTE pin to assert a softmute on DAC1. Disabling the decode block will cause any logical high on the MUTE pin to apply a softmute to all DAC's. For compatibility with the WM8772 register the MUTE pin decode bit is also found in the ADC control register, which is redundant on this chip. The OR of these two register bit is taken internally.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0001100<br>ADC Control | 6 | MPD | 0 | MUTE pin decode disable:<br>0: MUTE pin decode enable<br>1: MUTE pin decode disable |
| 0001111<br>DAC4 control | 5 | MPD | 0 | MUTE pin decode disable:<br>0: MUTE pin decode enable<br>1: MUTE pin decode disable |

### DAC DIGITAL VOLUME CONTROL

The DAC volume may also be adjusted in the digital domain using independent digital attenuation control registers

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| 0000000 Digital Attenuation DACL1 | 7:0 | LDA1[7:0] | 11111111 (0dB) | Digital Attenuation data for Left channel DACL1 in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store LDA1 in intermediate latch (no change to output)<br>1: Store LDA1 and update attenuation on all channels |
| 0000001 Digital Attenuation DACR1 | 7:0 | RDA1[6:0] | 11111111 (0dB) | Digital Attenuation data for Right channel DACR1 in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store RDA1 in intermediate latch (no change to output)<br>1: Store RDA1 and update attenuation on all channels. |
| 0000100 Digital Attenuation DACL2 | 7:0 | LDA2[7:0] | 11111111 (0dB) | Digital Attenuation data for Left channel DACL2 in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store LDA2 in intermediate latch (no change to output)<br>1: Store LDA2 and update attenuation on all channels. |
| 0000101 Digital Attenuation DACR2 | 7:0 | RDA2[7:0] | 11111111 (0dB) | Digital Attenuation data for Right channel DACR2 in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store RDA2 in intermediate latch (no change to output)<br>1: Store RDA2 and update attenuation on all channels. |
| 0000110 Digital Attenuation DACL3 | 7:0 | LDA3[7:0] | 11111111 (0dB) | Digital Attenuation data for Left channel DACL3 in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store LDA3 in intermediate latch (no change to output)<br>1: Store LDA3 and update attenuation on all channels. |
| 0000111 Digital Attenuation DACR3 | 7:0 | RDA3[7:0] | 11111111 (0dB) | Digital Attenuation data for Right channel DACR3 in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store RDA3 in intermediate latch (no change to output)<br>1: Store RDA3 and update attenuation on all channels. |
| 0001101 Digital Attenuation DACL4 | 7:0 | LDA3[7:0] | 11111111 (0dB) | Digital Attenuation data for Left channel DACL4 in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store LDA4 in intermediate latch (no change to output)<br>1: Store LDA4 and update attenuation on all channels. |
| 0001110 Digital Attenuation DACR4 | 7:0 | RDA3[7:0] | 11111111 (0dB) | Digital Attenuation data for Right channel DACR4 in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store RDA4 in intermediate latch (no change to output)<br>1: Store RDA4 and update attenuation on all channels. |
| 0001000 Master Digital Attenuation (all channels) | 7:0 | MASTDA [7:0] | 11111111 (0dB) | Digital Attenuation data for all DAC channels in 0.5dB steps. See Table 16 |
| | 8 | UPDATE | Not latched | Controls simultaneous update of all Attenuation Latches<br>0: Store gain in intermediate latch (no change to output)<br>1: Store gain and update attenuation on all channels. |

**Note:**

**When MCLK is removed, digital volume settings are re-set to default (0dB). When MCLK is re-applied, the user must write the desired volume level to the volume control registers.**

| L/RDAX[7:0] | ATTENUATION LEVEL |
|---|---|
| 00(hex) | -∞ dB (mute) |
| 01(hex) | -127.5dB |
| : | : |
| : | : |
| : | : |
| FE(hex) | -0.5dB |
| FF(hex) | 0dB |

**Table 16 Digital Volume Control Attenuation Levels**

### SOFTWARE REGISTER RESET

Writing to register 11111 will cause a register reset, resetting all register bits to their default values. This reset will last either 2*MCLK periods or until another write is made to the serial interface.

## REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8768 can be configured using the Control Interface. All unused bits should be set to '0'.

| REGISTER | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0(00h) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | UPDATE | LDA1[7:0] | | | | | | | | 011111111 |
| R1(01h) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | UPDATE | RDA1[7:0] | | | | | | | | 011111111 |
| R2(02h) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | PL[8:5] | | | | IZD | ATC | PDWN All DAC | DEEMP ALL DAC | MUTE All DAC | 100100000 |
| R3(03h) | 0 | 0 | 0 | 0 | 0 | 1 | 1 | PHASE[8:6] | | | DACIWL[5:4] | | DACBCP | DACLRP | DACFMT[1:0] | | 000000000 |
| R4(04h) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | UPDATE | LDA2[7:0] | | | | | | | | 011111111 |
| R5(05h) | 0 | 0 | 0 | 0 | 1 | 0 | 1 | UPDATE | RDA2[7:0] | | | | | | | | 011111111 |
| R6(06h) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | UPDATE | LDA3[7:0] | | | | | | | | 011111111 |
| R7(07h) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | UPDATE | RDA3[7:0] | | | | | | | | 011111111 |
| R8(08h) | 0 | 0 | 0 | 1 | 0 | 0 | 0 | UPDATE | MASTDA[7:0] | | | | | | | | 011111111 |
| R9(09h) | 0 | 0 | 0 | 1 | 0 | 0 | 1 | DEEMP[8:6] | | | DMUTE[5:3] | | | DZFM[2:1] | | ZCD | 000000000 |
| R10(0Ah) | 0 | 0 | 0 | 1 | 0 | 1 | 0 | DACRATE[8:6] | | | DACMS | PWRDN ALL | DACD[3:1] | | | 0 | 010000000 |
| R12(0Ch) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | MPD | 0 | 0 | 0 | 0 | 0 | 0 | 000000000 |
| R13(0Dh) | 0 | 0 | 0 | 1 | 1 | 0 | 1 | UPDATE | LDA4[7:0] | | | | | | | | 011111111 |
| R14(0Eh) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | UPDATE | RDA4[7:0] | | | | | | | | 011111111 |
| R15(0Fh) | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | MPD | DEEMP 4 | PHASE4 | DMUTE 4 | DZFM4 | DACD4 | 000000000 |
| R31(1Fh) | 0 | 0 | 1 | 1 | 1 | 1 | 1 | RESET | | | | | | | | | 000000000 |

## DIGITAL FILTER CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **DAC Filter** | | | | | |
| Passband | ±0.05 dB | | | 0.444fs | |
| | -3dB | | 0.487fs | | |
| Passband ripple | | | | ±0.05 | dB |
| Stopband | | 0.555fs | | | |
| Stopband Attenuation | f > 0.555fs | -60 | | | dB |
| Group Delay | | | 21 | | fs |

**Table 17 Digital Filter Characteristics**

## DAC FILTER RESPONSES

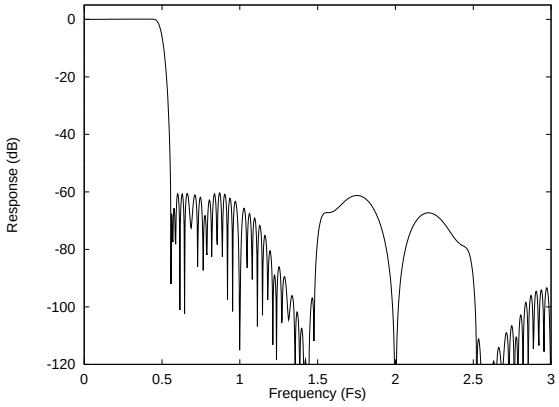



**Figure 21 DAC Digital Filter Frequency Response – 44.1, 48 and 96kHz**

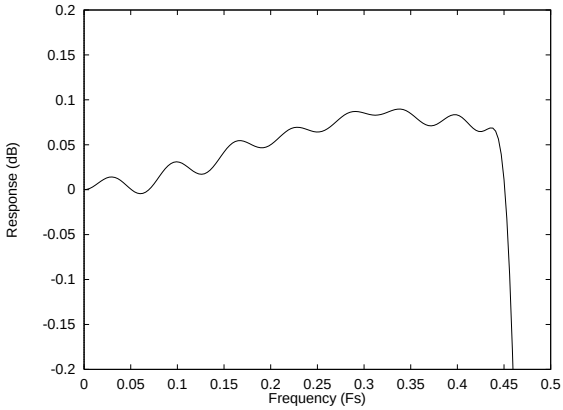



**Figure 22 DAC Digital Filter Ripple –44.1, 48 and 96kHz**

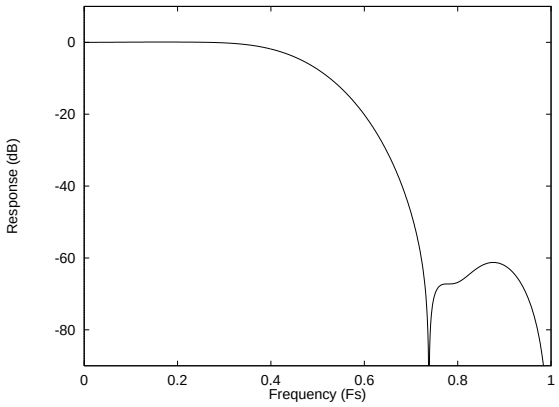



**Figure 23 DAC Digital Filter Frequency Response – 192kHz**

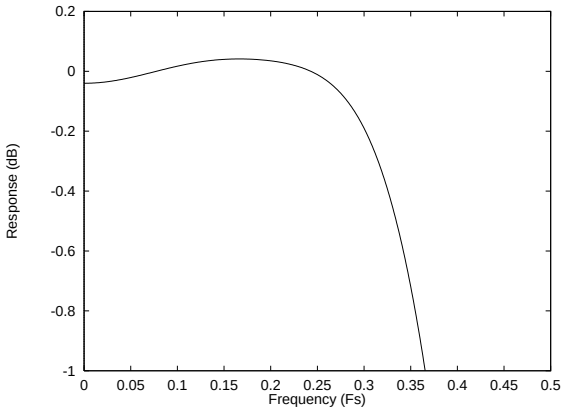



**Figure 24 DAC Digital filter Ripple – 192kHz**

## DIGITAL DE-EMPHASIS CHARACTERISTICS

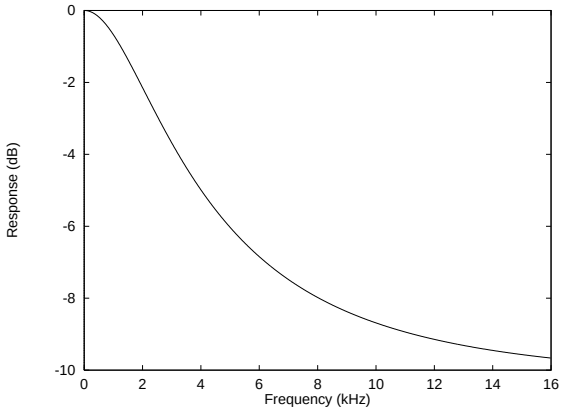



**Figure 25 De-Emphasis Frequency Response (32kHz)**

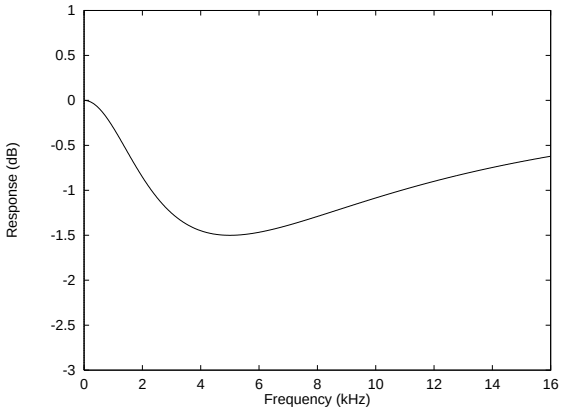



**Figure 26 De-Emphasis Error (32kHz)**

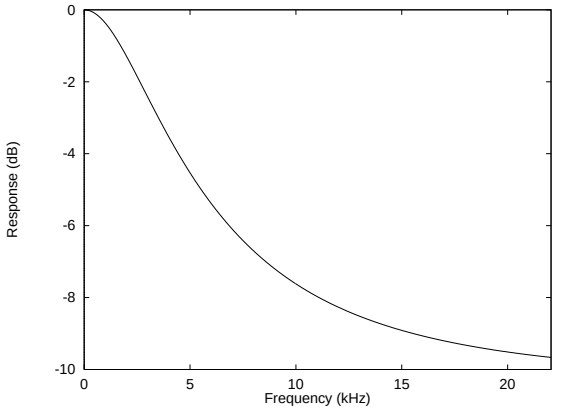



**Figure 27 De-Emphasis Frequency Response (44.1kHz)**

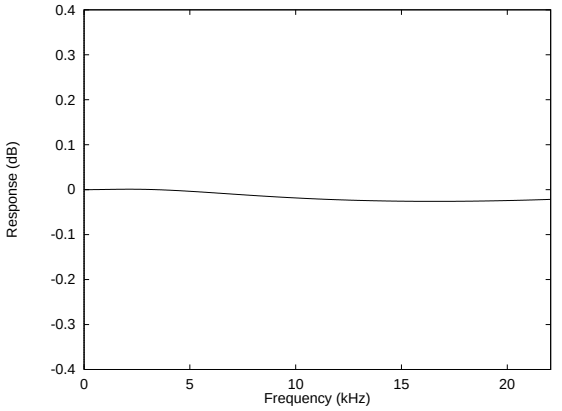



**Figure 28 De-Emphasis Error (44.1kHz)**

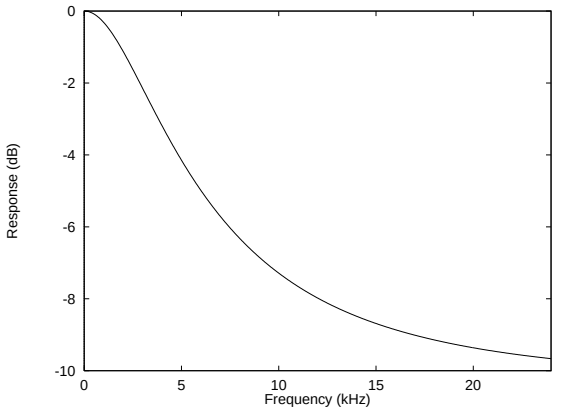



**Figure 29 De-Emphasis Frequency Response (48kHz)**

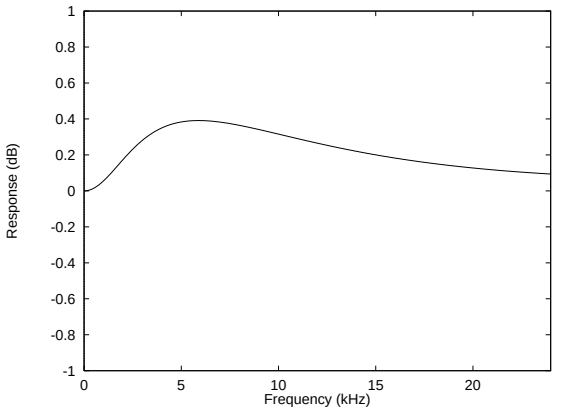



**Figure 30 De-Emphasis Error (48kHz)**

# APPLICATIONS INFORMATION

## RECOMMENDED EXTERNAL COMPONENTS

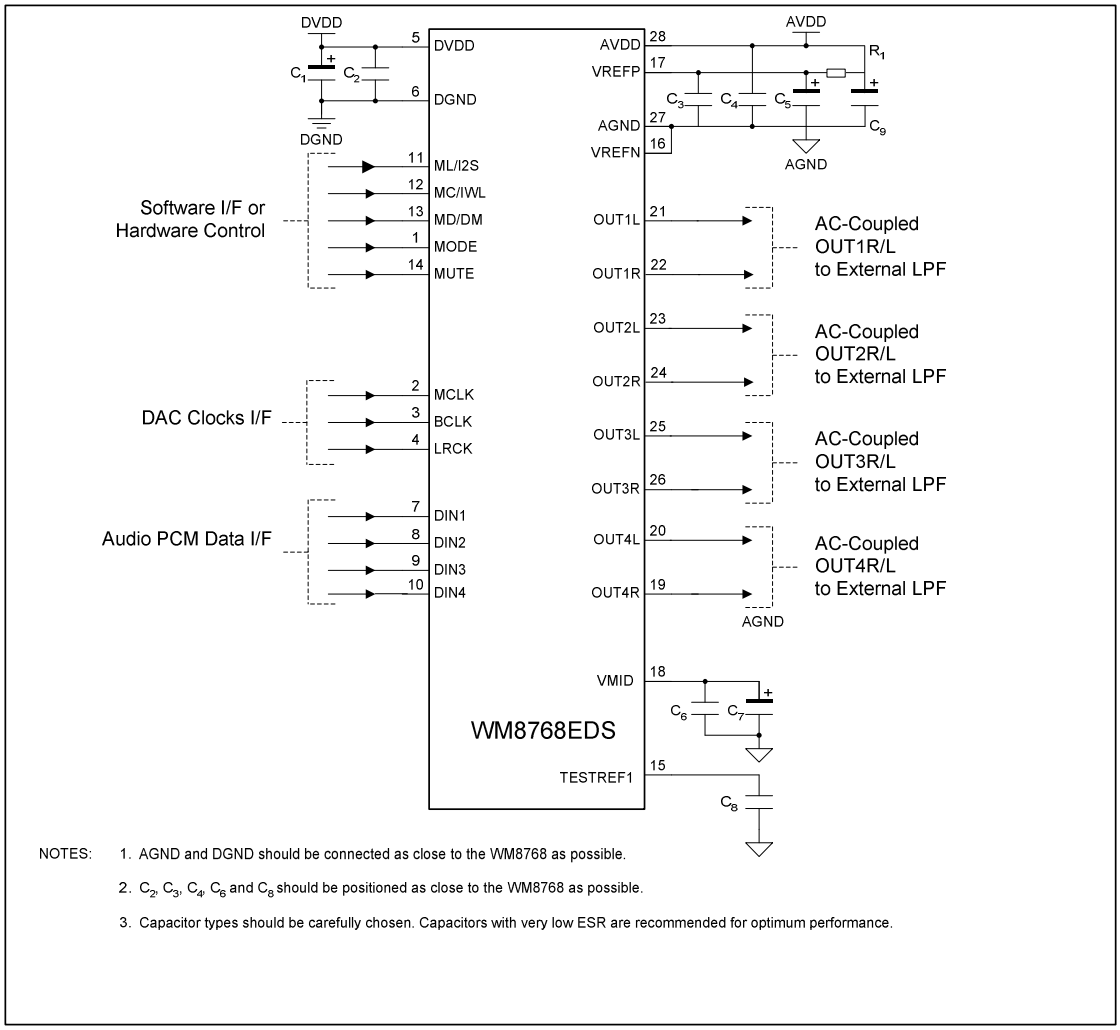



**Figure 31 Recommended External Component Diagram**

## RECOMMENDED EXTERNAL COMPONENTS VALUES

| COMPONENT REFERENCE | SUGGESTED VALUE | DESCRIPTION |
|---|---|---|
| C1 and C5 | 10µF | De-coupling for DVDD and AVDD. |
| C2 to C4 | 0.1µF | De-coupling for DVDD and AVDD. |
| C6 | 0.1µF | Reference de-coupling capacitors for VMID. |
| C7 | 10µF | |
| C8 | 0.1µF | De-coupling for TESTREF1 |
| C9 | 100µF | Filtering for VREFP. Omit if AVDD low noise. |
| R1 | 33Ω | Filtering for VREFP. Use 0Ω if AVDD low noise. |

**Table 18 External Components Description**

## SUGGESTED ANALOGUE LOW PASS POST DAC FILTERS

It is recommended that a lowpass filter be applied to the output from each DAC channel for Hi Fi applications. Typically a second order filter is suitable and provides sufficient attenuation of high frequency components (the unique low order, high bit count multi-bit sigma delta DAC structure used in WM8768 produces much less high frequency output noise than normal sigma delta DACs. This filter is typically also used to provide the 2x gain needed to provide the standard 2Vrms output level from most consumer equipment. Figure 32 shows a suitable post DAC filter circuit, with 2x gain. Alternative inverting filter architectures might also be used with as good results.

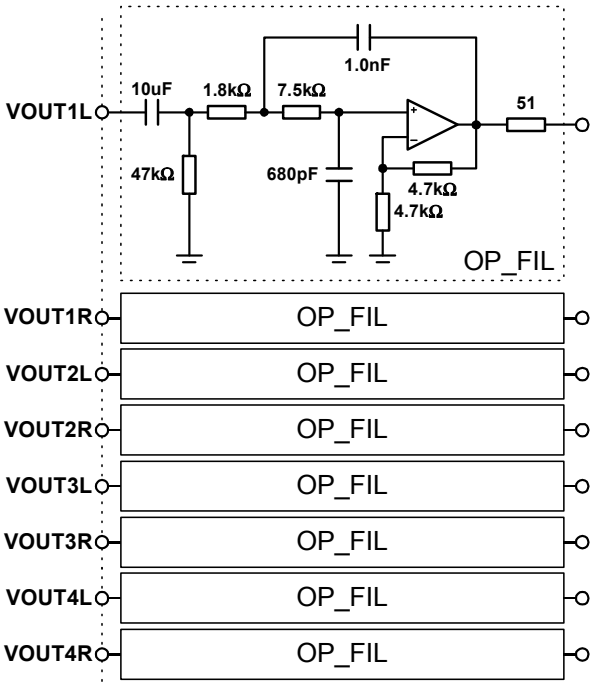
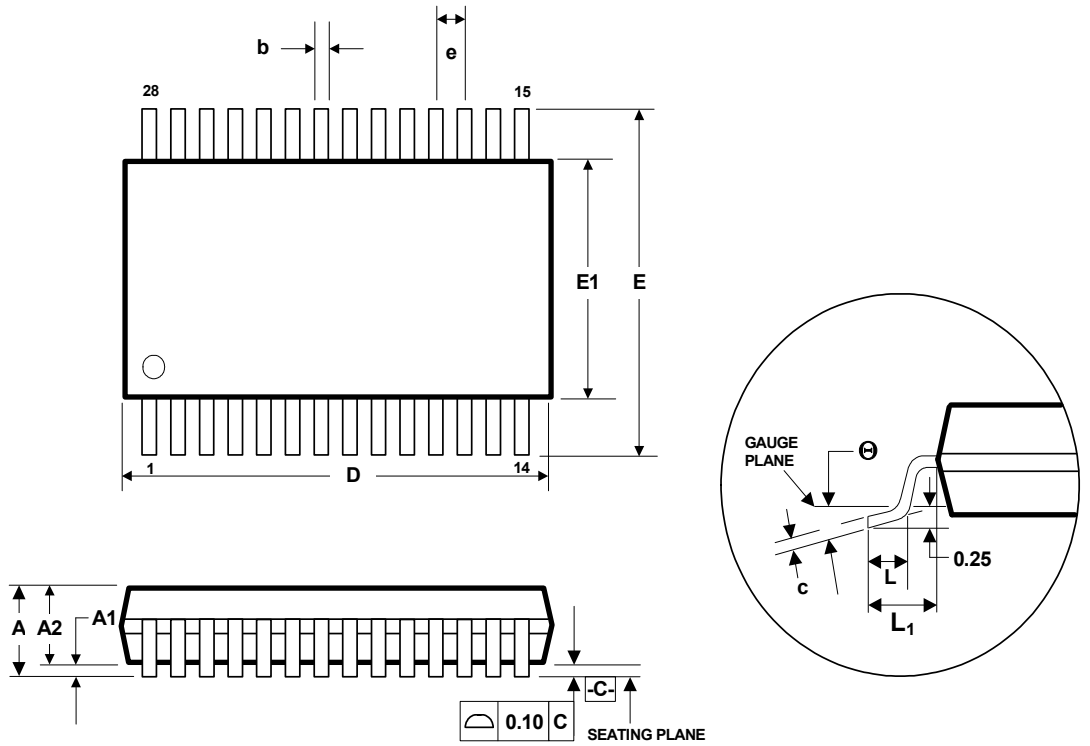



**Figure 32 Recommended Post DAC Filter Circuit**

## PACKAGE DRAWING

**DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm)** **DM007.E**




| Symbols | Dimensions (mm) | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | ----- | ----- | 2.0 |
| $A_1$ | 0.05 | ----- | 0.25 |
| $A_2$ | 1.65 | 1.75 | 1.85 |
| b | 0.22 | 0.30 | 0.38 |
| c | 0.09 | ----- | 0.25 |
| D | 9.90 | 10.20 | 10.50 |
| e | | 0.65 BSC | |
| E | 7.40 | 7.80 | 8.20 |
| $E_1$ | 5.00 | 5.30 | 5.60 |
| L | 0.55 | 0.75 | 0.95 |
| $L_1$ | | 1.25 REF | |
| θ | $0^o$ | $4^o$ | $8^o$ |
| | | | |
| REF: | JEDEC.95, MO-150 | | |

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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## ADDRESS:

Wolfson Microelectronics plc

Westfield House

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com