512K UVEPROM

UV Erasable Programmable Read-Only Memory

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-87648
- MIL-STD-883

FEATURES

- Organized 65,536 x 8
- High-reliability MIL-PRF-38535 processing
- Single +5V ±10% power supply
- Pin-compatible with existing 512K read-only memories (ROMs) and electrically programmable ROMs (EPROMs)
- All inputs/outputs fully TTL compatible
- Power-saving CMOS technology
- Very high-speed SNAP! Pulse Programming
- 3-state output buffers
- 400mV minimum DC noise immunity with standard TTL loads
- Latchup immunity of 250mA on all input and output lines
- Low power dissipation (CMOS input levels)
  - ✓Active - 193mW (MAX)
  - ✓Standby - 1.7mW (MAX)

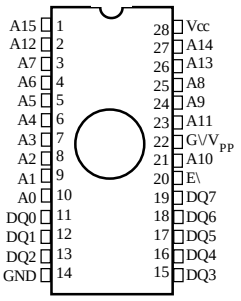
OPTIONS — MARKING

- **Timing**
  - 150ns access — -15
  - 200ns access — -20
  - 250ns access — -25
- **Package(s)**
  - Ceramic DIP (600mils) — J — No. 110
- **Operating Temperature Ranges**
  - Military (-55°C to +125°C) — M

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PIN ASSIGNMENT
(Top View)

28-Pin DIP (J) 600-Mils



Pin Name	Function
A0 - A15	Address Inputs
DA0-DQ7	Inputs (programming)/Outputs
E\	Chip Enable/Power Down
GND	Ground
G\ /V_{PP}	Output Enable/13V Programming
V_{CC}	5V Power Supply

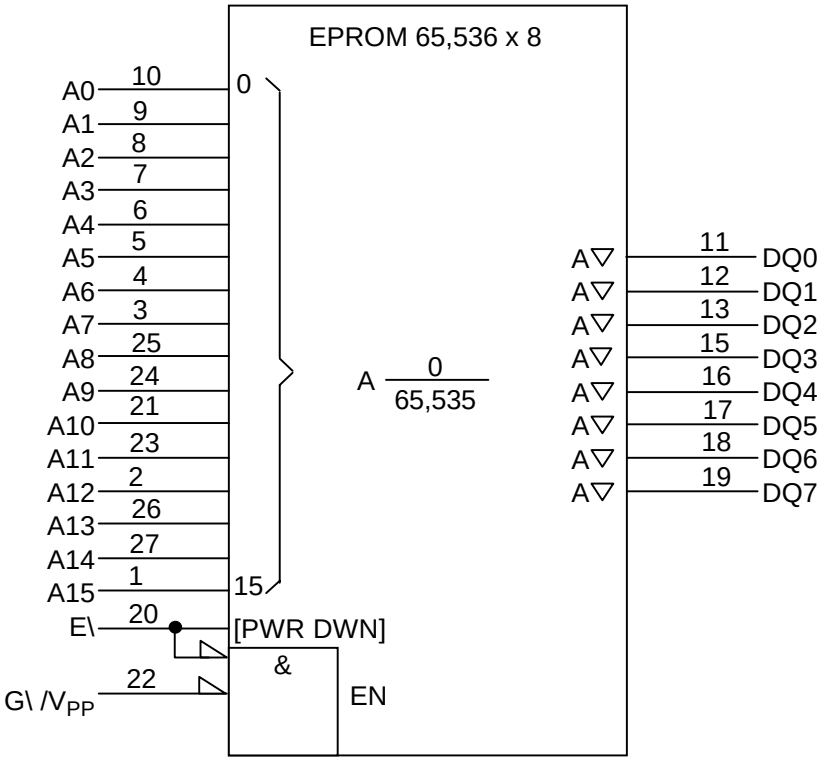
GENERAL DESCRIPTION

The SMJ27C512 is a set of 65536 by 8-bit (524,288-bit), ultraviolet (UV) light erasable, electrically programmable read-only memories. These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs can be driven by Series 54 TTL circuits without the use of external pullup resistors. Each output can drive one Series 54 TTL circuit without external resistors. The data outputs are 3-state for connecting multiple devices to a common bus. The SMJ27C512 is pin-compatible with existing 28-pin 512K ROMs and EPROMs.

Because this EPROM operates from a single 5V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other supply (13V) is needed for programming. All programming signals are TTL level. This device is programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13V and a V_{CC} of 6.5V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

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FUNCTIONAL BLOCK DIAGRAM*



* This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

OPERATION

The seven modes of operation for the SMJ27C512 are listed in Table 1. The read mode requires a single 5V supply. All inputs are TTL level except for V_{PP} during programming (13V for SNAP! Pulse), and 12V on A9 for signature mode.

TABLE 1. OPERATION MODES

FUNCTION (PINS)	MODE*							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
E\ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
G\ /V_{PP} (22)	V_{IL}	V_{IH}	X	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_{ID}	V_{ID}
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0-DQ7 (11-13, 15-19)	Data Out	High-Z	High-Z	Data In	Data Out	High-Z	CODE	
							MFG	DEVICE
							97h	85h

* X can be V_{IL} or V_{IH}

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READ/OUTPUT DISABLE

When the outputs of two or more SMJ27C512 are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of the selected SMJ27C512, a low-level signal is applied to the E\ and G\ /V_{PP}. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

LATCHUP IMMUNITY

Latchup immunity on the SMJ27C512 is a minimum of 250mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the printed circuit board level when the EPROM is interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

POWER DOWN

Active I_{CC} supply current can be reduced from 35mA to 500µA(TTL-level inputs) or 300µA (CMOS-level inputs) by applying a high TTL/CMOS signal to the E\ pin. In this mode all outputs are in the high-impedance state.

ERASURE

Before programming, the SMJ27512 is erased by exposing the chip through the transparent lid to a high-intensity ultra-violet (UV) light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic-high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity x exposure time) is 15 W·s/cm^2. A typical 12mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure; therefore, when using the SMJ27C512, the window should be covered with an opaque label.

SNAP! PULSE PROGRAMMING

The SMJ27C512 is programmed using the SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1. This algorithm programs in a nominal time of seven seconds. Actual programming time varies as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, E\ is pulsed. The SNAP! Pulse programming algorithm uses an initial pulse of 100µs followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to ten 100µs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when G\ /V_{PP} = 13V, V_{CC}= 6.5V, and E\ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = 5V, G\ /V_{PP} = V_{IL}, and E\ = V_{IL}.

PROGRAM INHIBIT

Programming can be inhibited by maintaining high level input on E\.

PROGRAM VERIFY

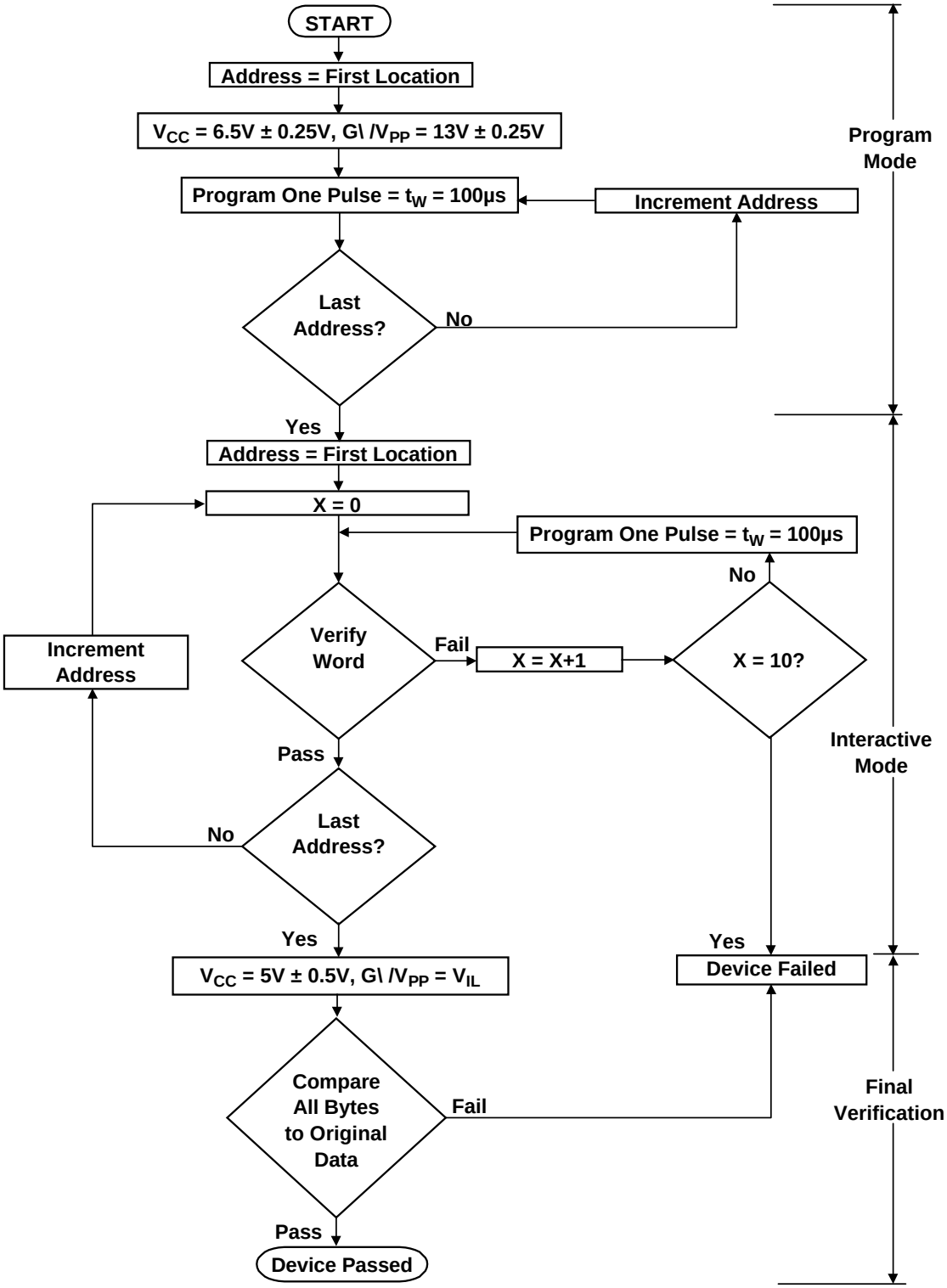
Programmed bits can be verified with G\ /V_{PP} and E\ = V_{IL}.

SIGNATURE MODE

The signature mode provides access to a binary code identifying the manufacturer and device type. This mode is activated when A9 (terminal 24) is forced to 12V ±0.5V. Two identifier bytes are accessed by A0 (terminal 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ0-DQ7; A0 = V_{IH} accesses the device code, which is also output on DQ0-DQ7. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit DQ7. The manufacturer code for these devices is 97h and the device code is 85h.

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FIGURE 1. SNAP! PULSE PROGRAMMING FLOW CHART



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range, V_{CC}**.....-0.6V to +7.0V
Supply Voltage Range, V_{pp}**.....-0.6V to +14.0V
Input Voltage Range, All inputs except A9**....-0.6V to 6.5V
A9....-0.6V to +13.5V
Output Voltage Range**.....-0.6V to V_{CC} +1V
Operating Cage Temperature Range, T_C.....-55°C to 125°C
Storage Temperature Range, T_{stg}.....-65°C to 150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
** All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

				MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage[1]	Read Mode		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
G\ /V_{PP}	Supply Voltage[2]	SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{ID}	Voltage level on A9 for signature mode			11.5		12.5	V
V_{IH}	High-level DC input voltage		TTL	2		V_{CC}+1	V
			CMOS	V_{CC}-0.2		V_{CC}+1	V
V_{IL}	Low-level DC input voltage		TTL	-0.5		0.8	V
			CMOS	-0.5		0.2	V
T_C	Operating case temperature			-55		125	°C

NOTES:

1. V_{CC} must be applied before or at the same time as G\ /V_{PP} and removed after or at the same time as G\ /V_{PP}. The deivce must not be inserted into or removed from the board when G\ /V_{PP} or V_{CC} is applied.
2. G\ /V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case is I_{CC} + I_{PP}.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF OPERATING CONDITIONS

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX
V_{OH}	High-level output voltage		I_{OH} = -400µA	2.4		
V_{OL}	Low-level output voltage		I_{OL} = 2.1mA			0.4
I_I	Input current (leakage)		V_I = 0V to 5.5V			10
I_O	Output current (leakage)		V_O = 0V to V_{CC}			10
I_{PP}	G\ /V_{PP} supply current (during program pulse)[2]		G\ /V_{PP} = 13V		35	70
I_{CC1}	V_{CC} supply current (standby)	TTL-Input Level	V_{CC} = 5.5V, E\=V_{IH}			500
		CMOS-Input Level	V_{CC} = 5.5V, E\=V_{CC}			325
I_{CC2}	V_{CC} supply current (active)		E\=V_{IL}, V_{CC}=5.5V t_{cycle} = minimum cycle time, outputs open		35	50

NOTES:

1. Typical values are at T_C=25°C and nominal voltages.
2. This parameter has been characterized at 25°C and is not production tested.

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CAPACITANCE OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING CASE TEMPERATURE, f = 1MHz*

PARAMETER		TEST CONDITIONS	TYP**	UNIT
C_I	Input capacitance	V_I = 0V	6	pF
C_O	Output capacitance	V_O = 0V	10	pF
C_G/V_{PP}	G\ /V_{PP} input capacitance	G\ /V_{PP} = 0V	20	pF

* Capacitance measurements are made on sample basis only.

** All typical values are at T_C = 25°C and nominal voltages.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING CASE TEMPERATURE

PARAMETER		TEST CONDITIONS[1,2]	-15		-20		-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 2		150		200		250	ns
$t_{a(E)}$	Access time from E\			150		200		250	ns
$t_{en(G)}$	Output enable time from G\ /V_{PP}			70		75		100	ns
t_{dis}	Output disable time from G\ /V_{PP} or E\, whichever occurs first[3]		0	50	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, E\, or G\, whichever occurs first[3]		0		0		0		ns

NOTES:

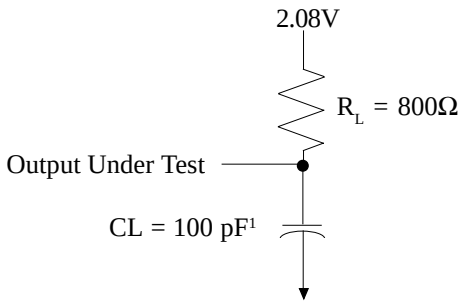
1. Timing measurements are made at 2V for logic high and 0.8V for logic low. (see Figure 2)
2. Common test conditions apply for t_{dis} except during programming.
3. Value calculated from 0.5V delta to measured output level. This parameter is only sampled and not 100% tested.

RECOMMENDED TIMING REQUIREMENTS FOR PROGRAMMING: V_{CC} = 6.5V and G\ /V_{PP} = 13V (SNAP! Pulse), T_C = 25°C (see Figure 2)

		MIN	NOM	MAX	UNIT
$t_{dis(E)}$	Output disable time from E\	0		130	ns
$t_{h(A)}$	Hold Time, address	0			µs
$t_{h(D)}$	Hold time, address	2			µs
$t_{h(VPP)}$	Hold time, G\ /V_{PP}	2			µs
$t_{w(IPGM)}$	Pulse duration, initial program	95	100	105	µs
$t_{rec(PG)}$	Recovery time, G\ /V_{PP}	2			µs
$t_{su(A)}$	Setup Time, Address	2			µs
$t_{su(D)}$	Setup Time, Data	2			µs
$t_{su(Vpp)}$	Setup Time, G\ /V_{PP}	2			µs
$t_{su(Vcc)}$	Setup Time, V_{CC}	2			µs
$t_{v(ELD)}$	Data valid from E\ low			1	µs
$t_{r(PG)}$	G\ /V_{PP} rise time	50			ns

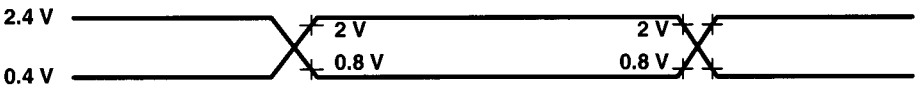
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PARAMETER MEASUREMENT INFORMATION



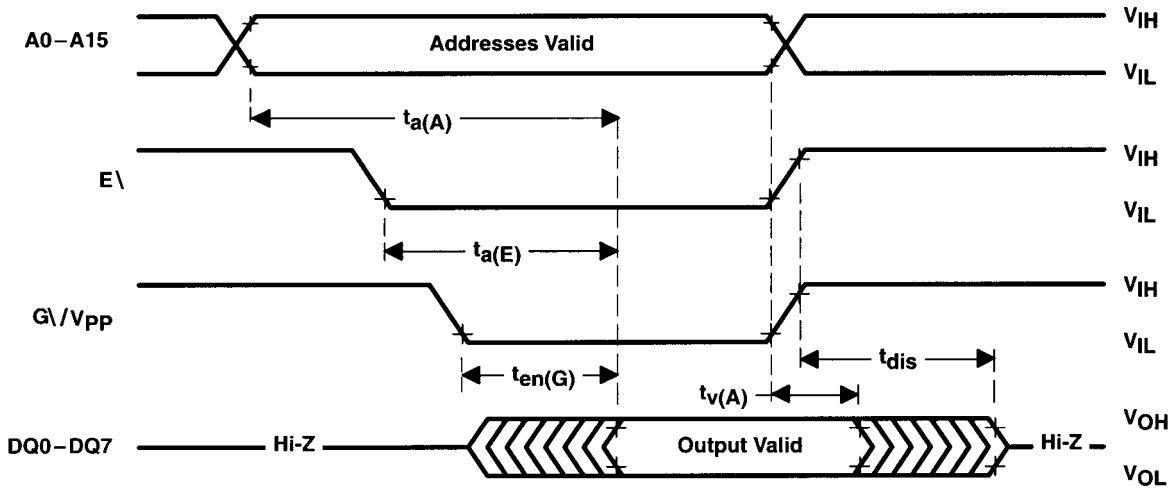
NOTES:
1. C_L includes probe and fixture capacitance.

FIGURE 2. LOAD CIRCUIT AND VOLTAGE WAVEFORM



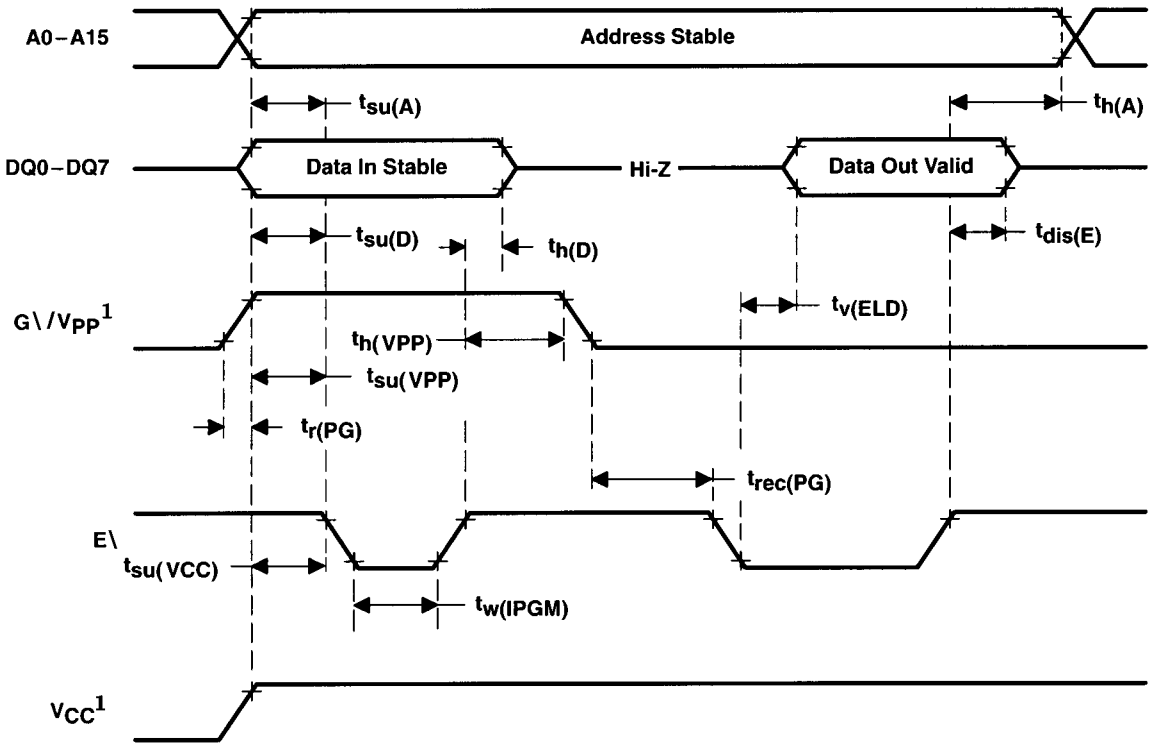
AC testing inputs are driven at 2.4V for logic high and 0.4V for logic low. Timing measurements are made at 2V for logic high and 0.8V for logic low for both inputs and outputs.

FIGURE 3. READ-CYCLE TIMING



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FIGURE 4. PROGRAM-CYCLE TIMING (SNAP! PULSE PROGRAMMING)

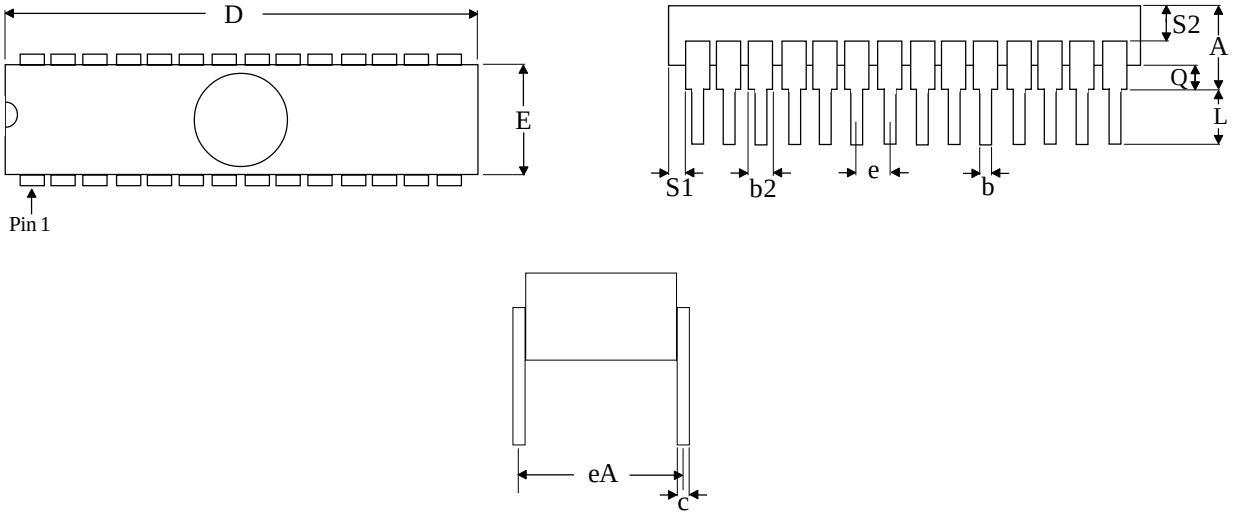


NOTES:

1. $G\backslash/V_{PP}$ = 13V and V_{CC} = 6.5V for SNAP! Pulse programming.

MECHANICAL DEFINITION*

ASI Case #110 (Package Designator J)
SMD 5962-87648, Case Outline X



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.232
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	---
S2	0.005	---

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

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ORDERING INFORMATION

EXAMPLE: SMJ27C512-25JM

Device Number	Speed ns	Package Type	Operating Temp.
SMJ27C512	-15	J	*
SMJ27C512	-20	J	*
SMJ27C512	-25	J	*

***AVAILABLE PROCESSES**

M = Extended Temperature Range -55°C to +125°C

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ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator J

TI Part #**	SMD Part #
SMJ27C512-15JM	5962-8764801XA
SMJ27C512-20JM	5962-8764802XA
SMJ27C512-25JM	5962-8764803XA

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*
*** Parts are listed on SMD under the old Texas Instruments part number. ASI purchased this product line in November of 1999.*

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