Ninja C/CX (ADM6992C/CX)

Two Port Bridge Fiber to Fast Ethernet Converter

Communications

Never stop thinking.

Edition 2005-11-25

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1 Product Overview

Features and the block diagram.

1.1 Overview

The NINJA C/CX (ADM6992C/CX) is a single chip integrating two 10/100 Mbps MDIX TX/FX transceivers with a two-port 10/100M Ethernet L2 switch controller. Features include a converter mode to meet demanding applications, such as Fiber-to-Ethernet media converters. The ADM6992CX is the environmentally friendly “green” package version.

The NINJA C/CX (ADM6992C/CX) supports 16 entries of packet classification and marking or filtering for TCP/UDP port numbering, IP protocol ID and Ethernet Type. These can be configured either using the EEPROM or on-the-fly using a small, low-cost micro controller.

On the media side, the NINJA C/CX (ADM6992C/CX)’s 0 and 1 ports support auto-MDIX 10Base-T/100Base-TX and 100Base-FX as specified by the IEEE 802.3 committee through uses of digital circuitry and high speed A/D.

The NINJA C/CX (ADM6992C/CX) also supports a serial management interface (SMI), which is initialized and configured using a small low-cost micro controller. It also provides the port status for remote agent monitoring and a smart counter for reporting port statistics.

1.2 Features

Main features:

- 2-port10/100M switch integrated with a 2-port PHY (10/100TX and 100FX)
- Provides TX<--> FX Converter modes with Link Pass Through (LPT)
- Built-in data buffer 6Kx64bit SRAM
- Up to 1k of Unicast. MAC addresses with a 4-way associative hashing table
- MAC address learning table with aging function
- Supports store & forward frame forwarding, modify cut-through frame forwarding, and fast cut-through frame forwarding.
- Forwarding and filtering at non-blocking full wire speed
- 802.3x flow control for full duplex and back-pressure for half duplex
- Supports Auto-Negotiation
- Supports Auto Cross-Over
- Packet lengths up to 9216 bytes.
- 16 entries of packet classification and marking or filtering for TCP/UDP Port Numbering, IP Protocol ID and Ethernet Type
- Serial Management Interface for low-end CPU
- Hardware bandwidth control support for both ingress/egress traffic
- Provides port status for remote agent monitoring
- Provides smart counters for port statistics reporting
- 64 LQFP packaging with 1.8 V/3.3 V power supply

1.3 Block Diagram

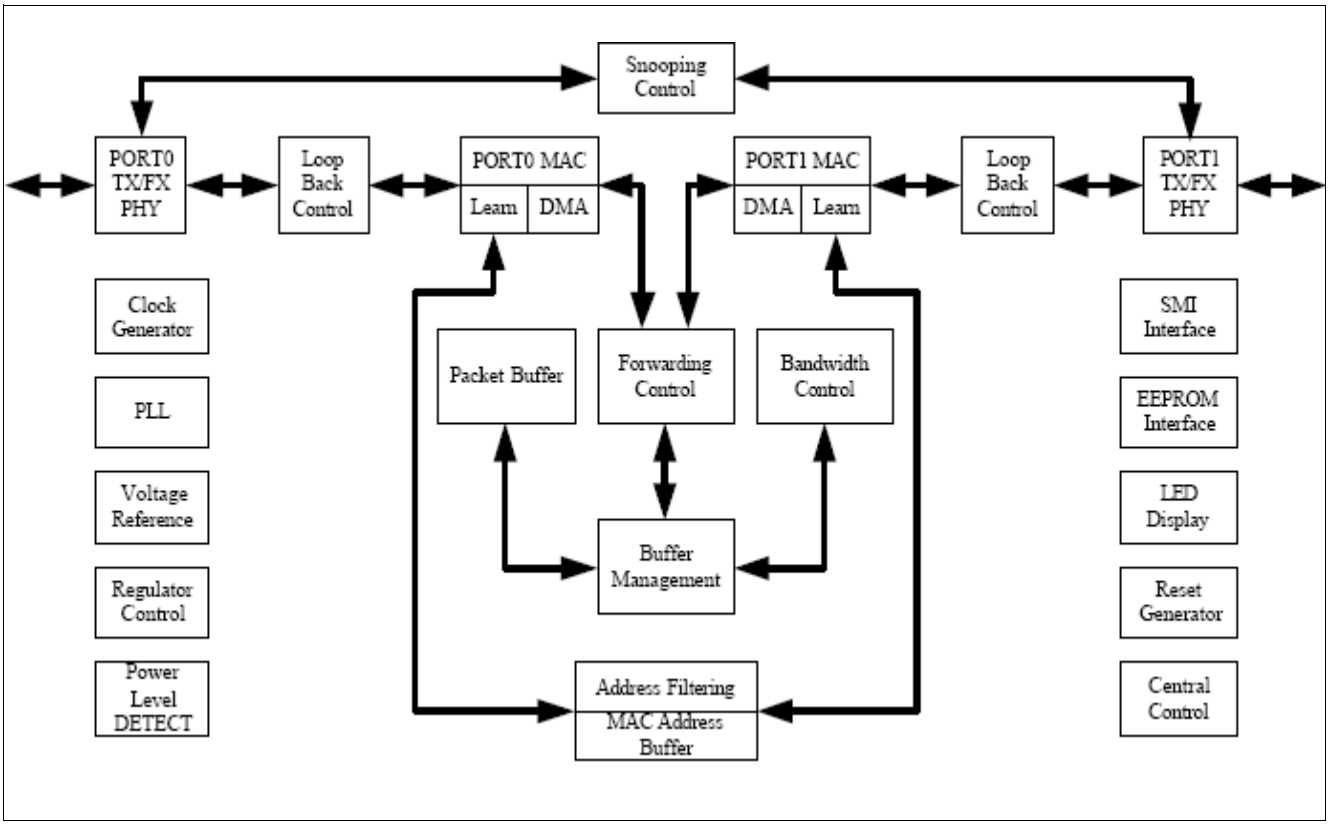


Figure 1 NINJA C/CX (ADM6992C/CX) Block Diagram

1.4 Data Lengths Conventions

Table 1 Data Lengths Conventions

qword	64 bits
dword	32 bits
word	16 bits
byte	8 bits
nibble	4 bits

2 NINJA C/CX Interface Description

This chapter describes Pin Diagram, Pin Type and Buffer Type Abbreviations, and Pin Descriptions.

2.1 Pin Diagram

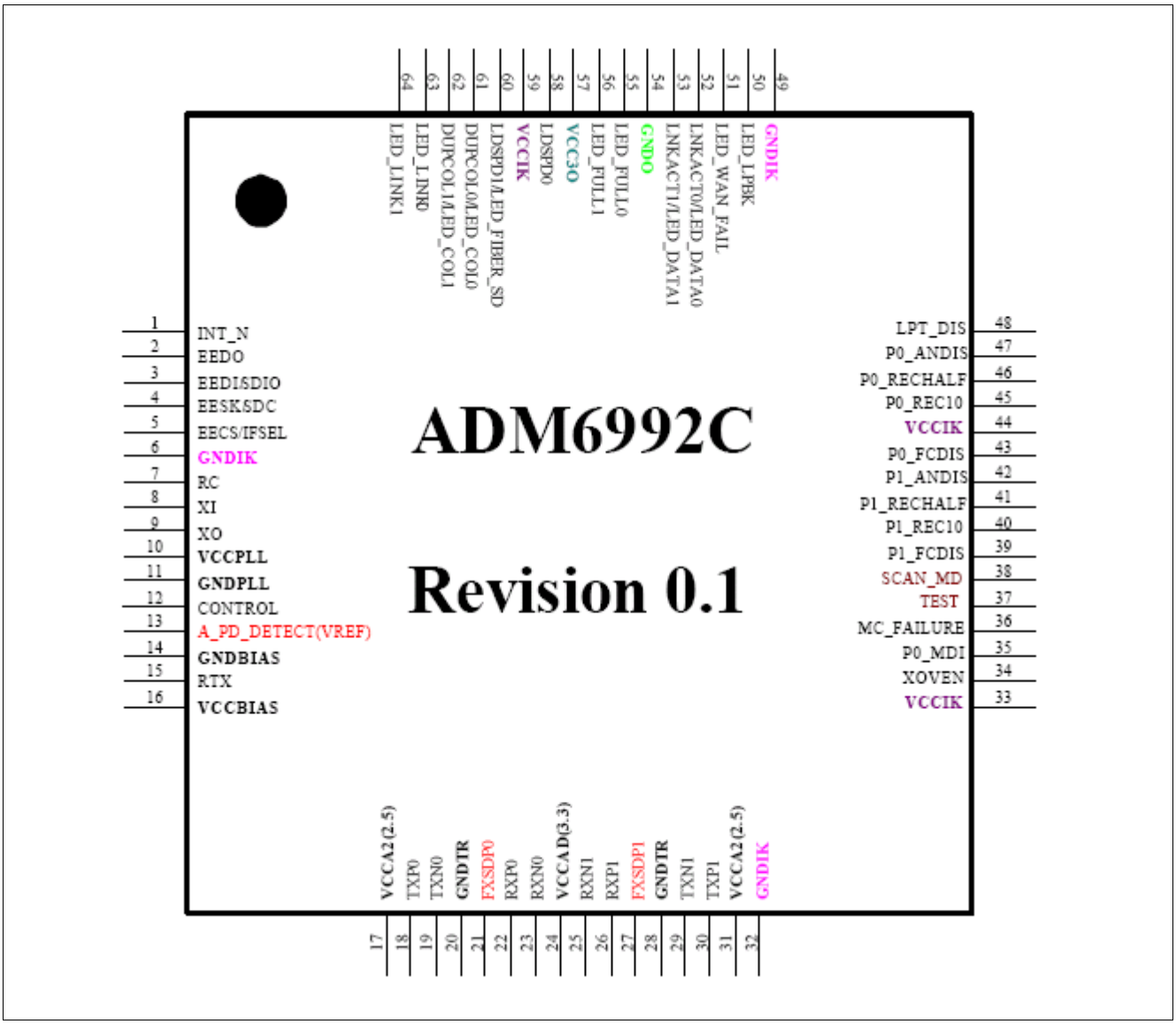


Figure 2 NINJA C/CX (ADM6992C/CX) 64-Pin Assignment

2.2 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

Table 2 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 3 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Descriptions

Interfaces:

- Port 0/1 Twisted Pair Interface, 8 pins
- LED Interface, 12 pins
- EEPROM Interface, 4 pins
- Configuration Interface, 28 pins
- Ground/Power Interface, 27 pins
- Miscellaneous, 14 pins

Note: If not specified, all signals default to digital signals.

Table 4 Port 0/1 Twisted Pair Interface (8 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
18	TXP_0	AI/O		**Twisted Pair Transmit** Output Positive.
30	TXP_1	AI/O		
19	TXN_0	AI/O		**Twisted Pair Transmit** Output Negative.
29	TXN_1	AI/O		
22	RXP_0	AI/O		**Twisted Pair Receive** Input Positive.
26	RXP_1	AI/O		
23	RXN_0	AI/O		**Twisted Pair Receive** Input Negative.
25	RXN_1	AI/O		
21	FXSDP_0	AI		**OMD Signal Detect In**
27	FXSDP_1	AI		

Table 5 LED Interface (12 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
52	LNKACT_0	I/O	TTL, PD, 8mA	**PORT0 Link & Active LED/Link LED.** If LEDMODE_0 is 1, this pin indicates both link status and RX/TX activity. When link status is LINK_UP, LNKACT_0 will be turned on. While PORT0 is receiving/transmitting data, LNKACT_0 will be off for 100ms and then on for 100ms. If LEDMODE[0] is 0, this pin only indicates RX/TX activity.
	LED_DATA_0			
	LEDMODE_0			**LED mode for LINK/ACT LED of PORT0.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as LEDMODE_0.

Table 5 LED Interface (12 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
53	LNKACT_1	I/O	TTL, PD, 8mA	**PORT1 Link & Active LED/Link LED.** If LEDMODE_2 is 1, this pin indicates both link status and RX/TX activity. When link status is LINK_UP, LNKACT_1 will be turned on. While PORT1 is receiving/transmitting data, LNKACT_1 will be off for 100ms and then on for 100ms. If LEDMODE[2] is 0, this pin only indicates RX/TX activity.
	LED_DATA_1			
	LEDMODE_1			**LED mode for LINK/ACT LED of PORT0 & PORT1.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as LEDMODE_1. If LEDMODE_1 is 1, DUPCOL[1:0] will display both duplex condition and collision status. If LEDMODE_1 is 0, only collision status will be displayed.
61	DUPCOL_0	I/O	TTL, PD, 8mA	**PORT0 Duplex/Collision LED** If LEDMODE_1 is 1, this pin indicates both duplex condition and collision status. When FULL_DUPLEX, this pin will be turned on for PORT0. When HALF_DUPLEX and no collision occurs, this pin will be turned off. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and then on for 100ms. If LEDMODE_1 is 0, this pin indicates collision status. When in HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and turn on for 100ms.
	LED_COL_0			**Collision LED**
	DIS_LEARN			**Disable Address Learning.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as DIS_LEARN. If DIS_LEARN is 1, MAC address learning will be disabled.
62	DUPCOL_1	I/O	TTL, PU, 8mA	**PORT1 Duplex** If LEDMODE_1 is 1, this pin indicates both duplex condition and collision status. When FULL_DUPLEX, this pin will be turned on for PORT1. When HALF_DUPLEX and no collision occurs, this pin will be turned off. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and then on for 100ms. If LEDMODE_1 is 0, this pin indicates collision status. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and turn on for 100ms.
	LED_COL_1			**Collision LED**
58	LDSPD_0	I/O	TTL, PD, 8mA	**PORT0 Speed LED** Used to indicate speed status of PORT0. When operating in 100Mbps this pin is turned on, and when operating in 10Mbps this pin is off.
	FXMODE0			**FXMODE0** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as bit 0 of FXMODE.

Table 5 LED Interface (12 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
60	LDSPD_1	I/O	TTL, PD, 8mA	**Speed LED, PORT1** Used to indicate speed status of PORT1. When operating in 100Mbps this pin is turned on, and when operating in 10Mbps this pin is off.
	LED_FIBER_SD			**LED_FIBER_SD.** Used to indicate signal status of PORT1 when NINJA C/CX (ADM6992C/CX) is operating in converter mode.
	LEDMODE2			**LED mode for LINK/ACT LED of PORT1.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as LEDMODE2. 0_B **TBD**, ACT 1_B **TBD**, LINK/ACT
63	LED_LINK_0	I/O	TTL, PU, 8mA	**PORT0 Link LED** This pin indicates link status. When Port0 link status is LINK_UP, this pin will be turned on.
	FXMODE1			**FXMODE1** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as bit 1 of FXMODE. FXMODE [1:0] Interface 00_B **TBD**, Both Port0 & Port1 are TP port 01_B **TBD**, Port0 is TP port and Port1 is FX port 10_B **TBD**, Port0 is TP port and Port1 is FX port (converter mode) 11_B **TBD**, Both Port0 & Port1 are FX port
64	LED_LINK_1	I/O	TTL, PU, 8mA	**PORT1 Link LED** This pin indicates link status. When Port1 link status is LINK_UP, this pin will be turned on.
	BYPASS_PAUSE			**Bypass frame** which destination address is reserved IEEE MAC address. During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as BYPASS_PAUSE. 0_B **D**, Disable 1_B **E**, Enable
55	LED_FULL_0	I/O	TTL, PU, 8mA	**PORT0 Full Duplex LED** This pin indicates current duplex condition of PORT0. When FULL_DUPLEX, this pin will be turned on. When HALF_DUPLEX this pin will be turned off.
	$\overline{\text{CHIPID_0}}$			**Chip ID Bit 0.** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as $\overline{\text{CHIPID_0}}$.

Table 5 LED Interface (12 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
56	LED_FULL_1	I/O	TTL, PU, 8mA	**PORT1 Full Duplex LED** This pin indicates current duplex condition of PORT1. When FULL_DUPLEX, this pin will be turned on. When HALF_DUPLEX this pin will be turned off.
	$\overline{\text{CHIPID_1}}$			**Chip ID Bit 1** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as $\overline{\text{CHIPID_1}}$. [$\overline{\text{CHIPID_1}}$:$\overline{\text{CHIPID_0}}$] 00_B **TBD**, Master Device 01_B **TBD**, Slave Device $1X_B$ **TBD**, Slave Device
50	LED_LPBK	I/O	TTL, PU, 8mA	**Loop Back Test LED** While performing loop back test this pin is turned on.
	$\overline{\text{CHIPID_2}}$			**Chip ID Bit 2** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as $\overline{\text{CHIPID_2}}$.
51	LED_WAN_FAIL	O	TTL, PD, 8mU	**WAN Fail LED** When receiving an OAM frame which has a S2 bit = 1, this pin is turned on.
	$\overline{\text{DISBP}}$			**Disable Back Pressure** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as $\overline{\text{DISBP}}$. 0_B **E**, Enable back-pressure (Default) 1_B **D**, Disable back-pressure

Table 6 EEPROM Interface (4 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
2	EEDO	I	TTL, PU	**EEPROM Data Output** Serial data input from EEPROM. This pin is internal pull-up.
5	EECS/IFSEL	I/O	PD, 4mA	**EEPROM Chip Select** This pin is an active high chip enabled for EEPROM. When RESETL is low, it will be tristate. 0_B **SM**, Select Serial Management Interface 1_B **EE**, Select EEPROM interface

Table 6 EEPROM Interface (4 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
4	EECK/SDC	I/O	TTL, PU, 4mA	**Serial Clock** This pin is the EEPROM clock source. When RESETL is low, it will be tristate. This pin is internal pull-up. If IFSEL is 1, this pin is used as EECK. If IFSEL is 0, this pin is used as SDC.
3	EEDI/SDIO	I/O	TTL, PU, 4mA	**EEPROM Serial Data Input** This pin is the output for serial data transfer. When RESETL is low, it will be tristate. If IFSEL is 1, this pin is used as EEDI. If IFSEL is 0, this pin is used as SDIO.

Table 7 Configuration Interface (28 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
47	P0_ANDIS	I	TTL, PD	**Auto-Negotiation Disable for PORT0** 0_B **E**, Enable 1_B **D**, Disable
46	P0_RECHALF	I	TTL, PD	**Recommend Half Duplex Communication for PORT0** 0_B **F**, Full 1_B **H**, Half
45	P0_REC10	I	TTL, PD	**Recommend 10M for PORT0** 0_B **100**, 100M 1_B **10**, 10M
43	P0_FCDIS	I	TTL, PD	**Flow Control Disable for PORT0** 0_B **E**, Enable 1_B **D**, Disable
42	P1_ANDIS	I	TTL, PD	**Auto-Negotiation Disable for PORT1** 0_B **E**, Enable 1_B **D**, Disable
41	P1_RECHALF	I	TTL, PD	**Recommend Half Duplex Communication for PORT1** 0_B **F**, Full 1_B **H**, Half
40	P1_REC10	I	TTL, PD	**Recommend 10M for PORT1** 0_B **100**, 100M 1_B **10**, 10M
39	P1_FCDIS	I	TTL, PD	**Flow Control Disable for PORT1** 0_B **E**, Enable 1_B **D**, Disable

Table 7 Configuration Interface (28 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
34	XOVEN	I	TTL, PU	**Auto-MDIX Enable.** 0_B **D**, Disable 1_B **E**, Enable
35	P0_MDI	I	TTL, PU	**MDI/MDIX Control for PORT0** This setting will be ignored if enabled Auto-MDIX. 0_B **MDIX**, MDIX 1_B **MDI**, MDI

Table 8 Ground/Power Interface (27 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
20, 28	GNDTR	GND, A		**Ground used by AD receiver/transmitter block.**
17, 31	VCCA2	PWR, A		**1.8 V used for Analogue block**
24	VCCAD	PWR, A		**3.3 V used for TX line driver**
14	GNDBIAS	GND, A		**Ground used by digital substrate**
16	VCCBIAS	PWR, A		**3.3 V used for bios block**
11	GNDPLL	GND, A		**Ground used by PLL**
10	VCCPLL	PWR, A		**1.8 V used for PLL**
6, 32, 49	GNDIK	GND, A		**Ground used by digital core and pre-driver**
33, 44, 59	VCCIK	PWR, D		**1.8 V used for digital core and pre-driver**
54	GNDO	GND, D		**Ground used by digital pad**
57	VCC3O	PWR, D		**3.3 V used for digital pad.**

Table 9 Miscellaneous (14 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
1	$\overline{\text{INT}}$	O	TTL, OD, 4mA	**Interrupt** This pin will be used to interrupt external management device. When EEPROM register 0x5 Bit [15] is 0, this pin is low-active. When EEPROM register 0x5 Bit [15] is 1, this pin is high-active.
12	CONTROL	AO		**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator.
15	RTX	A		**TX Resistor**
13	A_PD_DETECT	A		**Analog Reference Voltage**
7	RC	I	TTL, ST	**RC Input for Power On Reset** NINJA C/CX (ADM6992C/CX) sample pin RC as RESETL with the clock input from pin XI.

Table 9 Miscellaneous (14 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
8	XI	AI		**25M Crystal Input** 25M Crystal Input. Variation is limited to +/- 50ppm.
9	XO	AO		**25M Crystal Output** When connected to oscillator, this pin should left unconnected.
37	TEST	I	TTL, PD	**Test pin** During power on reset, value will be latched by NINJA C/CX (ADM6992C/CX) at the rising edge of RESETL as TEST. Connect to GND at normal application.
38	SCAN_MD	I	TTL, PD	**Scan Mode** For Test Only. Connect to GND at normal application.

3 Function Description

The NINJA C/CX (ADM6992C/CX) integrates two 100Base-X physical layer devices (PHY), two complete 10BaseT modules, a two-port 10/100 switch controller and memory into a single chip for both 10Mbps and 100 Mbps Ethernet switch operation. It also supports 100Base-FX operations through external fiber-optic transceivers. The device is capable of operating in either Full-Duplex or Half-Duplex mode in both 10 Mbps and 100 Mbps operation. Operation modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The NINJA C/CX (ADM6992C/CX) consists of four major blocks:

- OAM Engine
- 10/100M PHY Block
- Switch Controller Block
- Built-in 6Kx64 SSRAM

3.1 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- 100Base-X physical medium dependent (PMD)

The 10Base-T section of the device implements the following functional blocks:

- 10Base-T physical layer signaling (PLS)
- 10Base-T physical medium attachment (PMA)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interfaces used for the communication between the PHY block and switch core is a MII interface.

An Auto MDIX function is supported. This function can be Enabled/Disabled using the hardware pin. A digital approach for the integrated PHY of the NINJA C/CX (ADM6992C/CX) has been adopted.

3.2 Auto Negotiation and Speed Configuration

3.2.1 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operations supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further details regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The NINJA C/CX (ADM6992C/CX) supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the NINJA C/CX (ADM6992C/CX) can be controlled either by internal register access or by the use of configuration pins. If disabled, auto negotiation will not occur until software enables bit 12 in MII Register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the NINJA C/CX (ADM6992C/CX) transmits the abilities programmed into the auto negotiation advertisement register at address 04_H via FLP bursts. Any combination of 10 Mbps, 100 Mbps, half duplex, and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiating, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05_H.

The contents of the “auto negotiation link partner ability register” are used to automatically configure the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation, by comparing the contents of register 04_H and 05_H and then selecting the technology whose bit is set in both registers of highest priority relative to the following list:

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

The basic mode control register at address 0_H controls the enabling, disabling and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbps or 100 Mbps operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operations when the auto negotiation enabled bit (bit 12) is set.

The basic mode status register at address 1_H indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the NINJA C/CX (ADM6992C/CX). The BMSR also provides status on:

- Whether auto negotiation is complete (bit 5)
- Whether the Link Partner is advertising that a remote fault has occurred (bit 4)
- Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 04_H indicates the auto negotiation abilities to be advertised by the NINJA C/CX (ADM6992C/CX). All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05_H indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bit (bit 5, register address 1_H) is set.

3.2.2 Speed Configuration

The twelve sets of four pins listed in **Table 10** configure the speed capability of each channel of the NINJA C/CX (ADM6992C/CX). The logic states of these pins are latched into the advertisement register (register address 4_H)

for auto negotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 0_H) according to **Table 10**.

In order to make these pins have the same Read/Write priority as software, they should be programmed to 11111111_B in case a user wishes to update the advertisement register through software.

Table 10 Speed Configuration

Advertise all capability	Advertise single capability	Parallel detect follow IEEE std.	Auto Negoti-ation (Pin & EEPROM)	Speed (Pin & EEPROM)	Duplex (Pin & EEPROM)	Auto Negotiation	Advertise Capability				Parallel Detect Capability			
							10 0F	10 0H	10 F	10 H	10 0F	10 0H	10 F	10 H
1	0	0	1	X	X	1	1	1	1	1	1	0	1	0
1	0	1	1	X	X	1	1	1	1	1	0	1	0	1
1	1	0	1	X	X	1	1	0	0	0	1	0	0	0
1	1	1	1	X	X	1	1	0	0	0	0	1	0	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	1	1	0	1	0	1
0	1	0	1	1	1	1	1	0	0	0	1	0	0	0
0	1	1	1	1	1	1	1	0	0	0	0	1	0	0
0	0	X	1	1	0	1	0	1	0	1	0	1	0	1
0	1	X	1	1	0	1	0	1	0	0	0	1	0	0
0	0	0	1	0	1	1	0	0	1	1	0	0	1	0
0	0	1	1	0	1	1	0	0	1	1	0	0	0	1
0	1	0	1	0	1	1	0	0	1	0	0	0	1	0
0	1	1	1	0	1	1	0	0	1	0	0	0	0	1
0	X	X	1	0	0	1	0	0	0	1	0	0	0	1
X	X	X	0	1	1	0	1	—	—	—	—	—	—	—
X	X	X	0	1	0	0	—	1	—	—	—	—	—	—
X	X	X	0	0	1	0	—	—	1	—	—	—	—	—
X	X	X	0	0	0	0	—	—	—	1	—	—	—	—

3.3 Switch Functional Description

The NINJA C/CX (ADM6992C/CX) supports three types of data forwarding mode, store & forward mode, modified and MII cut-through.

3.3.1 Store & Forward Mode

The NINJA C/CX (ADM6992C/CX) allows switching between different speed media (e.g. 10BaseX and 100BaseX) in store & forward mode. The entire received frame will be stored into its packet buffer. The NINJA C/CX (ADM6992C/CX) checks the length and frame check sequence (FCS) of the received frame to prevent the forwarding of corrupted packets before forwarding to the destination port. A MAC address filtering process can be enabled to filter local traffic to improve overall network performance. The maximum packet length is up to 9216 bytes in this mode. The maximum packet length is defined in Bit [13:0] of EEPROM register 03_H.

3.3.2 Modified Cut-through Mode

The NINJA C/CX (ADM6992C/CX) begins to forward the received packet when it receives the first 64 bytes of the packet. The latency is about 512 bits time width. The NINJA C/CX (ADM6992C/CX) will not forward fragment packets. The MAC address learning & filtering should be disabled in this mode, because the received packets may be corrupted. The maximum packet length is up to 9216 bytes in this mode. The maximum packet length is defined in Bit [13:0] of EEPROM register 03_H.

3.3.3 MII cut-through Mode

The NINJA C/CX (ADM6992C/CX) begins to forward the received packet at the beginning of the received packet. It provides the minimum latency in this mode. The maximum packet length is 9216 bytes if the clock difference between MII receive clock and MII transmit clock is 200Ppm.

3.4 Basic Operations

3.4.1 MAC Address Learning & Filtering

The NINJA C/CX (ADM6992C/CX) adopts 4-way associative hash architecture to store the MAC address table. It can store up to a maximum 1K of MAC addresses.

In store & forward mode, the NINJA C/CX (ADM6992C/CX) receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address, and then forwards the packet to the other port, if appropriate. If the destination address is not found in the address table, the NINJA C/CX (ADM6992C/CX) treats the packet as a broadcast packet and forwards the packet to the other ports. If the destination port is the same with the port where the packet received from, the NINJA C/CX (ADM6992C/CX) treats the packet as a local traffic packet and discards it.

3.4.2 Address Learning

The NINJA C/CX (ADM6992C/CX) searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

1. The NINJA C/CX (ADM6992C/CX) automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed
2. If the SA was not found in the Address Table (a new address), the NINJA C/CX (ADM6992C/CX) waits until the end of the packet (non-error packet) and updates the Address Table
3. If the SA was found in the Address Table, then the aging value of each corresponding entry will be reset to 0
4. When the DA is in PAUSE mode, then the learning process will be disabled automatically by the NINJA C/CX (ADM6992C/CX)

3.4.3 Hash Algorithm

The NINJA C/CX (ADM6992C/CX) supports two types of hash algorithms for address learning & filtering. The first is the CRC-CCITT polynomial method. The 48 bits MAC address is reduced to a 16 bits CRC hash value. Bit [7:0] of the CRC are used to index the 1K address table. The CRC-CCITT polynomial is

$$X^{16} + X^{12} + X^5 + 1$$

The second is the direct-map method. The 48-bit MAC address is mapped into a 8 bits address spaced by XOR-method to index the 1K address table.

The hash type can be selected by using bit [15] of EEPROM register 03_H.

3.4.4 Address Recognition and Packet Forwarding

The address learning & filtering process forwards the incoming packets between bridged ports according to the Destination Address (DA) as below.

1. If the DA is a UNICAST address and the address was found in the Address Table, the NINJA C/CX (ADM6992C/CX) will check the port number and act as follows:
   a) If the port number is equal to the port on which the packet was received, the packet is discarded.
   b) If the port number is different from the port on which the packet was received, the packet is forwarded across the bridge.
2. If the DA is a UNICAST address and the address was not found, the NINJA C/CX (ADM6992C/CX) treats it as a multicast packet and forwards it across the bridge.
3. If the DA is a Multicast address, the packet is forwarded across the bridge.
4. If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by the NINJA C/CX (ADM6992C/CX). The NINJA C/CX (ADM6992C/CX) can issue and learn PAUSE commands.
5. The NINJA C/CX (ADM6992C/CX) will forward by default or filter out the packet with DA of (01-80-C2-00-00-00), discard the packet with DA of (01-80-C2-00-00-01), filter out the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F), and forward the packet with DA of (01-80-C2-00-00-10 ~ 01-80-C2-00-00-FF) decided by EEPROM Reg. $0E_H$.

3.4.5 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the NINJA C/CX (ADM6992C/CX) internally has 300 seconds timer, after which the address will be “aged out” (removed) from the address table. Aging function can enabled/disabled by the user. Normally, disabling the aging function is for security purposes.

3.4.6 Back off Algorithm

The NINJA C/CX (ADM6992C/CX) implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. The NINJA C/CX (ADM6992C/CX) will restart the back off algorithm by choosing 0-9 collision counts. The NINJA C/CX (ADM6992C/CX) resets the collision counter after 16 consecutive retransmitting trials.

3.4.7 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits time. The value is 9.6us for 10Mbps ETHERNET, 960ns for 100Mbps fast ETHERNET, and 96ns for 1000M. The NINJA C/CX (ADM6992C/CX) provides an option of 92 bit-time gaps in the EEPROM to prevent packet loss when Flow Control is turned off and the clock P.P.M. value differs.

3.4.8 Illegal Frames

In store & forward mode, the NINJA C/CX (ADM6992C/CX) will discard all illegal frames such as small packets (less than 64 bytes), oversized packets (greater than the value which is defined in Bit [13:0] of EEPROM register 03_H) and bad CRC. Dribbling packing with good CRC value will accept by NINJA C/CX (ADM6992C/CX).

In modified cut-through mode, the NINJA C/CX (ADM6992C/CX) will forward all received packets except for small packets (less than 64 bytes).

In MII cut-through mode, the NINJA C/CX (ADM6992C/CX) will forward all received packets.

3.4.9 Half Duplex Flow Control

A Back Pressure function is supported for half-duplex operation. When the NINJA C/CX (ADM6992C/CX) cannot allocate a received buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is disabled by DISBP which is set during RESETL assertion. A proprietary

algorithm is implemented inside the NINJA C/CX (ADM6992C/CX) to prevent the back pressure function causing HUB partition under a heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.4.10 Full Duplex Flow Control

When a full duplex port runs out of its received buffer space, a PAUSE packet command will be issued by the NINJA C/CX (ADM6992C/CX) to notify the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. The NINJA C/CX (ADM6992C/CX) can issue or receive pause packets.

3.4.11 Bandwidth Control

NINJA C/CX (ADM6992C/CX) supports hardware-based bandwidth control for both ingress and egress traffics. Ingress and egress rates can be limited independently on a per port base. The NINJA C/CX (ADM6992C/CX) uses 8ms at the scale, and the minimum bandwidth control unit is 4 kbit/s so users can configure the rate equal to K * 4 kbit/s, 1<=K<=25000. The NINJA C/CX (ADM6992C/CX) maintains two counters (input and output) for each port. For example, if users want to limit the rate to 64 kbit/s, they should configure the bandwidth control threshold to 16. For each time unit, the NINJA C/CX (ADM6992C/CX) will add 64 to the counter and decrease the byte length when receiving a packet during this period. When the counter is decreased to zero, we can divide the control behavior into two parts:

1. For the ingress control, the ingress port will not stop receiving packets. If flow control is enabled, Pause packets will be transmitted, if Back Pressure is enabled, Jam packets will be transmitted, and if the above functions are not enabled, the packet will be discarded.
2. For the egress control, the egress port will not transmit any packets. The port receiving packets that are forwarded to the egress port will transmit Pause packets if flow control is enabled, transmit Jam packets if Back Pressure is enabled, and discard packets if all the above functions are not enabled.

3.4.12 Interrupt

With the use of external CPU support, the NINJA C/CX (ADM6992C/CX) can issue an interrupt to the CPU if any event defined in SMI interrupt register 10_H and SMI interrupt mask register 11_H occurs.

3.4.13 Auto TP MDIX function

The normal application in which a Switch connects to a NIC card is by a one-to-one TP cable. If the Switch connects to other devices such as another Switch, it can be done by two ways. The first is to use a Cross Over TP cable and the second way is to use an extra RJ45 connector by internally crossing over the TXP/TXN and RXP/RXN signals. By using the second way, customers can use a one-to-one cable to connect two Switch devices. All these efforts add extra costs and are not a good solution. The NINJA C/CX (ADM6992C/CX) provides an Auto MDIX function, which adjusts the TXP/TXN and RXP/RXN automatically on the correct pins. Users can use one-to-one cabling between the NINJA C/CX (ADM6992C/CX) and other devices either switches or NICs.

3.5 Converter Functional Description

3.5.1 Fault Propagation

The NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter incorporates a Fault Propagation feature, which allows indirect sensing of a Fiber Link Loss via the 10/100Base-TX UTP connection. Whenever the NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter detects a Link Loss condition on the Received fiber (Fiber LNK OFF), it disables its UTP link pulse so that a Link Loss condition will be sensed on the UTP port to which the

NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter is connected. This link loss can then be sensed and reported by a Network Management agent in the remote UTP port's host equipment. This feature will affect the NINJA C/CX (NINJA C/CX (ADM6992C/CX)) UTP LNK LED.

The NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter also incorporates a Far End Fault feature, which allows the stations on both ends of a pair of fibers to be informed when there is a problem with one of the fibers. Without Far End Fault, it is impossible for a fiber interface to detect a problem that affects only its Transmitting fiber.

When Far End Fault is supported and enabled, a loss of received signal (link) will cause the transmitter to generate a Far End Fault pattern in order to inform the device at the far end of the fiber pair that a fault has occurred. Unless Fiber Link Loss occurs or if the UTP port link fails, the NINJA C/CX (NINJA C/CX (ADM6992C/CX)) Media Converter will also generate a Far End Fault pattern in order to inform the device at the far end of the fiber pair that a fault has occurred.

3.6 Serial Management Interface (SMI) Register Access

The SMI consists of two pins, management data clock (SDC) and management data input/output (SDIO). The NINJA C/CX (ADM6992C/CX) is designed to support an SDC frequency up to 25 MHz. The SDIO line is bi-directional and may be shared with other devices.

The SDIO pin requires a 1.5 K pull-up which, during idle and turnaround periods, will pull SDIO to a logic one state. NINJA C/CX (ADM6992C/CX) requires a single initialization sequence of 35 bits of preamble following power-up/hardware reset. The first 35 bits are preamble consisting of 35 contiguous logic one bits on SDIO and 35 corresponding cycles on SDC. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from management register operation, and <01> indicates write to management register operation. The next field is the management register address. It is 10 bits wide and the most significant bit is transferred first.

Table 11 SMI Read/Write Command Format

Operation	Preamble	SFD	OP	CHIPID[1:0]	Unused	Register Address	TA	Data
Read	35"1"s	01	10	2 bits CHIPID	00	6 bits Address	Z0	32 bits Data Read
Write	35"1"s	01	01	2 bits CHIPID	00	6 bits Address	10	32 bits Data Write

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the SDIO to avoid contention. Following the turnaround time, a 32-bit data stream is read from or written into the management registers of the NINJA C/CX (ADM6992C/CX).

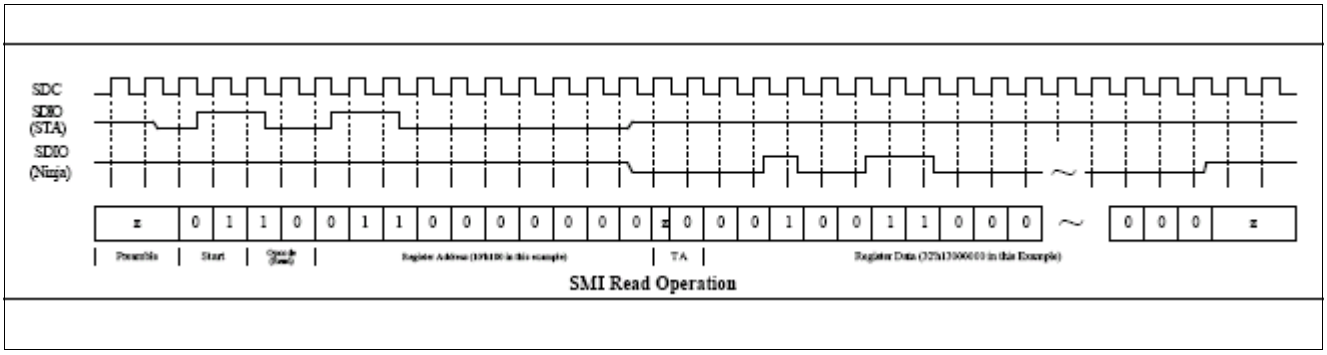


Figure 3 SMI Read Operation

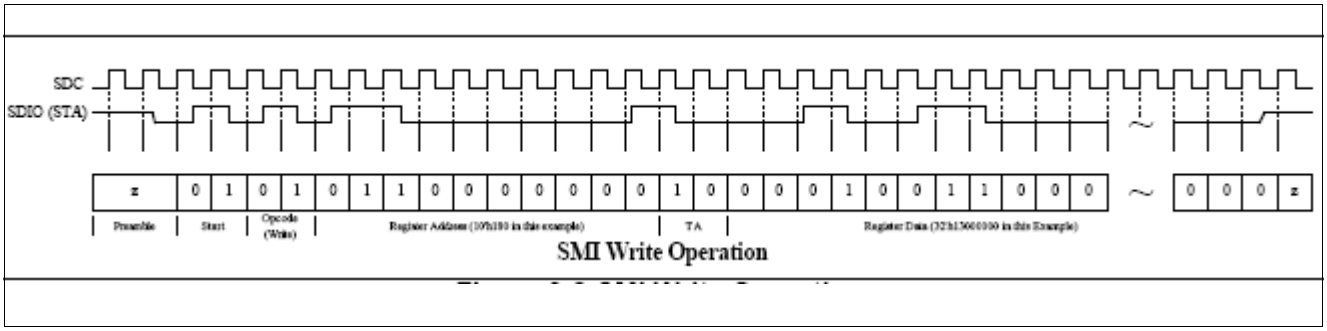


Figure 4 SMI Write Operation

3.6.1 Preamble Suppression

The SMI of NINJA C/CX (ADM6992C/CX) supports a preamble suppression mode. If the station management entity (i.e. MAC or other management controller) determines that all devices which are connected to the same SDC/SDIO in the system support preamble suppression, then the station management entity needs not to generate preamble for each management transaction. The NINJA C/CX (ADM6992C/CX) requires a single initialization sequence of 35 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of SDIO. While the NINJA C/CX (ADM6992C/CX) will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

When NINJA C/CX (ADM6992C/CX) detects that there is address match, then it will enable Read/Write capability for external access. When address is mismatched, then NINJA C/CX (ADM6992C/CX) will tristate the SDIO pin.

3.6.2 Read EEPROM Register via SMI Register

The following 2 steps are for reading the data of EEPROM Register via SMI Interface.

Write the address of the desired EEPROM Register and READ command to SMI Register 013_H

EX. <35”1”s><01><01><00000><10011><10><000 0000000 000001 0000000000000000>

CMD ADDRESS DATA

Read NINJA C/CX (ADM6992C/CX) Internal EEPROM mapping $Reg.1_H$. Read SMI Register 013_H. The data of desired EEPROM Register will be in bit [15:0].

EX. <35”1”s><01><10><00000><10011><z0><000 0000000 000000 0001000001001111>

CMD ADDRESS DATA

Get NINJA C/CX (ADM6992C/CX) Internal EEPROM mapping $Reg.1_H$. value 104f.

3.6.3 Write EEPROM Register via SMI Register

To write data into desired EEPROM Register, write the address of the EEPROM Register.

EX. <35”1”s><01><01><00000><00100><10><001 0000000 000001 0001000001000000>

CMD ADDRESS DATA

Write NINJA C/CX (ADM6992C/CX) Internal EEPROM mapping Reg.1_H. with value 820f.

3.7 Reset Operation

The NINJA C/CX (ADM6992C/CX) can be reset either by hardware or software. A hardware reset is accomplished by applying a negative pulse, with duration of at least 100 ms to the RC pin of the NINJA C/CX (ADM6992C/CX) during normal operation to guarantee internal SSRAM is reset properly.

Hardware reset operation samples the pins and initializes all registers to their default values. This process includes re-evaluation of all hardware configurable registers. A hardware reset affects all embedded PHYs in the device.

Software reset can reset all embedded PHY and it does not latch the external pins nor reset the registers to their respective default values. This can be achieved by writing FF to EEPROM Reg.$3F_H$.

Logic levels on several I/O pins are detected during a hardware reset to determine the initial functionality of NINJA C/CX (ADM6992C/CX). Some of these pins are used as output ports after reset operation.

Care must be taken to ensure that the configuration setup will not interfere with normal operations. Dedicated configuration pins can be tied to VCC or Ground directly. Configuration pins multiplexed with logic level output functions should be either weakly pulled up or weakly pulled down through external resistors.

3.7.1 Write EEPROM Register via EEPROM Interface

To write data into desired EEPROM Register via EEPROM interface.

If external EEPROM 93C46 or 93C66 exists, any WRITE programming instructions after EWEN instruction is executed can be updated effectively on EEPROM content and NINJA C/CX (ADM6992C/CX) internal mapping register on the same time.

If no external EEPROM exists, EECS/EECK/EEDI must be kept tristate at least 100ms after hardware reset. Any WRITE programming instructions after EWEN instruction is executed can be updated effectively on NINJA C/CX (ADM6992C/CX) internal mapping register. Please notice that NINJA C/CX (ADM6992C/CX) can only identify 93C66-programming instructions if no external EEPROM.

4 Registers Description

This chapter describes descriptions of EEPROM Registers and Serial Management Registers.

4.1 EEPROM Registers

Table 12 EEPROM Register Map

Register	Bit 15-8	Bit 7-0	Default Value
00_H	Signature		4154_H
01_H	Port 0 Configuration		$104F_H$
02_H	Port 1 Configuration		$104F_H$
03_H	Miscellaneous Configuration 0		0600_H
04_H	Miscellaneous Configuration 1		0000
05_H	Miscellaneous Configuration 2		0014_H
06_H	Buffer Management Configuration 0		0198_H
07_H	Buffer Management Configuration 1		0258_H
08_H	Buffer Management Configuration 2		0008_H
09_H	Bandwidth Control Configuration 0		0000_H
$0A_H$	Bandwidth Control Configuration 1		0000_H
$0B_H$	Bandwidth Control Configuration 2		0000_H
$0C_H$	Bandwidth Control Configuration 3		0000_H
$0D_H$	PHY Miscellaneous Configuration		$1A74_H$
$0E_H$	Reserved MAC Address Filtering Configuration		0014
$0F_H$	Filter Control Register 1	Filter Control Register 0	0000_H
10_H	Filter Control Register 3	Filter Control Register 2	0000_H
11_H	Filter Control Register 5	Filter Control Register 4	0000_H
12_H	Filter Control Register 7	Filter Control Register 6	0000_H
13_H	Filter Control Register 9	Filter Control Register 8	0000_H
14_H	Filter Control Register 11	Filter Control Register 10	0000_H
15_H	Filter Control Register 13	Filter Control Register 12	0000_H
16_H	Filter Control Register 15	Filter Control Register 14	0000_H
17_H	Filter Type Register 0		0000_H
18_H	Filter Type Register 1		0000_H
19_H	Filter Register 0		0000_H
$1A_H$	Filter Register 1		0000_H
$1B_H$	Filter Register 2		0000_H
$1C_H$	Filter Register 3		0000_H
$1D_H$	Filter Register 4		0000_H
$1E_H$	Filter Register 5		0000_H
$1F_H$	Filter Register 6		0000_H
20_H	Filter Register 7		0000_H
21_H	Filter Register 8		0000_H
22_H	Filter Register 9		0000_H

Table 12 EEPROM Register Map (cont'd)

Register	Bit 15-8	Bit 7-0	Default Value
23_H	Filter Register 10		0000_H
24_H	Filter Register 11		0000_H
25_H	Filter Register 12		0000_H
26_H	Filter Register 13		0000_H
27_H	Filter Register 14		0000_H
28_H	Filter Register 15		0000_H
29_H	PVID and PCID MASK of Port 0		00001
$2A_H$	PVID and PCID MASK of Port 0		0000_H
$2B_H$	PVID and PCID MASK of Port 1		00001
$2C_H$	PVID and PCID MASK of Port 1		$D000_H$
$2D_H$	Tag Rule 0		$F000_H$
$2E_H$	Tag Rule 0		$00FF_H$
$2F_H$	Tag Rule 1		$F000_H$
30_H	Tag Rule 1		$00FF_H$
31_H	Tag Rule 2		$F000_H$
32_H	Tag Rule 2		$00FF_H$
33_H	Tag Rule 3		$F000_H$
34_H	Tag Rule 2		$00FF_H$
35_H	OAM Configuration Register 1		0380_H
36_H	OAM Configuration Register 2		$FEFF_H$
37_H	Vender Code[15:0]		0000_H
38_H	Model Number[7:0]	Vender Code[23:16]	0000_H
39_H	Model Number[23:8]		0000_H
$3A_H$	Forwarding Configuration 1		6000_H
$3B_H$	Forwarding Configuration 2		0000_H
$3C_H$	Default Value Control Register		0000_H

4.2 EEPROM Register Descriptions

Table 13 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
EEPROM	00_H	$3C_H$	

Table 14 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SR	Signature Register	00_H	32
PCR_0	Port Configuration Register 0	01_H	33
PCR_1	Port Configuration Register 1	02_H	34
MC_0	Miscellaneous Configuration 0	03_H	35
MCR_1	Miscellaneous Configuration Register 1	04_H	35
MCR_2	Miscellaneous Configuration Register 2	05_H	37
BMC_0	Buffer Management Configuration 0	06_H	38
BMC_1	Buffer Management Configuration 1	07_H	38
BMC_2	Buffer Management Configuration 2	08_H	39
IBW_CCR_0	Ingress Bandwidth Control Configuration 0	09_H	39
EBW_CCR_1	Egress Bandwidth Control Configuration 1	$0A_H$	39
IBW_CCR_2	Ingress Bandwidth Control Configuration 2	$0B_H$	40
EBW_CCR_3	Egress Bandwidth Control Configuration 3	$0C_H$	40
PHY_MC	PHY Miscellaneous Configuration	$0D_H$	41
MAC_AFC	MAC Address Filtering Configuration	$0E_H$	42
PCFC_1_0	Packet Filter Control Register 1 and 0	$0F_H$	43
PCFC_3_2	Packet Filter Control Registers 3 and 2	10_H	43
PCFC_5_4	Packet Filter Control Registers 5 and 4	11_H	43
PCFC_7_6	Packet Filter Control Registers 7 and 6	12_H	43
PCFC_9_8	Packet Filter Control Registers 9 and 8	13_H	43
PCFC_11_10	Packet Filter Control Registers 11 and 10	14_H	43
PCFC_13_12	Packet Filter Control Registers 13 and 12	15_H	43
PCFC_15_14	Packet Filter Control Registers 15 and 14	16_H	43
TFTR_0	Filter Type Register 0	17_H	44
TFTR_1	Filter Type Register 1	18_H	44
FR_0	Filter Register 0	19_H	45
FR_1	Filter Register 1	$1A_H$	45
FR_2	Filter Register 2	$1B_H$	45
FR_3	Filter Register 3	$1C_H$	45
FR_4	Filter Register 4	$1D_H$	45
FR_5	Filter Register 5	$1E_H$	45
FR_6	Filter Register 6	$1F_H$	45
FR_7	Filter Register 7	20_H	45
FR_8	Filter Register 8	21_H	45

Table 14 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
FR_9	Filter Register 9	22_H	45
FR_10	Filter Register 10	23_H	45
FR_11	Filter Register 11	24_H	45
FR_12	Filter Register 12	25_H	45
FR_13	Filter Register 13	26_H	45
FR_14	Filter Register 14	27_H	45
FR_15	Filter Register 15	28_H	45
PB_ID_0_0	Port Base VLAN ID and Mask 0 of Port 0	29_H	46
PB_ID_1_0	Port Base VLAN ID and Mask 1 of Port 0	$2A_H$	46
PB_ID_0_1	Port Base VLAN ID and Mask 0 of Port 1	$2B_H$	47
PB_ID_1_1	Port Base VLAN ID and Mask 1 of Port 1	$2C_H$	47
TPR_0_0	Tag Port Rule 0 Register 0	$2D_H$	48
TPR_1_0	Tag Port Rule 1 Register 0	$2E_H$	48
TPR_0_1	Tag Port Rule 0 Register 1	$2F_H$	48
TPR_1_1	Tag Port Rule 1 Register 1	30_H	49
TPR_0_2	Tag Port Rule 0 Register 2	31_H	48
TPR_1_2	Tag Port Rule 1 Register 2	32_H	49
TPR_0_3	Tag Port Rule 0 Register 3	33_H	48
TPR_1x	Tag Port Rule 1 x	34_H	49
OAM_C_1	OAM Configuration Register 1	35_H	49
OAM_CR_2	OAM Configuration Register 2	36_H	51
MCR_3	Miscellaneous Configuration Register 3	37_H	51
MCR_4	Miscellaneous Configuration 4	38_H	52
MCR_5	Miscellaneous Configuration Register 5	39_H	52
FC_1	Forwarding Configuration 1	$3A_H$	53
FC_2	Forwarding Configuration 2	$3B_H$	53
DV_CR	Default Value Control Register	$3C_H$	54

The register is addressed wordwise.

Table 15 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register

Table 15 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Latch high, self clearing	lhsc	Latches high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latches high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latches high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latches high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiates the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiates the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

Table 16 Registers Clock Domains

Clock Short Name	Description

4.2.1 EEPROM Register Format

Signature Register

SR	Offset	Reset Value
Signature Register	00_H	4154_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Signature															
ro															

Field	Bits	Type	Description
Signature	15:0	ro	**Signature** 4154_H **SIG**, Default (AT)

Port Configuration Register 0

PCR_0 **Offset** **Reset Value**
Port Configuration Register 0 **01_H** **$104F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBC	PAC	RPT	OPTC	MAC					ANPD	AN	ANA	DX	SP	ANE	FC
rw	rw	rw	rw	rw					rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
LBC	15	rw	**Loop-back Control** 0_B **N**, Normal Operation (Default) 1_B **LP**, Local Loop-back for Port1/Port0
PAC	14	rw	**Packet Authorization Control** 0_B **ALL**, All packet (Default) 1_B **PPP**, PPPOE only
RPT	13	rw	**Receive Packet TAG Recognition Control** 0_B **REC**, Recognize VLAN TAG automatically (Default) 1_B **DIS**, Disable
OPTC	12	rw	**Output Packet Tagging Control** 0_B **TAG**, TAG/UNTAG packets if needed 1_B **BP**, Bypass TX packets same as RX (Default)
MAC	11:7	rw	**MAC Learning Table Entry Limitation** 0_B **DIS**, Disable Total MAC Limitation (Default) 1_B **MAX**, Maximum allowable total MAC
ANPD	6	rw	**Auto-Negotiation Parallel Detect Follow IEEE802.3** 0_B **B**, Both 1_B **H**, Half only (Default)
AN	5	rw	**Auto-Negotiation Advertise Single Capability** 0_B **E**, Expand (Default) 1_B **S**, Single
ANA	4	rw	**Auto-Negotiation Advertisement** 0_B **FS**, Follow speed and duplex setting to negotiate with link partner. (Default) 1_B **4W**, Always 4 way Auto-negotiation
DX	3	rw	**Duplex** 0_B **HD**, Half Duplex 1_B **FD**, Full Duplex (Default)

Field	Bits	Type	Description
SP	2	rw	**Speed** 0_B **10M**, 10M 1_B **100M**, 100M (Default)
ANE	1	rw	**Auto negotiation Enable** 0_B **D**, Disable Auto-negotiation 1_B **E**, Enable Auto-negotiation. (Default)
FC	0	rw	**802.3x Flow Control Command Ability** 0_B **D**, Disable 802.3x Flow control command ability 1_B **E**, Enable 802.3x Flow control command ability (Default)

Port Configuration Register 1

PCR_1	Offset	Reset Value
Port Configuration Register 1	02_H	$104F_H$

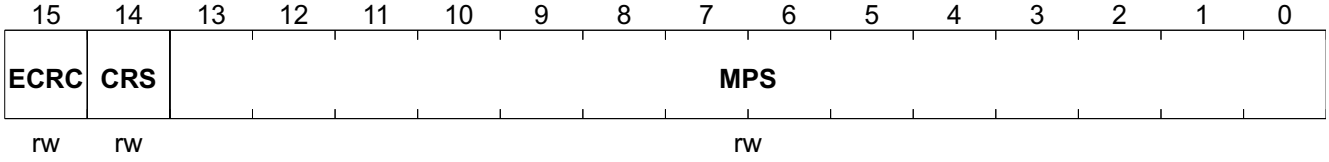
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBC	PAC	RPT	OPTC	MAC					ANPD	AN	ANA	DX	SP	ANE	FC
rw	rw	rw	rw	rw					rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
LBC	15	rw	**Loop-back Control** 0_B **N**, Normal Operation (Default) 1_B **LP**, Local Loop-back for Port1/Port0
PAC	14	rw	**Packet Authorization Control** 0_B **ALL**, All packet (Default) 1_B **PPP**, PPPOE only
RPT	13	rw	**Receive Packet TAG Recognition Control** 0_B **REC**, Recognize VLAN TAG automatically (Default) 1_B **DIS**, Disable
OPTC	12	rw	**Output Packet Tagging Control** 0_B **TAG**, TAG/UNTAG packets if needed 1_B **BP**, Bypass TX packets same as RX (Default)
MAC	11:7	rw	**MAC Learning Table Entry Limitation** 0_B **DIS**, Disable Total MAC Limitation (Default) 1_B **MAX**, Maximum allowable total MAC
ANPD	6	rw	**Auto-Negotiation Parallel Detect Follow IEEE802.3** 0_B **B**, Both 1_B **H**, Half only (Default)
AN	5	rw	**Auto-Negotiation Advertise Single Capability** 0_B **E**, Expand (Default) 1_B **S**, Single

Field	Bits	Type	Description
ANA	4	rw	**Auto-Negotiation Advertisement** 0_B **FS**, Follow speed and duplex setting to negotiate with link partner. (Default) 1_B **4W**, Always 4 way Auto-negotiation
DX	3	rw	**Duplex** 0_B **HD**, Half Duplex 1_B **FD**, Full Duplex (Default)
SP	2	rw	**Speed** 0_B **10M**, 10M 1_B **100M**, 100M (Default)
ANE	1	rw	**Auto negotiation Enable** 0_B **D**, Disable Auto-negotiation 1_B **E**, Enable Auto-negotiation. (Default)
FC	0	rw	**802.3x Flow Control Command Ability** 0_B **D**, Disable 802.3x Flow control command ability 1_B **E**, Enable 802.3x Flow control command ability (Default)

Miscellaneous Configuration 0

MC_0	Offset	Reset Value
Miscellaneous Configuration 0	**03_H**	**0600_H**



Field	Bits	Type	Description
ECRC	15	rw	**Enable CRC Check** 0_B **E**, Enable (Default) 1_B **D**, Disable
CRS	14	rw	**CRS (carrier sense) check disable** Checking of the length of CRS 0_B **ED**, Enable (Default) 1_B **DD**, Disable
MPS	13:0	rw	**Maximum Packet Size** Maximum allowable frame size in bytes 9216_D **MAX**, Max. bytes number 1536_D **DEF**, Default value

Miscellaneous Configuration Register 1

MCR_1 — **Offset** — **Reset Value**

Miscellaneous Configuration Register 1 — **04_H** — **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LED_ST	LED_ON	MAC	PFRC	Res	VLAN	EFM_P0	PL	DBO	DP	AD	Res				
rw	rw	rw	rw	ro	rw	rw	rw	rw	rw	rw	ro				

Field	Bits	Type	Description
LED_ST	15	rw	**LED Status Definition when UTP link down** 0_B **TBD**, always put off LEDs of UTP port when UTP link down (Default) 1_B **TBD**, LEDs of UTP port show DIPSW setting when auto-negotiation disabled and linked down
LED_ON	14	rw	**Turn on all LED** at the same time during LED self test 0_B **TBD**, Disable (Default) 1_B **TBD**, Enable
MAC	13	rw	**MAC address table hashing algorithm Control** 0_B **DM**, MAC address lookup table uses direct mode to generate hash key (Default) 1_B **CRC**, MAC address lookup table uses CRC to generate hash key
PFRC	12	rw	**Pause Frame Recognition Control** when auto-negotiation disabled 0_B **STOP**, Stop transmitting frame if PAUSE frame received. (Default) 1_B **NOS**, Don't stop transmitting frame if PAUSE frame received when flow control capability is disabled.
Res	11	ro	**Reserved** 0_B **DEF**, Default
VLAN	10	rw	**Replace VLAN ID 0 and 1 by PVID** 0_B **D**, Disable (Default) 1_B **R**, Replace
EFM_P0	9	rw	**Emulated Force Mode for Port0** 0_B **D**, Disable (Default) 1_B **TBD**,
PL	8	rw	**Preamble Leveling** 0_B **7B**, 7 bytes (Default) 1_B **6B**, 6 bytes
DBO	7	rw	**Disable Back-Off** 0_B **E**, Enable (Default) 1_B **D**, Disable
DP	6	rw	**Discard Packet after 16th Collision** 0_B **E**, Disable (Default) 1_B **D**, Enable

Field	Bits	Type	Description
AD	5	rw	**Aging Disable** 0_B **E**, Enable aging (Default) 1_B **D**, Disable aging
Res	4:0	ro	**Reserved**

Miscellaneous Configuration Register2

MCR_2	Offset	Reset Value
Miscellaneous Configuration Register 2	**05_H**	**0014_H**

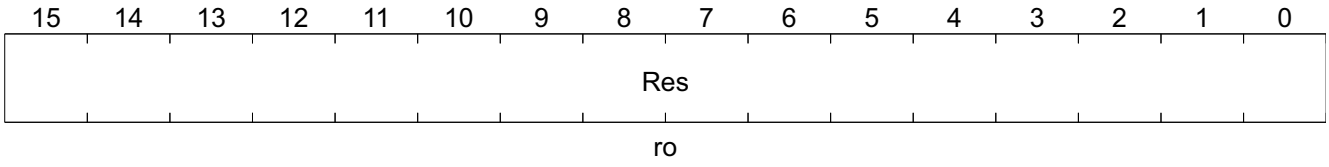
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD	**AG**	Res	**P0_MDI**	**XOVEN**	**FCDIS**	**RECHALF**	**REC10**	**ANDIS**	Res	Res		**FPC**	**Cut**	Res	Res
rw	rw	ro	rw	rw	rw	rw	rw	rw	ro	ro		rw	rw	ro	ro

Field	Bits	Type	Description
PD	15	rw	**Polarity definition** Change for hardware pin INT_N 0_B **LA**, INT_N Low Active (Default) 1_B **HA**, INT_N High Active
AG	14	rw	**Aging** 0_B **N**, Normal (Default) 1_B **F**, Fast
Res	13	ro	**Reserved**
P0_MDI	12	rw	**Polarity definition change for hardware pin P0_MDI** 0_B **DIP**, Disable Inverse Polarity of P0_MDI (Default) 1_B **IP**, Inverse Polarity of P0_MDI
XOVEN	11	rw	**Polarity definition change for hardware pin XOVEN** 0_B **DIP**, Disable Inverse Polarity of XOVEN (Default) 1_B **IP**, Inverse Polarity of XOVEN
FCDIS	10	rw	**Polarity definition change for hardware pin P0_FCDIS and P1_FCDIS** 0_B **DIP**, Disable Inverse Polarity (Default) 1_B **IP**, Inverse Polarity
RECHALF	9	rw	**Polarity definition change for hardware pin P0_RECHALF and P1_RECHALF** 0_B **DIP**, Disable Inverse Polarity (Default) 1_B **IP**, Inverse Polarity
REC10	8	rw	**Polarity definition change for hardware pin P0_REC10 and P1_REC10** 0_B **DIP**, Disable Inverse Polarity (Default) 1_B **IP**, Inverse Polarity

Field	Bits	Type	Description
ANDIS	7	rw	**Polarity definition change for hardware pin P0_ANDIS and P1_ANDIS** 0_B **DIP**, Disable Inverse Polarity (Default) 1_B **IP**, Inverse Polarity
Res	6	ro	**Reserved** 0_B **DEF**, Default
Res	5:4	ro	**Reserved**
FPC	3	rw	**Fault Propagation Control** 0_B **EP**, Enable Fault Propagation in converter mode (Default) 1_B **DP**, Disable Fault Propagation
Cut	2	rw	**Cut-Through Forwarding Control in converter mode** 0_B **ES**, Enable 100M snooping in converter mode 1_B **DS**, Disable snooping (Default)
Res	1	ro	**Reserved**
Res	0	ro	**Reserved**

Buffer Management Configuration 0

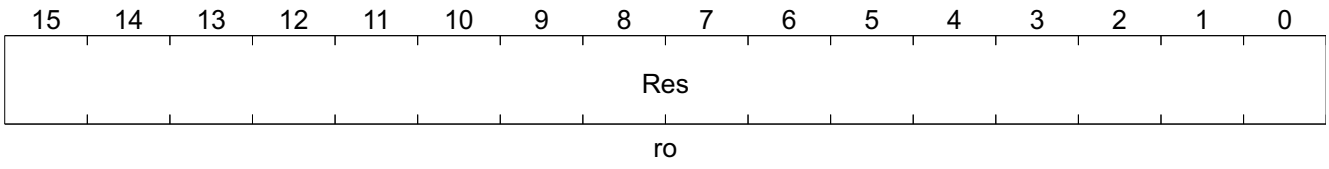
BMC_0 **Offset** **Reset Value**
Buffer Management Configuration 0 **06_H** **0198_H**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved** 0198_H **DEF**, Default

Buffer Management Configuration 1

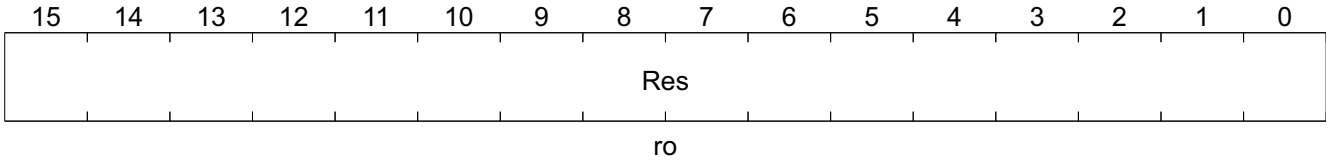
BMC_1 **Offset** **Reset Value**
Buffer Management Configuration 1 **07_H** **0258_H**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved** 0258_H **DEF**, Default

Buffer Management Configuration 2

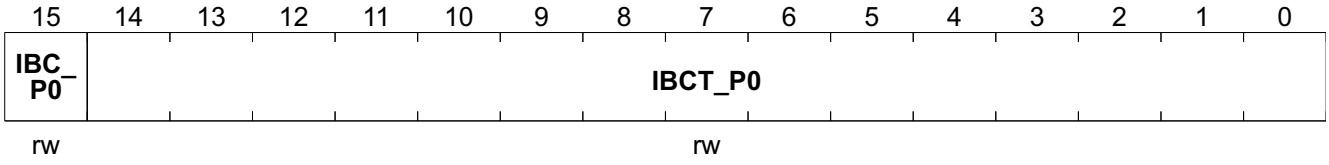
BMC_2 **Offset** **Reset Value**
Buffer Management Configuration 2 **08_H** **0008_H**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved** 0008_H **DEF**, Default

Ingress Bandwidth Control Configuration 0

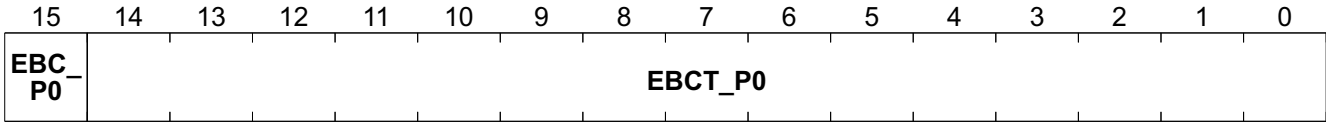
IBW_CCR_0 **Offset** **Reset Value**
Ingress Bandwidth Control Configuration 0 **09_H** **0000_H**



Field	Bits	Type	Description
IBC_P0	15	rw	**Port 0 Ingress Bandwidth Control** 0_B **D**, Disable (Default) 1_B **E**, Enable
IBCT_P0	14:0	rw	**Port0 Ingress Bandwidth Control Threshold** Step size: 4 Kbytes 0000_H **DEF**, Default

Egress Bandwidth Control Configuration 1

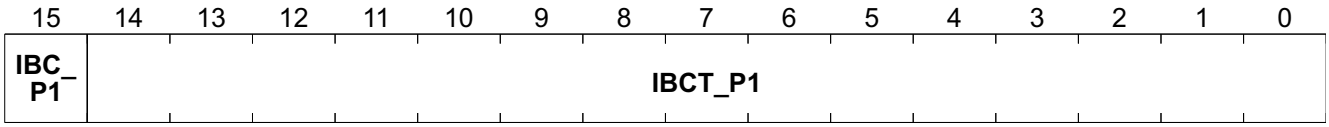
EBW_CCR_1 **Offset** **Reset Value**
Egress Bandwidth Control Configuration 1 **$0A_H$** **0000_H**



Field	Bits	Type	Description
EBC_P0	15	rw	**Port 0 Egress Bandwidth Control** 0_B **D**, Disable (Default) 1_B **E**, Enable
EBCT_P0	14:0	rw	**Port 0 Egress Bandwidth Control Threshold** Step size: 4 Kbytes 0000_H **Z**, Default

Ingress Bandwidth Control Configuration 2

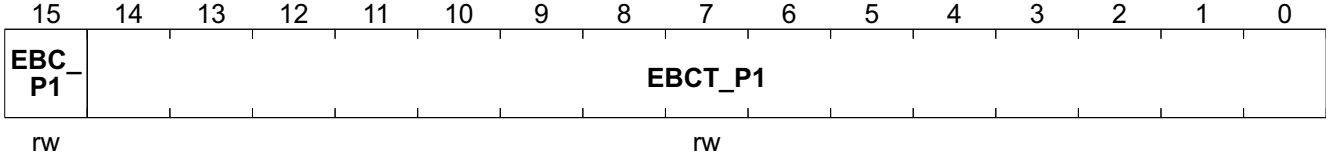
IBW_CCR_2 **Offset** **Reset Value**
Ingress Bandwidth Control Configuration 2 **$0B_H$** **0000_H**



Field	Bits	Type	Description
IBC_P1	15	rw	**Port 1 Ingress Bandwidth Control** 0_B **D**, Disable (Default) 1_B **E**, Enable
IBCT_P1	14:0	rw	**Port 1 Ingress Bandwidth Control Threshold** Step size: 4 Kbytes 0000_H **Z**, Default

Egress Bandwidth Control Configuration 3

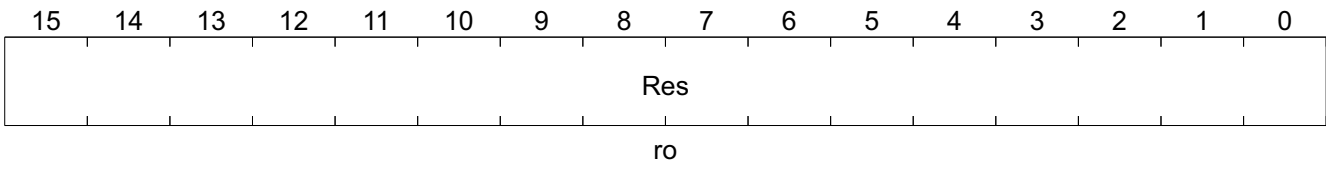
EBW_CCR_3 **Offset** **Reset Value**
Egress Bandwidth Control Configuration 3 **$0C_H$** **0000_H**



Field	Bits	Type	Description
EBC_P1	15	rw	**Port 1 Egress Bandwidth Control** 0_B **D**, Disable (Default) 1_B **E**, Enable
EBCT_P1	14:0	rw	**Port 1 Egress Bandwidth Control Threshold** Step size: 4 Kbytes 0000_H **Z**, Default

PHY Miscellaneous Configuration

PHY_MC	Offset	Reset Value
PHY Miscellaneous Configuration	**$0D_H$**	**$1A74_H$**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved** $1A74_H$ **CONF**, Default

Reserved MAC Address Filtering Configuration

MAC_AFC	Offset	Reset Value
MAC Address Filtering Configuration	$0E_H$	0014_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFM		**TUFM**		Res	**CRC**	Res		**PFM_10**		**PFM_02**		**PFM_01**		**PFM_00**	
rw		rw		ro	ro	ro		rw		ro		rw		rw	

Field	Bits	Type	Description
MFM	15:14	rw	**Match Frame Mode** 00_B **SAM**, CRC is correct and the same with CRC of last requested transmitted user frame (Default) 01_B **COR**, CRC is correct 10_B **DIF**, CRC is incorrect or different with CRC of last requested transmitted user frame 11_B **INC**, CRC is incorrect
TUFM	13:12	rw	**Transmit user frame mode** 00_B **SF**, Single frame (Default) 01_B **CMF**, Continuous transmit until match frame found or match timer expired $1x_B$ **CT**, Continuous transmit
Res	11	ro	**Reserved** 0_B **DEF**, Default
CRC	10	ro	**Disable OAM CRC check** 0_B **E**, Enable (Default) 1_B **D**, Disable
Res	9:8	ro	**Reserved** 00_B **DEF**, Default
PFM_10	7:6	rw	**Packet Filtering Mode for Received DA** = 01 80 C2 00 00 10 ~ 01 80 C2 00 00 FF 0_B **DEF**, Default
PFM_02	5:4	ro	**Packet Filtering Mode for Received DA** = 01 80 C2 00 00 02 ~ 01 80 C2 00 00 0F 1_B **DEF**, Default
PFM_01	3:2	rw	**Packet Filtering Mode for Received DA** = 01 80 C2 00 00 01 and OPCODE != PAUSE 01_B **DEF**, Default (Fixed)
PFM_00	1:0	rw	**Packet Filtering Mode for Received DA** = 01 80 C2 00 00 00 00_B **DEF**, Default

Packet Filter Control Registers 1 and 0

PCFC_1_0	Offset	Reset Value
Packet Filter Control Register 1 and 0	$0F_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	AP1_R1	AP0_R1	OPC_1A					Res	AP1_R1	AP1_R1	OPC_19				
ro	ro	ro	ro					ro	rw	rw	rw				

Field	Bits	Type	Description
Res	15	ro	**Reserved**
AP1_R1	14	ro	**Apply to Port 1 Rx 1** 0_B **DNA**, Do not apply 1_B **APL**, Apply
AP0_R1	13	ro	**Apply to Port 0 Rx 1** 0_B **DNA**, Do not apply 1_B **APL**, Apply
OPC_1A	12:8	ro	**OP Code for Filter** Defined in Register $1A_H$ ($1C_H$, $1E_H$, 20_H, 22_H, 24_H, 26_H, 28_H)
Res	7	ro	**Reserved**
AP1_R1	6	rw	**Apply to Port 1 Rx 1** 0_B **DNA**, Do not apply 1_B **APL**, Apply
AP1_R1	5	rw	**Apply to Port 0 Rx 1** 0_B **DNA**, Do not apply 1_B **APL**, Apply
OPC_19	4:0	rw	**OP Code for Filter** which defined in Register 19_H ($1B_H$, $1D_H$, $1F_H$, 21_H, 23_H, 25_H, 27_H)

Other Packet Filter Control Registers have the same structure and characteristics as **Packet Filter Control Registers 1 and 0**; the offset addresses are listed in **Table 17**.

Table 17 Other Packet Filter Control Regsiters

Register Short Name	Register Long Name	Offset Address	Page Number
PCFC_3_2	Packet Filter Control Registers 3 and 2	10_H	
PCFC_5_4	Packet Filter Control Registers 5 and 4	11_H	
PCFC_7_6	Packet Filter Control Registers 7 and 6	12_H	
PCFC_9_8	Packet Filter Control Registers 9 and 8	13_H	
PCFC_11_10	Packet Filter Control Registers 11 and 10	14_H	
PCFC_13_12	Packet Filter Control Registers 13 and 12	15_H	
PCFC_15_14	Packet Filter Control Registers 15 and 14	16_H	

Filter Type Register 0

TFTR_0 — **Filter Type Register 0**

Offset 17_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TF_7_15		TF_6_14		TF_5_13		TF_4_12		TF_3_11		TF_2_10		TF_1_9		TF_0_8	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
TF_7_15	15:14	rw	**Type of Filter 7**
TF_6_14	13:12	rw	**Type of Filter 6**
TF_5_13	11:10	rw	**Type of Filter 5**
TF_4_12	9:8	rw	**Type of Filter 4**
TF_3_11	7:6	rw	**Type of Filter 3**
TF_2_10	5:4	rw	**Type of Filter 2**
TF_1_9	3:2	rw	**Type of Filter 1**
TF_0_8	1:0	rw	**Type of Filter 0**

Filter Type Register 1

TFTR_1 — **Filter Type Register 1**

Offset 18_H

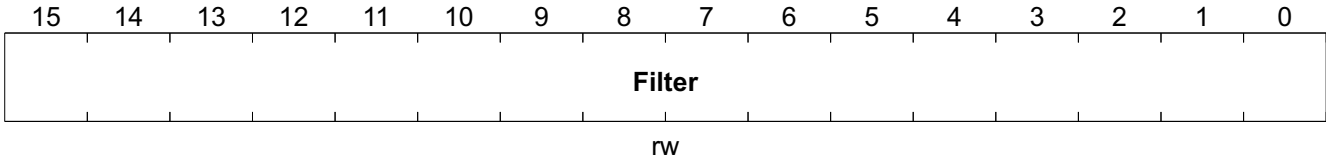
Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TF_7_15		TF_6_14		TF_5_13		TF_4_12		TF_3_11		TF_2_10		TF_1_9		TF_0_8	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
TF_7_15	15:14	rw	**Type of Filter 15**
TF_6_14	13:12	rw	**Type of Filter 14**
TF_5_13	11:10	rw	**Type of Filter 13**
TF_4_12	9:8	rw	**Type of Filter 12**
TF_3_11	7:6	rw	**Type of Filter 11**
TF_2_10	5:4	rw	**Type of Filter 10**
TF_1_9	3:2	rw	**Type of Filter 9**
TF_0_8	1:0	rw	**Type of Filter 8**

Filter Register 0

FR_0	Offset	Reset Value
Filter Register 0	19_H	0000_H



Field	Bits	Type	Description
Filter	15:0	rw	**Filter**

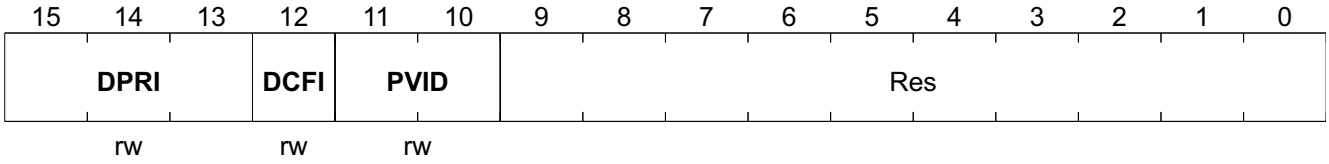
Other Filter Registers have the same structure and characteristics as **Filter Register 0**; the offset addresses are listed in **Table 18**.

Table 18 Other Filter Regsiters

Register Short Name	Register Long Name	Offset Address	Page Number
FR_1	Filter Register 1	$1A_H$	
FR_2	Filter Register 2	$1B_H$	
FR_3	Filter Register 3	$1C_H$	
FR_4	Filter Register 4	$1D_H$	
FR_5	Filter Register 5	$1E_H$	
FR_6	Filter Register 6	$1F_H$	
FR_7	Filter Register 7	20_H	
FR_8	Filter Register 8	21_H	
FR_9	Filter Register 9	22_H	
FR_10	Filter Register 10	23_H	
FR_11	Filter Register 11	24_H	
FR_12	Filter Register 12	25_H	
FR_13	Filter Register 13	26_H	
FR_14	Filter Register 14	27_H	
FR_15	Filter Register 15	28_H	

Port Base VLAN ID and Mask 0 of Port 0

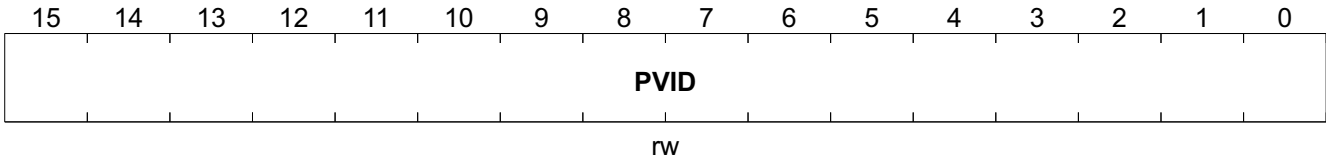
PB_ID_0_0	Offset	Reset Value
Port Base VLAN ID and Mask 0 of Port 0	**29_H**	**0001_H**



Field	Bits	Type	Description
DPRI	15:13	rw	**DPRI** Default Priority
DCFI	12	rw	**DCFI** Default CFI
PVID	11:10	rw	**PVID** Port base VLAN ID 01_B **DEF**, Default

Port Base VLAN ID and Mask 0 of Port 1

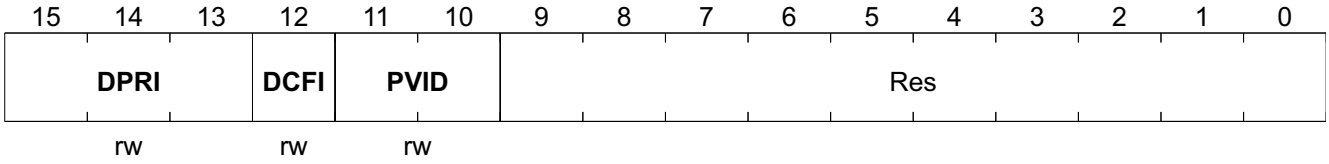
PB_ID_1_0	Offset	Reset Value
Port Base VLAN ID and Mask 1 of Port 0	**$2A_H$**	**0000_H**



Field	Bits	Type	Description
PVID	15:0	rw	**PVID Mask**

Port Base VLAN ID and Mask 0 of Port 1

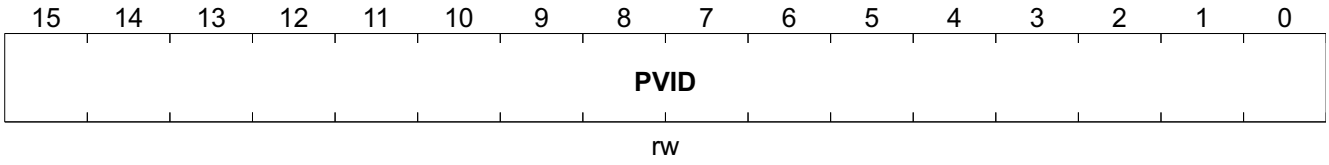
PB_ID_0_1	Offset	Reset Value
Port Base VLAN ID and Mask 0 of Port 1	**$2B_H$**	**0001_H**



Field	Bits	Type	Description
DPRI	15:13	rw	**DPRI** Default Priority
DCFI	12	rw	**DCFI** Default CFI
PVID	11:10	rw	**PVID** Port base VLAN ID 01_B **DEF**, Default

Port Base VLAN ID and Mask 1 of Port 1

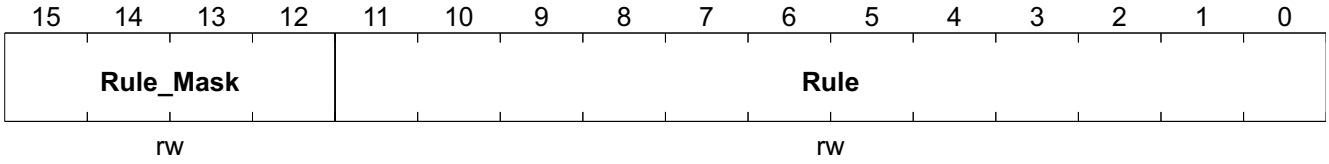
PB_ID_1_1	Offset	Reset Value
Port Base VLAN ID and Mask 1 of Port 1	**$2C_H$**	**0000_H**



Field	Bits	Type	Description
PVID	15:0	rw	**PVID Mask**

Tag Port Rule 0 Register 0

TPR_0_0	Offset	Reset Value
Tag Port Rule 0 Register 0	**$2D_H$**	**$F000_H$**



Field	Bits	Type	Description
Rule_Mask	15:12	rw	**Rule Mask** F_H **D**, Default
Rule	11:0	rw	**Rule**

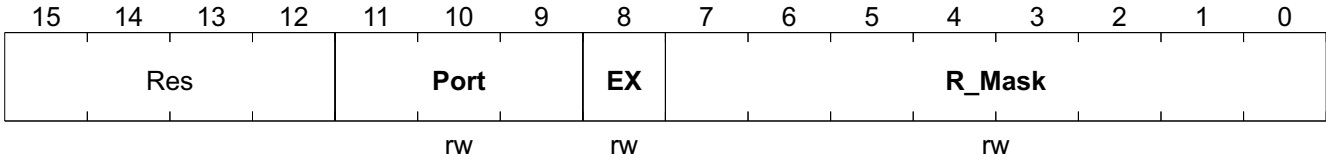
Other Tag Port Rule 0 Registers have the same structure and characteristics as **Tag Port Rule 0 Register 0**; the offset addresses are listed in **Table 19**.

Table 19 Other Tag Port Rule 0 Registers

Register Short Name	Register Long Name	Offset Address	Page Number
TPR_0_1	Tag Port Rule 0 Register 1	$2F_H$	
TPR_0_2	Tag Port Rule 0 Register 2	31_H	
TPR_0_3	Tag Port Rule 0 Register 3	33_H	

Tag Port Rule 1 Register 0

TPR_1_0	Offset	Reset Value
Tag Port Rule 1 Register 0	**$2E_H$**	**$00FF_H$**



Field	Bits	Type	Description
Port	11:9	rw	**Port to apply the rule**
EX	8	rw	**Exclude Rule**
R_Mask	7:0	rw	**Rule Mask[11:4]**

Other Tag Port Rule 1 Registers have the same structure and characteristics as **Tag Port Rule 1 Register 0**; the offset addresses are listed in **Table 20**.

Table 20 Other Tag Port Rule 1 Regsiters

Register Short Name	Register Long Name	Offset Address	Page Number
TPR_1_1	Tag Port Rule 1 Register 1	30_H	
TPR_1_2	Tag Port Rule 1 Register 2	32_H	

Tag Port Rule 1 x

TPR_1x	Offset	Reset Value
Tag Port Rule 1 x	34_H	$00FF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBTM	Timer			Port			ER	Rule_Mask							
rw	rw			rw			rw	rw							

Field	Bits	Type	Description
LBTM	15	rw	**Loop Back Test Mode** 0_B **TBD**, depends on current speed configuration to test 10M or 100M PHY (Default) 1_B **TBD**, Always test 100M PHY
Timer	14:12	rw	**Timer** Timer to qualify power failure recovery status (second) 000_B~111_B, 0~8 seconds 000_B , 0 seconds (Default)
Port	11:9	rw	**Port to apply the rule**
ER	8	rw	**Exclude Rule**
Rule_Mask	7:0	rw	**Rule Mask[11:4]**

OAM Configuration Register 1

OAM_C_1	Offset	Reset Value
OAM Configuration Register 1	35_H	0380_H

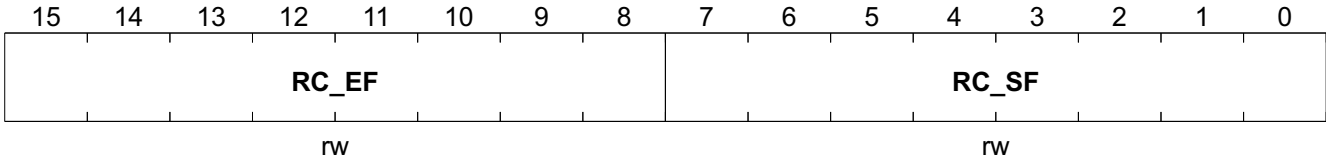
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_Def				TS_C	PRMT			DC	RCSO	RCSF	U_LU	U_LD	TXF	SNFC	MC
rw				rw	rw			rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TS_Def	15:12	rw	**TS-1000 OAM C field Bit[4:7] Definition for Remote Control** 0000_B **Z**, Default
TS_C	11	rw	**TS-1000 OAM C field Bit[1] Check** 0_B **CD**, Check direction of OAM frame (Default) 1_B **NC**, Do not check direction of OAM frame
PRMT	10:8	rw	**NINJA C/CX (ADM6992C/CX) Power Recovery Mask Timer when Power-On-Initial** Timer for Mask OAM after power up and Port 1 link up (second) 000_B~111_B, 0~8 seconds 011_B , 3 seconds (Default)
DC	7	rw	**NINJA C/CX (ADM6992C/CX) Power Detection Control** 0_B **Z**, Should be set 1_B **TBD**,
RCSO	6	rw	**NINJA C/CX (ADM6992C/CX) OAM Remote Control Stop OAM Enable** 0_B **E**, Enable Remote Control OAM (Default) 1_B **D**, Disable Remote Control OAM
RCSF	5	rw	**NINJA C/CX (ADM6992C/CX) OAM Remote Control Start Function Enable** 0_B **D**, Disable Remote Control (Default) 1_B **E**, Enable Remote Control
U_LU	4	rw	**TS-1000 OAM S field Bit[7:10]** Definition when UTP link up 0_B **SHOW**, S7-S8 and S9 of OAM frame show PHY status if PHY link up (Default) 1_B **NOT**, S7-S8 and S9 of OAM frame don't show PHY status if PHY link up
U_LD	3	rw	**TS-1000 OAM S field Bit[7:10]** Definition when auto-negotiation enable and UTP link down 0_B **DIS**, Disable idiot setting. NINJA C/CX (ADM6992C/CX) will send DIPSW setting to CO when UTP port auto-negotiation enable and link down (Default) 1_B **EIS**, Enable idiot setting. NINJA C/CX (ADM6992C/CX) will always send 10MH to CO when UTP port auto-negotiation enable and link down
TXF	2	rw	**Transmit MC_FAILURE when load EEPROM fail** 0_B **TBD**, Assert MC_FAILURE when load EEPROM fail (Default) 1_B **TBD**, Don't assert MC_FAILURE when load EEPOM fail
SNFC	1	rw	**NTT TS-1000 Status Notification Frame Control** 0_B **TBD**, Transmit one OAM frame if state changes or state notification request frame is received. (Default) 1_B **TBD**, Transmit three OAM frames if state changes or state notification request frame is received.
MC	0	rw	**NTT TS-1000 MC Mode Control** 0_B **TBD**, CPE mode (Default) 1_B **TBD**, CO mode

OAM Configuration Register 2

NINJA C/CX (ADM6992C/CX) OAM C field Bit[8:15] definition for Remote Control

OAM_CR_2	Offset	Reset Value
OAM Configuration Register 2	36_H	$FEFF_H$

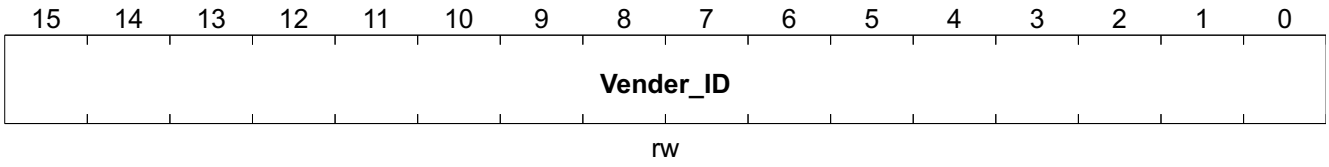


Field	Bits	Type	Description
RC_EF	15:8	rw	**Remote Control End Function** OAM C field Bit[8:15] definition FE_H **EF**, Default
RC_SF	7:0	rw	**Remote Control Start Function** OAM C field Bit[8:15] definition FF_H **SF**, Default

Miscellaneous Configuration Register 3

Vender ID

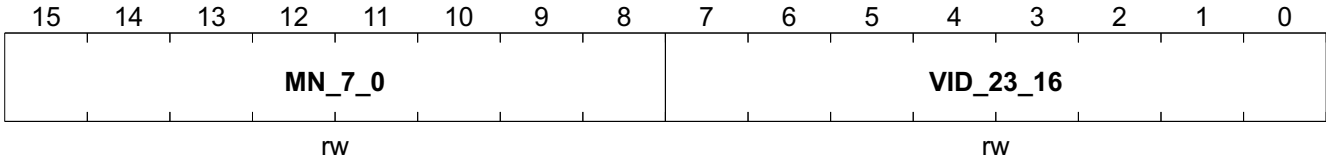
MCR_3	Offset	Reset Value
Miscellaneous Configuration Register 3	37_H	0000_H



Field	Bits	Type	Description
Vender_ID	15:0	rw	**NTT TS-1000 OAM M field Bit[15:0] definition** Vender ID Bits

Miscellaneous Configuration Register 4

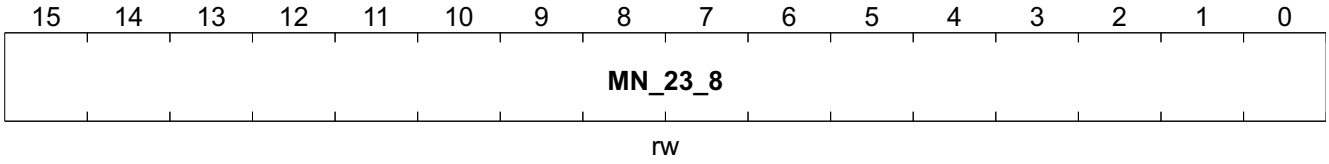
MCR_4	Offset	Reset Value
Miscellaneous Configuration 4	38_H	0000_H



Field	Bits	Type	Description
MN_7_0	15:8	rw	**NTT TS-1000 OAM M field Bit[31:24] definition** Model Number Bit [7:0]
VID_23_16	7:0	rw	**NTT TS-1000 OAM M field Bit[23:16] definition** Vender ID Bit [23:16]

Miscellaneous Configuration Register 5

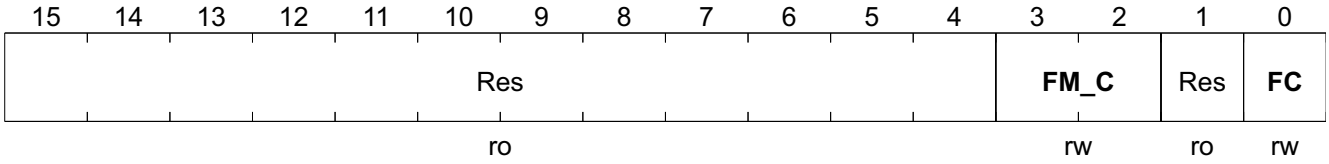
MCR_5	Offset	Reset Value
Miscellaneous Configuration Register 5	39_H	0000_H



Field	Bits	Type	Description
MN_23_8	15:0	rw	**NTT TS-1000 OAM M field Bit[47:32] definition** Model Number Bits [23:8]

Forwarding Configuration 1

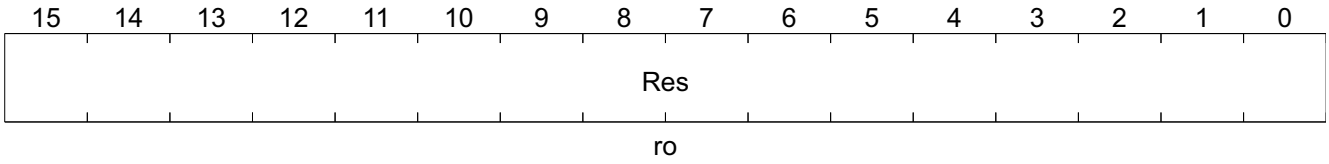
FC_1	Offset	Reset Value
Forwarding Configuration 1	**$3A_H$**	**6000_H**



Field	Bits	Type	Description
Res	15:4	ro	**Reserved** 600_H **D**, Default
FM_C	3:2	rw	**Forwarding Mode Control** 00_B **SF**, Store & Forward (Default) 01_B **MCT**, Modify Cut-Through 10_B **R**, Reserved 11_B **MII**, MII Cut-Through
Res	1	ro	**Reserved** 0_B , Default
FC	0	rw	**Forwarding Mode auto-change Control** 0_B **FIX**, Fix Forwarding Mode (Default) 1_B **A**, Automatically Change Forwarding Mode

Forwarding Configuration 2

FC_2	Offset	Reset Value
Forwarding Configuration 2	**$3B_H$**	**0000_H**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved** 0000_H **Z**, Default

Default Value Control Register

DV_CR	Offset	Reset Value
Default Value Control Register	$3C_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PU_M	PS_D	PS_C	PM_T	IPG	IP_D	IP_F	BP	EO	DL	FX1	FX_0	LED_2	LED_1	LED_0	DIS
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PU_M	15	rw	**Power up mask mode** 0_B **TBD**, by timer defined in EEPROM register 35_H Bit[10:8] (Default) 1_B **TBD**, by LED self test
PS_D	14	rw	**Power status detect mode** 0_B **TBD**, mode 0 (Default) 1_B **TBD**, mode 1
PS_C	13	rw	**Power status change mask timer** 0_B **TBD**, the same with power up mask timer which defined in EEPROM register 35_H Bit[10:8] (Default) 1_B **TBD**, EEPROM register 34_H Bit [14:12]
PM_T	12	rw	**Power mask timer time base before first OAM was sent** 0_B **TBD**, 1 sec. (Default) 1_B **TBD**, 0.5 sec.
IPG	11	rw	**Place IPG** 0_B **TBD**, Place IPG before and after OAM frame and loop back test frame (Default) 1_B **TBD**, Place IPG/2 before and after OAM frame and loop back test frame
IP_D	10	rw	**Inverse Polarity of A_PD_DETECT** 0_B **TBD**, Disable inverse the polarity (Default) 1_B **TBD**, Inverse the polarity
IP_F	9	rw	**Inverse Polarity of MC_FAILURE** 0_B **TBD**, Disable inverse the polarity (Default) 1_B **TBD**, Inverse the polarity
BP	8	rw	**Polarity definition change for power-on-setting pin BYPASS_PAUSE** 0_B **TBD**, Disable inverse the default value (Default) 1_B **TBD**, Inverse the default value
EO	7	rw	**Polarity definition change for power-on-setting pin EN_OAM** 0_B **TBD**, Disable inverse the default value (Default) 1_B **TBD**, Inverse the default value
DL	6	rw	**Polarity definition change for power-on-setting pin DIS_LEARN** 0_B **TBD**, Disable inverse the default value of DIS_LEARN (Default) 1_B **TBD**, Inverse the default value of DIS_LEARN

Field	Bits	Type	Description
FX1	5	rw	**Polarity definition change for power-on-setting pin FXMODE[1]** 0_B **TBD**, Disable inverse the default value (Default) 1_B **TBD**, Inverse the default value
FX_0	4	rw	**Polarity definition change for power-on-setting pin FXMODE[0]** 0_B **TBD**, Disable inverse the default value (Default) 1_B **TBD**, Inverse the default value
LED_2	3	rw	**Polarity definition change for power-on-setting pin LEDMODE[2]** 0_B **TBD**, Disable inverse the default value (Default) 1_B **TBD**, Inverse the default value
LED_1	2	rw	**Polarity definition change for power-on-setting pin LEDMODE[1]** 0_B **TBD**, Disable inverse the default value (Default) 1_B **TBD**, Inverse the default value
LED_0	1	rw	**Polarity definition change for power-on-setting pin LEDMODE[0]** 0_B **TBD**, Disable inverse the default value (Default) 1_B **TBD**, Inverse the default value
DIS	0	rw	**Polarity definition change for power-on-setting pin DISBP_N** 0_B **TBD**, Disable inverse the default value (Default) 1_B **TBD**, Inverse the default value

4.3 Serial Management Registers

Table 21 Serial Management Register Map

Register	Bit 31-0	Default Value
00_H	Chip Identify	$0002\ 1090_H$
01_H	Over Flow Flag	$0000\ 0000_H$
02_H	P0 Receive packets	$0000\ 0000_H$
03_H	P0 Receive byte count	$0000\ 0000_H$
04_H	P0 Transmit packets	$0000\ 0000_H$
05_H	P0 Transmit byte count	$0000\ 0000_H$
06_H	P0 error count	$0000\ 0000_H$
07_H	P0 collision count	$0000\ 0000_H$
08_H	P1 Receive packets	$0000\ 0000_H$
09_H	P1 Receive byte count	$0000\ 0000_H$
$0A_H$	P1 Transmit packets	$0000\ 0000_H$
$0B_H$	P1 Transmit byte count	$0000\ 0000_H$
$0C_H$	P1 error count	$0000\ 0000_H$
$0D_H$	P1 collision count	$0000\ 0000_H$
$0E_H$	Per Port Counter Reset	$0000\ 0000_H$
$0F_H$	Hardware Settings	Pin
10_H	Interrupt Register	$0000\ 0000_H$
11_H	Interrupt mask Register	$0000\ 0000_H$
12_H	Port Status	Real Time Status
13_H	EEPROM Register File Access Control	$0000\ 4154_H$

Table 21 Serial Management Register Map (cont'd)

Register	Bit 31-0	Default Value
14_H	OAM Control Register	$0000\ 0000_H$
15_H	Source Address of Loop Back Test User Frame 0	$0000\ 0000_H$
16_H	Source Address of Loop Back Test User Frame 1	$0000\ 0000_H$
17_H	Transmit OAM Frame Register 0	$0000\ 0000_H$
18_H	Transmit OAM Frame Register 1	$0000\ 0000_H$
19_H	Transmit OAM Frame Register 2	$0000\ 0000_H$
$1A_H$	Received OAM Frame Register 0	$0000\ 0000_H$
$1B_H$	Received OAM Frame Register 1	$0000\ 0000_H$
$1C_H$	Received OAM Frame Register 2	$0000\ 0000_H$
$1D_H$	OAM Frame Status Register	$0000\ 0000_H$

4.4 Serial Management Register Descriptions

Table 22 Registers Address Space

Module	Base Address	End Address	Note
Serial	00_H	$1D_H$	

Table 23 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Chip_ID	Chip Identifier	00_H	58
OFR	Overflow Flag Register	01_H	59
PCNR_0	Port 0 Counter Register	02_H	60
P0RBC	P0 Receive byte count	03_H	60
P0TP	P0 Transmit packets	04_H	60
P0TBC	P0 Transmit byte count	05_H	60
P0EC	P0 Error count	06_H	60
P0CC	P0 Collision count	07_H	60
P1RP	P1 Receive packets	08_H	60
P1RBC	P1 Receive byte count	09_H	60
P1TP	P1 Transmit packets	$0A_H$	60
P1TBC	P1 Transmit byte count	$0B_H$	60
P1EC	P1 Error count	$0C_H$	60
P1CC	P1 Collision count	$0D_H$	60
PCRR	Port Counter Reset Register	$0E_H$	60
HW_SSR	Hardware Setting Status Register	$0F_H$	62
INT	Interrupt Register	10_H	63
INT_M	Interrupt Mask Register	11_H	64
PSR	Port Status Register	12_H	66
EE_RFAC	EEPROM Register File Access Control	13_H	67
OAM_CR	OAM Control Register	14_H	68
SA_F_0	Source Address of Loop Back Test User Frame 0	15_H	69
SA_F_1	Source Address of Loop Back Test User Frame 1	16_H	70
TFR_0	Transmit OAM Frame Register 0	17_H	70
TFR_1	Transmit OAM Frame Register 1	18_H	70
TFR_2	Transmit OAM Frame Register 2	19_H	71
RFR_0	Received OAM Frame Register 0	$1A_H$	72
RFR_1	Received OAM Frame Register 1	$1B_H$	72
RFR_2	Received OAM Frame Register 0	$1C_H$	73
OAM_FSR	OAM Frame Status Register	$1D_H$	73

The register is addressed wordwise.

Table 24 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latches high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latches high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latches high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latches high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiates the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

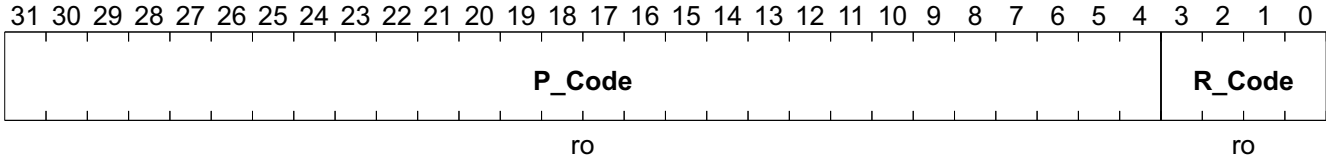
Table 25 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.4.1 Serail Management Register Format

Chip Identifier

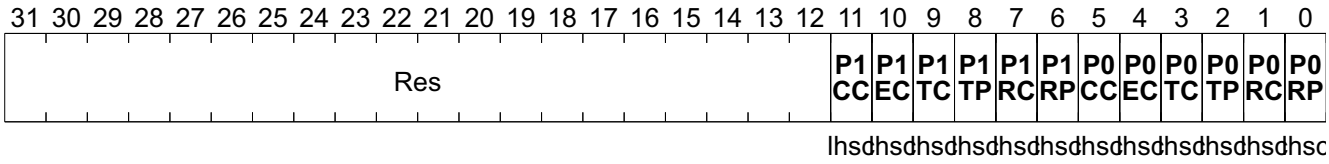
Chip_ID	Offset	Reset Value
Chip Identifier	**00_H**	**$0002\ 1090_H$**



Field	Bits	Type	Description
P_Code	31:4	ro	**Project Code**
R_Code	3:0	ro	**Revision Code**

Overflow Flag Register

OFR	Offset	Reset Value
Overflow Flag Register	**01_H**	**$0000\ 0000_H$**

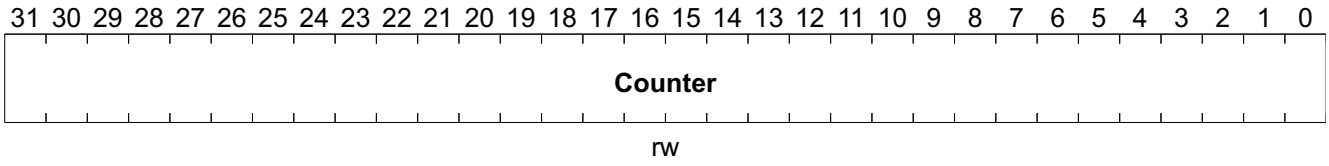


Field	Bits	Type	Description
P1CC	11	lhsc	**P1 collision count** 1_B **TBD**, Overflow
P1EC	10	lhsc	**P1 error count overflow** 1_B **TBD**, Overflow
P1TC	9	lhsc	**P1 transmit byte count overflow** 1_B **TBD**, Overflow
P1TP	8	lhsc	**P1 transmit packets overflow** 1_B **TBD**, Overflow
P1RC	7	lhsc	**P1 Receive byte count overflow** 1_B **TBD**, Overflow
P1RP	6	lhsc	**P1 Receive packets overflow** 1_B **TBD**, Overflow
P0CC	5	lhsc	**P0 collision count overflow** 1_B **TBD**, Overflow
P0EC	4	lhsc	**P0 error count overflow** 1_B **TBD**, Overflow
P0TC	3	lhsc	**P0 Transmit byte count overflow** 1_B **TBD**, Overflow

Field	Bits	Type	Description
P0TP	2	lhsc	**P0 Transmit packets overflow** 1_B **TBD**, Overflow
P0RC	1	lhsc	**P0 Receive byte count overflow** 1_B **TBD**, Overflow
P0RP	0	lhsc	**P0 Receive packets overflow** 1_B **TBD**, Overflow

Port 0 Counter Register

PCNR_0	Offset	Reset Value
Port 0 Counter Register	**02_H**	**$0000\ 0000_H$**



Field	Bits	Type	Description
Counter	31:0	rw	**Counter**

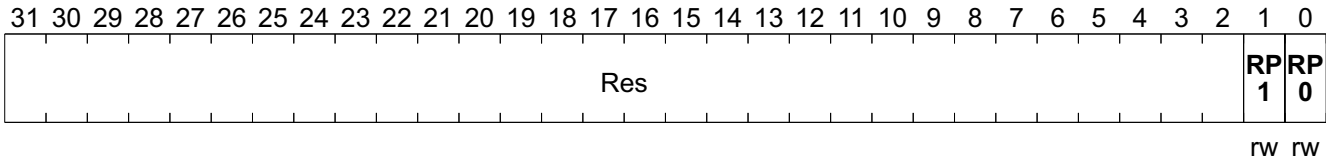
Other Counter Registers have the same structure and characteristics as **Port 0 Counter Register**; the names and offset addresses are listed in **Table 26**.

Table 26 Other Counter Registers

Register Short Name	Register Long Name	Offset Address	Page Number
P0RBC	P0 Receive byte count	03_H	
P0TP	P0 Transmit packets	04_H	
P0TBC	P0 Transmit byte count	05_H	
P0EC	P0 Error count	06_H	
P0CC	P0 Collision count	07_H	
P1RP	P1 Receive packets	08_H	
P1RBC	P1 Receive byte count	09_H	
P1TP	P1 Transmit packets	$0A_H$	
P1TBC	P1 Transmit byte count	$0B_H$	
P1EC	P1 Error count	$0C_H$	
P1CC	P1 Collision count	$0D_H$	

Port Counter Reset Register

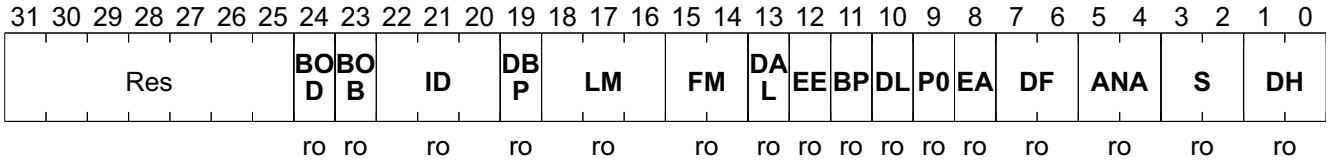
PCRR	Offset	Reset Value
Port Counter Reset Register	$0E_H$	$0000\ 0000_H$



Field	Bits	Type	Description
RP1	1	rw	**Reset All Counter of Port 1** 1_B **RP1**, Reset
RP0	0	rw	**Reset All Counter of Port 0** 1_B **RP0**, Reset

Hardware Setting Status Register

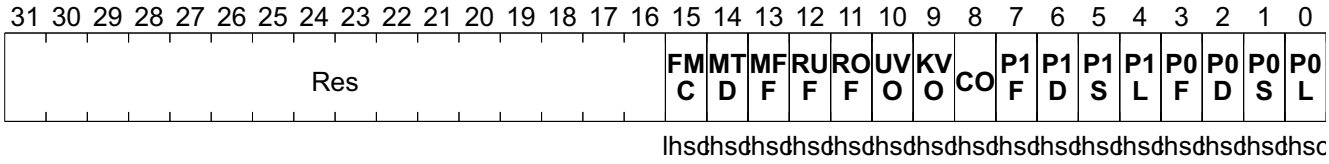
HW_SSR	Offset	Reset Value
Hardware Setting Status Register	$0F_H$	pin_H



Field	Bits	Type	Description
BOD	24	ro	**Bonding option: Disoam**
BOB	23	ro	**Bonding option: Bond128**
ID	22:20	ro	**Chip ID[2:0]**
DBP	19	ro	**Disable Back Pressure**
LM	18:16	ro	**Led Mode[2:0]**
FM	15:14	ro	**Fiber Mode[1:0]**
DAL	13	ro	**Disable MAC address learning**
EE	12	ro	**Enable OAM engine**
BP	11	ro	**Bypass Reserved MAC address Filtering**
DL	10	ro	**Disable Link Pass Through**
P0	9	ro	**P0 MDI/MDIX**
EA	8	ro	**Enable Auto-Crossover**
DF	7:6	ro	**Disable Flow Control[1:0]**
ANA	5:4	ro	**Recommend Auto-Negotiation Ability for TP Port[1:0]**
S	3:2	ro	**Recommend Speed 10 for TP Port[1:0]**
DH	1:0	ro	**Recommend Duplex Half for TP/FX Port[1:0]**

Interrupt Register

INT	Offset	Reset Value
Interrupt Register	10_H	$0000\ 0000_H$



Field	Bits	Type	Description
FMC	15	lhsc	**Forwarding Mode Change**
MTD	14	lhsc	**Match Timer Done**
MFF	13	lhsc	**Match Frame Found**
RUF	12	lhsc	**Request User Frame transmitted.**
ROF	11	lhsc	**Request OAM Frame transmitted.**
UVO	10	lhsc	**Unknown Valid OAM Frame received**
KVO	9	lhsc	**Known Valid OAM Frame received**
CO	8	lhsc	**Counter Overflow(** 0_B **TBD**, Normal 1_B **TBD**, Any counter defined in register 0x02~0x0e overflow
P1F	7	lhsc	**Port 1 Flow Control Ability Change** 0_B **N**, Normal 1_B **SC**, Status change
P1D	6	lhsc	**Port 1 Duplex Change(** 0_B **N**, Normal 1_B **SC**, Status change
P1S	5	lhsc	**Port 1 Speed Change(** 0_B **N**, Normal 1_B **SC**, Status change
P1L	4	lhsc	**Port 1 Link Status Change** 0_B **N**, Normal 1_B **SC**, Status change
P0F	3	lhsc	**Port 0 Flow Control Ability Change** 0_B **N**, Normal 1_B **SC**, Status change)
P0D	2	lhsc	**Port 0 Duplex Change** 0_B **N**, Normal 1_B **SC**, Status change
P0S	1	lhsc	**Port 0 Speed Change** 0_B **N**, Normal 1_B **SC**, Status change

Field	Bits	Type	Description
P0L	0	lhsc	**Port 0 Link Status Change** 0_B **N**, Normal 1_B **SC**, Status change

Interrupt Mask Register

INT_M	Offset	Reset Value
Interrupt Mask Register	**11_H**	**$0000\ 0000_H$**

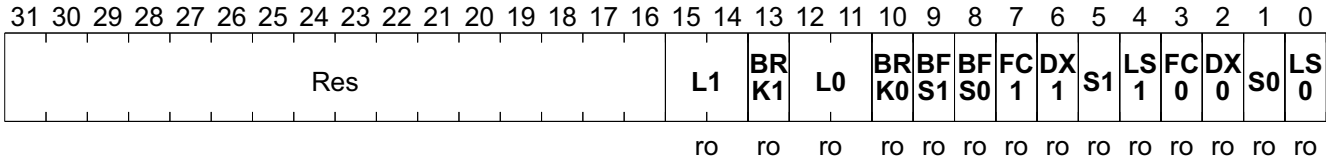
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res																FMC	MTD	MFCF	RUF	ROF	UVO	KVO	CO	P1F	P1D	P1S	P1L	P0F	P0D	P0S	P0L
																rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FMC	15	rw	**Forwarding Mode Change** 0_B **D**, Disable 1_B **E**, Enable
MTD	14	rw	**Match Timer Done** 0_B **D**, Disable 1_B **E**, Enable
MFCF	13	rw	**Match Frame Found** 0_B **D**, Disable 1_B **E**, Enable
RUF	12	rw	**Request User Frame transmitted.** 0_B **D**, Disable 1_B **E**, Enable
ROF	11	rw	**Request OAM Frame transmitted.** 0_B **D**, Disable 1_B **E**, Enable
UVO	10	rw	**Unknown Valid OAM Frame received** 0_B **D**, Disable 1_B **E**, Enable
KVO	9	rw	**Known Valid OAM Frame received** 0_B **D**, Disable 1_B **E**, Enable
CO	8	rw	**Counter Overflow** 0_B **D**, Disable 1_B **E**, Enable
P1F	7	rw	**Port 1 Flow Control Ability Change** 0_B **D**, Disable 1_B **E**, Enable

Field	Bits	Type	Description
P1D	6	rw	**Port 1 Duplex Change** 0_B **D**, Disable 1_B **E**, Enable
P1S	5	rw	**Port 1 Speed Change** 0_B **D**, Disable 1_B **E**, Enable
P1L	4	rw	**Port 1 Link Status Change** 0_B **D**, Disable 1_B **E**, Enable
P0F	3	rw	**Port 0 Flow Control Ability Change** 0_B **D**, Disable 1_B **E**, Enable
P0D	2	rw	**Port 0 Duplex Change** 0_B **D**, Disable 1_B **E**, Enable
P0S	1	rw	**Port 0 Speed Change** 0_B **D**, Disable 1_B **E**, Enable
P0L	0	rw	**Port 0 Link Status Change** 0_B **D**, Disable 1_B **E**, Enable

Port Status Register

PSR	Offset	Reset Value
Port Status Register	12_H	Real Time Status$_H$

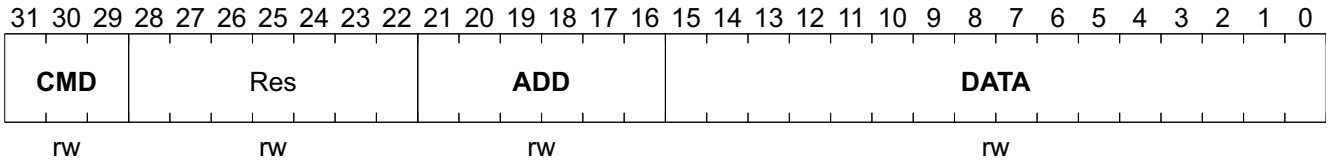


Field	Bits	Type	Description
L1	15:14	ro	**CBBRK_LENGTH of P1** 00_B **L1**, 0~60m 01_B **L2**, 60~90m 10_B **L3**, 90~130m 11_B **L4**, 130~170m
BRK1	13	ro	**CBBRK of P1** 0_B **N**, Normal 1_B **CB**, Cable Broken
L0	12:11	ro	**CBBRK_LENGTH of P0** 00_B **L1**, 0~60m 01_B **L2**, 60~90m 10_B **L3**, 90~130m 11_B **L4**, 130~170m
BRK0	10	ro	**CBBRK of P0** 0_B **N**, Normal 1_B **CB**, Cable Broken
BFS1	9	ro	**Buffer Full Status of Port 1** 0_B **N**, Normal 1_B **BF**, Buffer Full
BFS0	8	ro	**Buffer Full Status of Port 0** 0_B **N**, Normal 1_B **BF**, Buffer Full
FC1	7	ro	**Flow Control of Port 1** 0_B **D**, Disable 1_B **E**, Enable
DX1	6	ro	**Duplex of Port 1** 0_B **HD**, Half Duplex 1_B **FD**, Full Duplex
S1	5	ro	**Speed of Port 1** 0_B **10M**, 10M 1_B **100M**, 100M
LS1	4	ro	**Link Status of Port 1** 0_B **LD**, Link Down 1_B **LU**, Link Up

Field	Bits	Type	Description
FC0	3	ro	**Flow Control of Port 0** 0_B **D**, Disable 1_B **E**, Enable
DX0	2	ro	**Duplex of Port 0** 0_B **HD**, Half Duplex 1_B **FD**, Full Duplex
S0	1	ro	**Speed of Port 0** 0_B **10M**, 10M 1_B **100M**, 100M
LS0	0	ro	**Link Status of Port 0** 0_B **LD**, Link Down 1_B **LU**, Link Up

EEPROM Register File Access Control

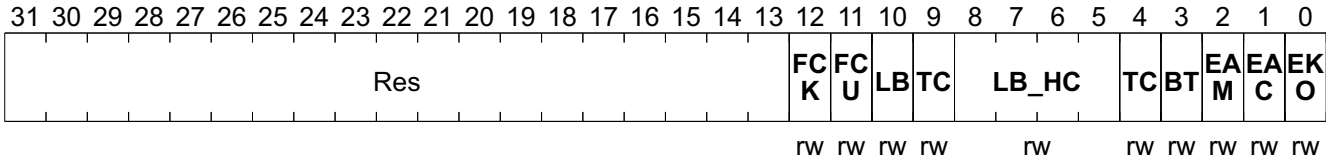
EE_RFAC	Offset	Reset Value
EEPROM Register File Access Control	**13_H**	**0000 4154$_H$**



Field	Bits	Type	Description
CMD	31:29	rw	**Command** 000_B **R**, Read 001_B **W**, Write others$_B$ **Res**, Reserved
Res	28:22	rw	**Reserved** 0000000_B **Res**, Reserved
ADD	21:16	rw	**Address** 00_H to $3F_H$
DATA	15:0	rw	**Data**

OAM Control Register

OAM_CR	Offset	Reset Value
OAM Control Register	14_H	$0000\ 0000_H$

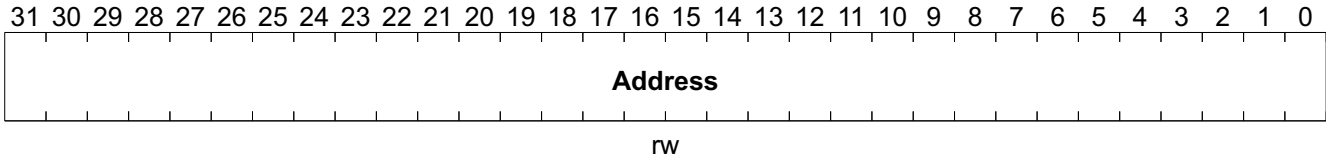


Field	Bits	Type	Description
FCK	12	rw	**OAM FIFO Control for NTT TS-1000 frame** 0_B **SK**, Store known OAM frame to FIFO (Default) 1_B **N**, Do not store
FCU	11	rw	**OAM FIFO Control for unknown frame** 0_B **SU**, Store unknown OAM frame to FIFO (Default) 1_B **N**, Do not store
LB	10	rw	**Loop Back Test User Frame Transmit Control** 0_B **N**, Normal (Default) 1_B **REQ**, Request to transmit an user frame which the SA is defined in SMI register 15_H and 16_H. After the requested user frame is transmitted, this bit is cleared.
TC	9	rw	**OAM frame Transmit control** 0_B **N**, Normal (Default) 1_B **REQ**, Request to transmit an OAM frame which is defined in SMI register 17_H, 18_H and 19_H. After the requested OAM frame is transmitted, this bit is cleared.
LB_HC	8:5	rw	**Loop Back Test User Frame Handling Control** 0000_B **D**, Disable (Default) $> 0000_B$ **N**, Find the first valid received Ethernet frame with its CRC is the same with the most recently transmitted Ethernet frame during NNNN*10ms After the frame is found or the timer count done, the register will be cleared. And the search result will be stored to Register $1D_H$ Bit [1:0].
TC	4	rw	**Discard all Ethernet frame from FX control** 0_B **N**, Normal (Default) 1_B **DE**, Discard all Ethernet frames received from Port1
BT	3	rw	**Block the traffic from TP to FX control** 0_B **N**, Normal (Default) 1_B **BT**, Block the traffic from Port0 to Port1
EAM	2	rw	**Enable Auto M field** NTT TS-1000 OAM Vendor ID/Model Number by embedded OAM engine 0_B **E**, Enable (Default) 1_B **D**, Disable

Field	Bits	Type	Description
EAC	1	rw	**Enable Auto CRC** NTT TS-1000 OAM CRC by embedded OAM engine 0_B **E**, Enable (Default) 1_B **D**, Disable
EKO	0	rw	**Enable Known OAM Frame Handling** NTT TS-1000 OAM Frame by embedded OAM engine 0_B **E**, Enable(Default) 1_B **D**, Disable

Source Address of Loop Back Test User Frame 0

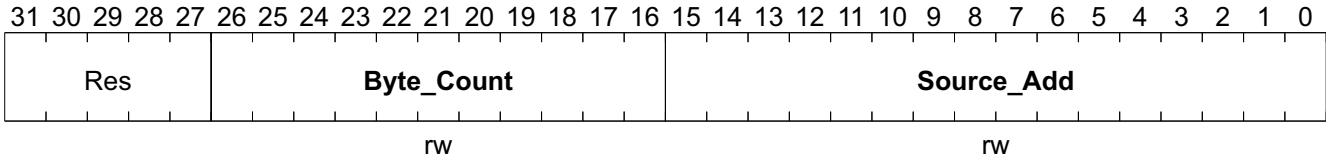
SA_F_0	Offset	Reset Value
Source Address of Loop Back Test User Frame 0	**15_H**	**$0000\ 0000_H$**



Field	Bits	Type	Description
Address	31:0	rw	**Source Address**

Source Address of Loop Back Test User Frame 1

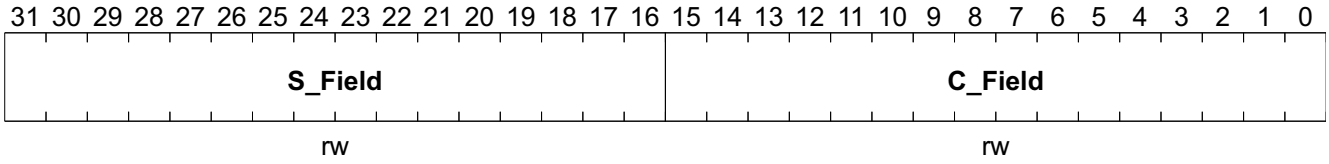
SA_F_1	Offset	Reset Value
Source Address of Loop Back Test User Frame 1	16_H	0000 0000_H



Field	Bits	Type	Description
Byte_Count	26:16	rw	**Total Byte Count of payload** Valid Ethernet frame: 46 byte ~ 1500 byte
Source_Add	15:0	rw	**Source Address SA[47:32]**

Transmit OAM Frame Register 0

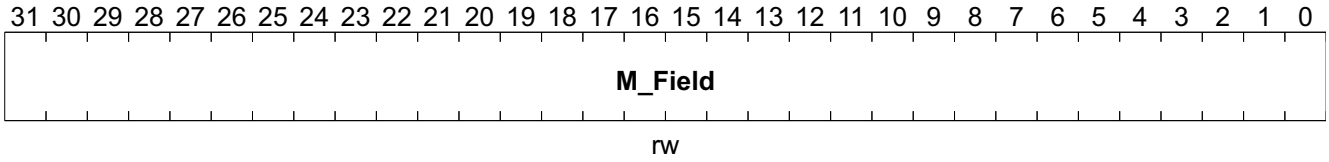
TFR_0	Offset	Reset Value
Transmit OAM Frame Register 0	17_H	0000 0000_H



Field	Bits	Type	Description
S_Field	31:16	rw	**S Field of OAM Frame**
C_Field	15:0	rw	**C Field of OAM Frame**

Transmit OAM Frame Register 1

TFR_1	Offset	Reset Value
Transmit OAM Frame Register 1	18_H	0000 0000_H

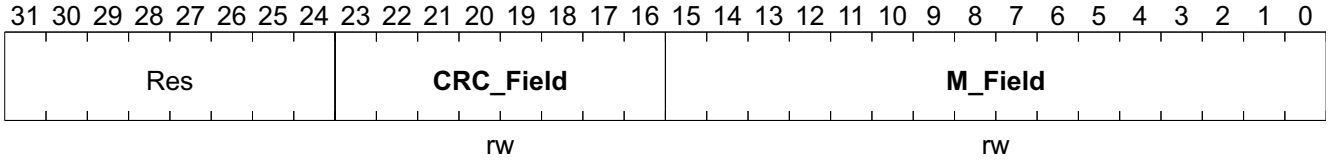


Field	Bits	Type	Description
M_Field	31:0	rw	**M Field Bit [31:0] of OAM Frame**

Transmit OAM Frame Register 2

TFR_2 **Offset** **Reset Value**

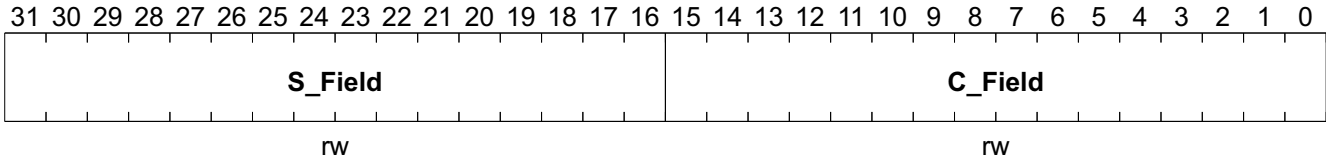
Transmit OAM Frame Register 2 **19_H** **$0000\ 0000_H$**



Field	Bits	Type	Description
CRC_Field	23:16	rw	**CRC Field of OAM Frame**
M_Field	15:0	rw	**M Field Bit [47:32] of OAM Frame**

Received OAM Frame Register 0

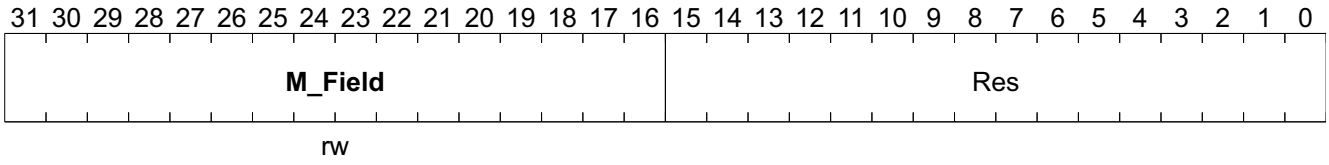
RFR_0	Offset	Reset Value
Received OAM Frame Register 0	**$1A_H$**	**$0000\ 0000_H$**



Field	Bits	Type	Description
S_Field	31:16	rw	**S Field of Received OAM Frame**
C_Field	15:0	rw	**C Field of Received OAM Frame**

Received OAM Frame Register 1

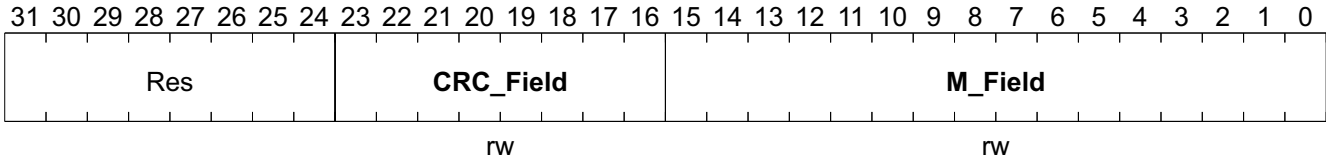
RFR_1	Offset	Reset Value
Received OAM Frame Register 1	**$1B_H$**	**$0000\ 0000_H$**



Field	Bits	Type	Description
M_Field	31:16	rw	**M Field Bit [31:0] of Received OAM Frame**

Received OAM Frame Register 2

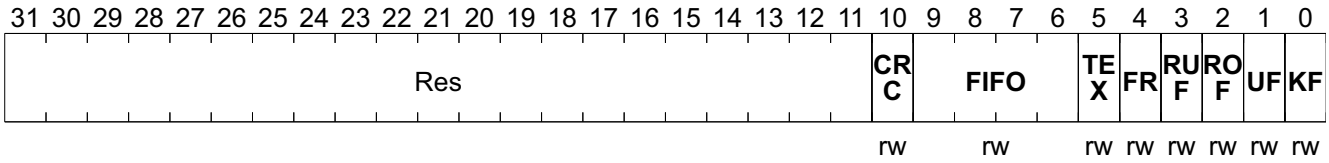
RFR_2	Offset	Reset Value
Received OAM Frame Register 0	$1C_H$	$0000\ 0000_H$



Field	Bits	Type	Description
CRC_Field	23:16	rw	**CRC Field of Received OAM Frame**
M_Field	15:0	rw	**M Field Bit [47:32] of Received OAM Frame**

OAM Frame Status Register

OAM_FSR	Offset	Reset Value
OAM Frame Status Register	$1D_H$	$0000\ 0000_H$



Field	Bits	Type	Description
CRC	10	rw	**Bad CRC OAM Received** 0_B **NB**, No bad CRC OAM received 1_B **B**, Bad CRC OAM received
FIFO	9:6	rw	**Embedded OAM FIFO Utilization** 0000_B **E**, FIFO empty 1000_B **25**, 25% 1100_B **50**, 50% 1110_B **75**, 75% 1111_B **F**, FIFO full
TEX	5	rw	**Status of Loop Back Test Timer** 0_B **NOT**, Timer does not expire before a matched frame is found 1_B **YES**, Timer expires before a matched frame found
FR	4	rw	**Status of Loop Back Test User Frame** 0_B **NF**, Matched frame is not found 1_B **F**, Matched frame is found
RUF	3	rw	**Request User Frame transmitted**
ROF	2	rw	**Request OAM Frame transmitted**

Field	Bits	Type	Description
UF	1	rw	**Unknown Valid OAM Frame received**
KF	0	rw	**Known Valid OAM Frame received**

5 Electrical Specification

DC and AC.

5.1 DC Characterization

Table 27 Electrical Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	-0.3		3.6	V	
Input Voltage	V_{IN}	-0.3		V_{CC} + 0.3	V	
Output Voltage	*Vout*	-0.3		V_{CC} + 0.3	V	
Storage Temperature	*TSTG*	-55		155	C	
Power Dissipation	*PD*			990	mW	
ESD Rating	*ESD*			2	KV	

Table 28 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply[1)]	*Vcc*	3.135	3.3	3.465	V	
Core Power Supply[2)]	*Vcore*	1.71	1.8	1.89		
Input Voltage	*Vin*	0	-	Vcc	V	
Junction Operating Temperature	*Tj*	0	25	115	°C	

1) VCC3O. VCCBIAS
2) VCCIK. VCCA2. VCCPLL

Table 29 DC Electrical Characteristics for 3.3 V Operation[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	*VIL*			0.8	V	TTL
Input High Voltage	*VIH*	2.0			V	TTL
Output Low Voltage	*VOL*			0.4	V	TTL
Output High Voltage	*VOH*	2.4			V	TTL
Input Pull_up/down Resistance	*RI*		50		KΩ	VIL = 0 V or VIH = Vcc

1) Under VCC = 3.0 V~ 3.6 V, Tj = °C ~ 115 °C

5.2 AC Characterization

Power on Reset Timing, EEPROM Interface Timing, and SMI Timing.

Power on Reset Timing

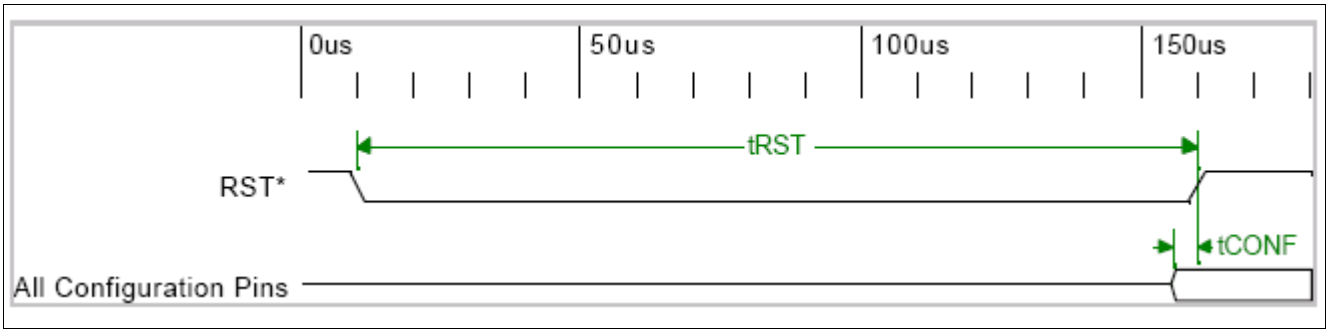


Figure 5 Power on Reset Timing

Table 30 Power on Reset Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RST Low Period	t_{RST}	100			ms	TTL
Start of Idle Pulse Width	t_{CONF}	100			ns	TTL

EEPROM Interface Timing

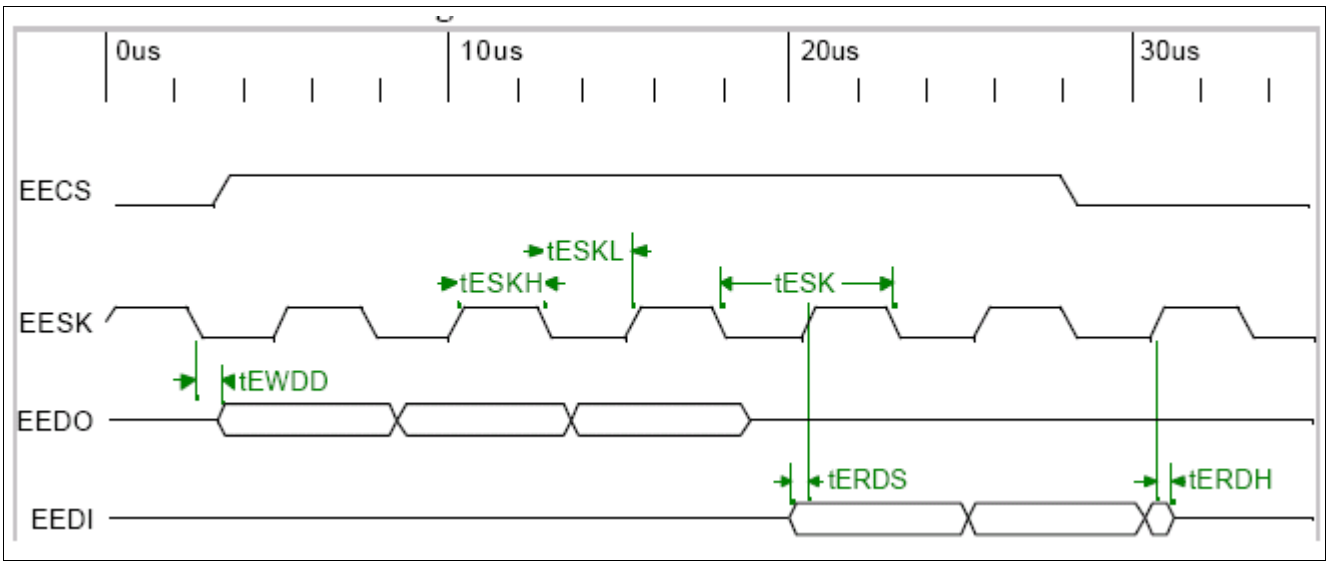


Figure 6 EEPROM Interface Timing

Table 31 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	t_{ESK}		5120		ns	
EESK Low Period	t_{ESKL}	2550		2570	ns	
EESK High Period	t_{ESKH}	2550		2570	ns	
EEDI to EESK Rising Setup Time	t_{ERDS}	10			ns	

Table 31 EEPROM Interface Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EEDI to EESK Rising Hold Time	t_{ERDH}	10			ns	
EESK Falling to EEDO Output Delay Time	t_{EWDD}			20	ns	

SMI Timing

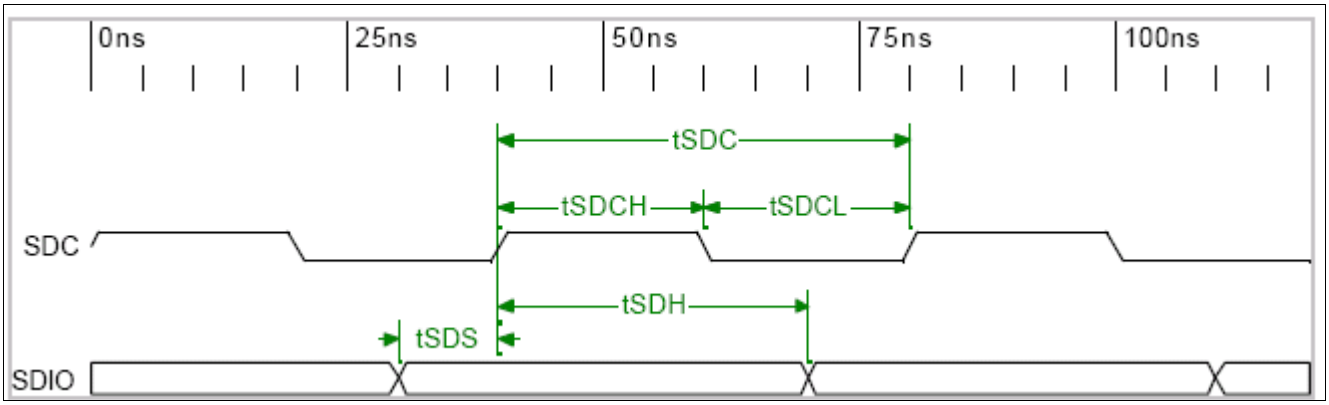


Figure 7 SMI Timing

Table 32 SMI Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDC Period	t_{CK}	20			ns	
SDC Low Period	t_{CKL}	10			ns	
SDC High Period	t_{CKH}	10			ns	
SDIO to SDC rising setup time on read/write cycle	t_{SDS}	4			ns	
SDIO to SDC rising hold time on read/write cycle	t_{SDH}	2			ns	

6 Packaging

64 LQFP Packaging for NinjaC (ADM6992-C)

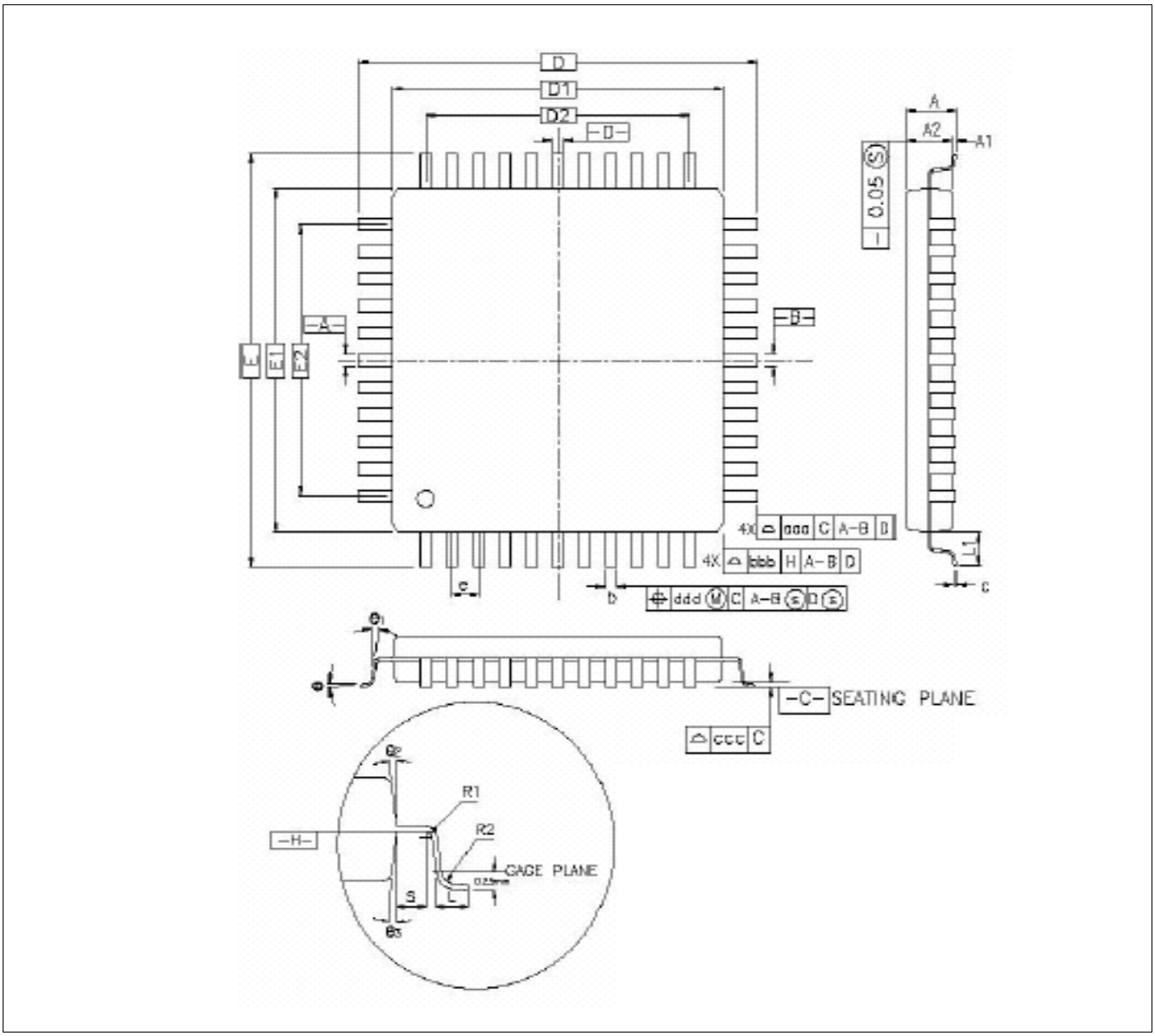


Figure 8 64 pin LQFP Outside Dimension

Table 33 Dimensions for 64 Pin LQFP Outside Dimension

Symbol	Millimeter (mm)			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	–	–	1.60	–	–	0.063
A_1	0.05	–	0.15	0.002	–	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D		12.00 BSC.			0.472 BSC.	
D_1		10.00 BSC			0.393 BSC.	
E		12.00 BSC			0.472 BSC.	
E_1		10.00 BSC			0.393 BSC.	
R_2	0.08	–	0.20	0.003	–	0.008
R_1	0.08	–	–	0.003	–	–
Θ	0°	3.5°	7°	0°	3.5°	7°
$Θ_1$	0°	–	–	0°	–	–
$Θ_2$	11°	12°	13°	11°	12°	13°
$Θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 Ref.			0.039 Ref.	
S	0.20	–	–	0.008	–	–
			64L			
b	0.17	0.20	0.27	0.007	0.008	0.011
e		0.50 BSC.			0.020 BSC.	
D_2		7.50			0.295	
E_2		7.50			0.295	
Tolerance of Form and Position						
aaa		0.20			0.008	
bbb		0.20			0.008	
ccc		0.08			0.003	
ddd		0.08			0.003	

Note:

1. *Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
2. *Dimensions b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.*
3. *Dimension of 44L “b“ different with JEDEC spec.(ASE: 0.22/0.30/0.38)(JEDEC: 0.30/0.37/0.45).*

References

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Terminology

A

B

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