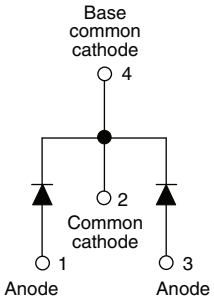
Schottky Rectifier, 2 x 3.5 A



D-PAK (TO-252AA)



FEATURES

- Popular D-PAK outline
- Center tap configuration
- Small foot print, surface mountable
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Compliant to RoHS Directive 2002/95/EC
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C

RoHS COMPLIANT

DESCRIPTION

The VS-6CWQ04FNPbF surface mount, center tap, Schottky rectifier series has been designed for applications requiring low forward drop and small foot prints on PC board. Typical applications are in disk drives, switching power supplies, converters, freewheeling diodes, battery charging, and reverse battery protection.

PRODUCT SUMMARY	
Package	D-PAK (TO-252AA)
$I_{F(AV)}$	2 x 3.5 A
V_R	40 V
V_F at I_F	See Electrical table
I_{RM}	24 mA at 125 °C
T_J max.	150 °C
Diode variation	Common cathode
E_{AS}	8 mJ

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	7	A
V_{RRM}		40	V
I_{FSM}	t_p = 5 µs sine	500	A
V_F	3 Apk, T_J = 125 °C (per leg)	0.49	V
T_J	Range	- 40 to 150	°C

VOLTAGE RATINGS			
PARAMETER	SYMBOL	VS-6CWQ04FNPbF	UNITS
Maximum DC reverse voltage	V_R	40	V
Maximum working peak reverse voltage	V_{RWM}		

ABSOLUTE MAXIMUM RATINGS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current See fig. 5	per leg	$I_{F(AV)}$	50 % duty cycle at T_C = 135 °C, rectangular waveform	3.5	A
	per device			7	
Maximum peak one cycle non-repetitive surge current per leg See fig. 7		I_{FSM}	5 µs sine or 3 µs rect. pulse; Following any rated load condition and with rated V_{RRM} applied	500	
			10 ms sine or 6 ms rect. pulse; Following any rated load condition and with rated V_{RRM} applied	80	
Non-repetitive avalanche energy per leg		E_{AS}	T_J = 25 °C, I_{AS} = 1 A, L = 16 mH	8.0	mJ
Repetitive avalanche current per leg		I_{AR}	Current decaying linearly to zero in 1 µs Frequency limited by T_J maximum V_A = 1.5 x V_R typical	1.0	A

ELECTRICAL SPECIFICATIONS					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**VALUES**	**UNITS**
Maximum forward voltage drop per leg See fig. 1	V_{FM} (1)	3 A	T_J = 25 °C	0.53	V
		6 A		0.67	
		3 A	T_J = 125 °C	0.49	
		6 A		0.62	
Maximum reverse leakage current per leg See fig. 2	I_{RM} (1)	T_J = 25 °C	V_R = Rated V_R	2	mA
		T_J = 125 °C		24	
Threshold voltage	$V_{F(TO)}$	T_J = T_J maximum		0.34	V
Forward slope resistance	r_t			37.33	mΩ
Typical junction capacitance per leg	C_T	V_R = 5 V_{DC} (test signal range 100 kHz to 1 MHz), 25 °C		189	pF
Typical series inductance per leg	L_S	Measured lead to lead 5 mm from package body		5.0	nH
Maximum voltage rate of change	dV/dt	Rated V_R		10 000	V/µs

Note

(1) Pulse width < 300 µs, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER		**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum junction and storage temperature range		T_J (1), T_{Stg}		- 40 to 150	°C
Maximum thermal resistance, junction to case	per leg	R_{thJC}	DC operation See fig. 4	4.70	°C/W
	per device			2.35	
Approximate weight				0.3	g
				0.01	oz.
Marking device			Case style D-PAK (similar to TO-252AA)	6CWQ04FN	

Note

(1) $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$ thermal runaway condition for a diode on its own heatsink

For technical questions within your region, please contact one of the following:
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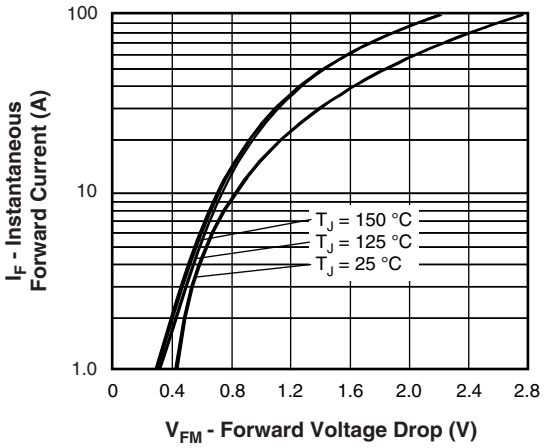


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

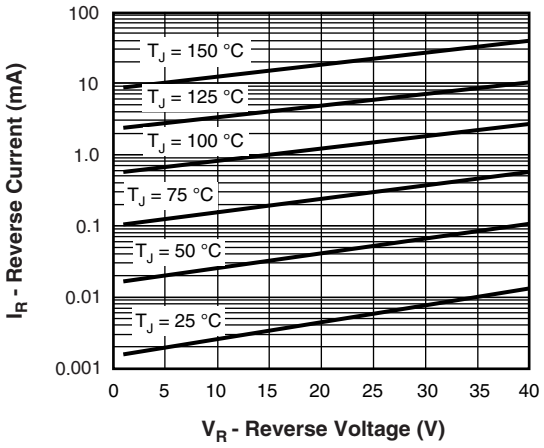


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

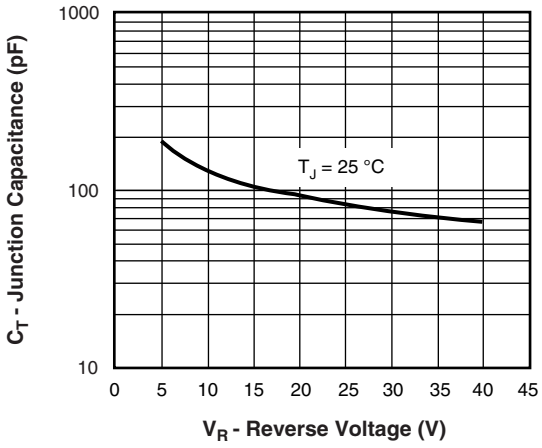


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

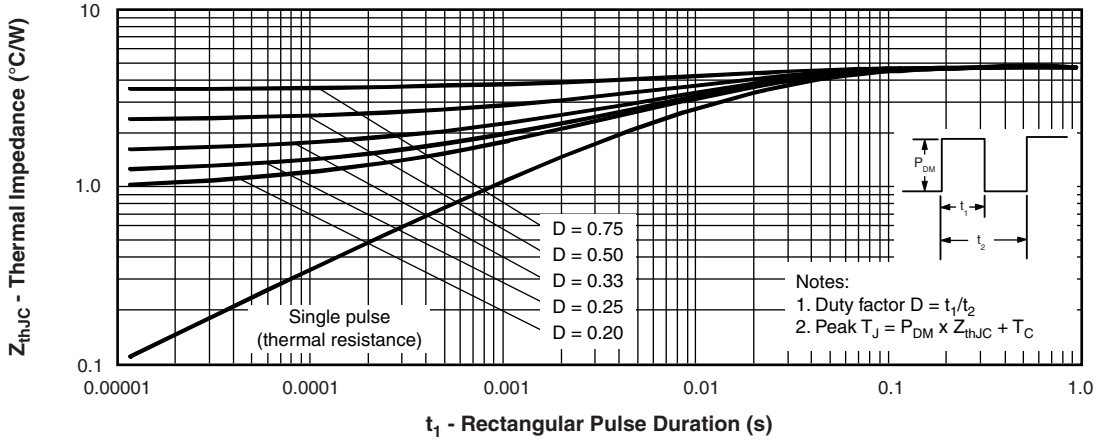


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics (Per Leg)

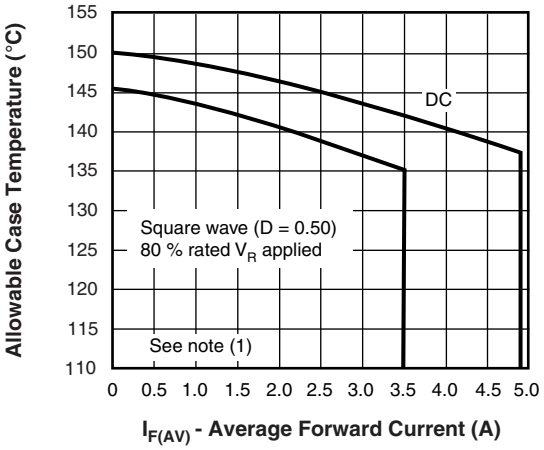


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

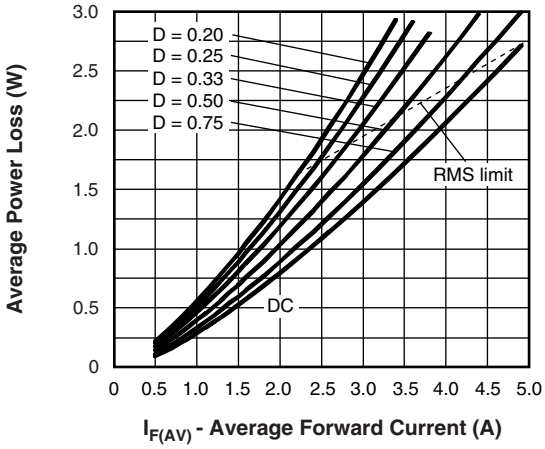


Fig. 6 - Forward Power Loss Characteristics (Per Leg)

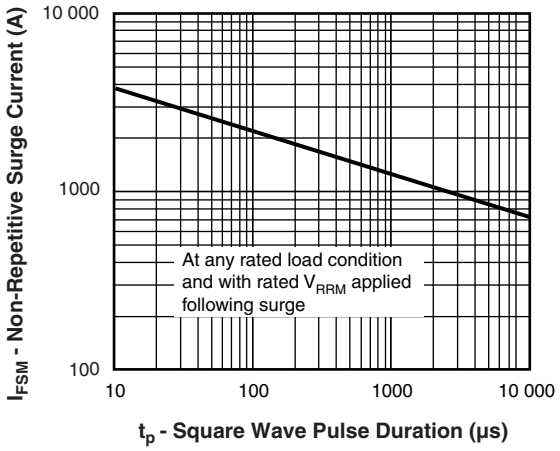


Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

Note

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$;
Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}$/D) (see fig. 6);
Pd_{REV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at V_{R1} = 80 % rated V_R

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ORDERING INFORMATION TABLE

Device code

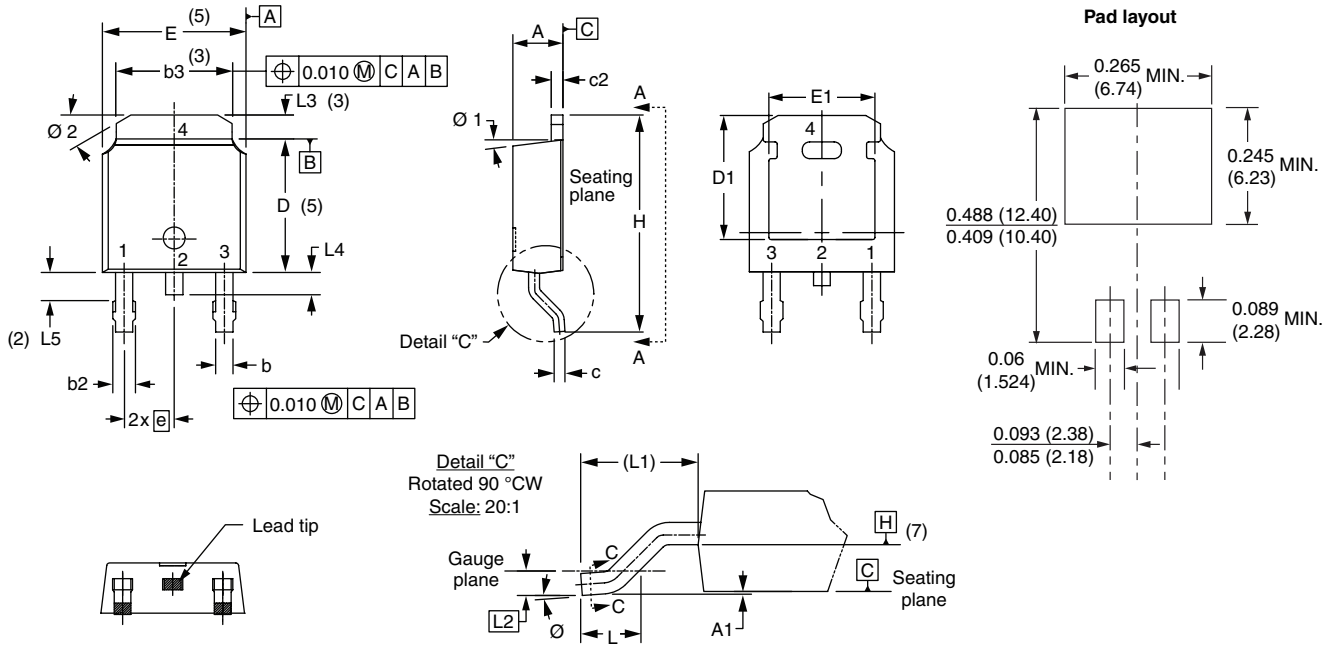
VS-	6	C	W	Q	04	FN	TRL	PbF
1	2	3	4	5	6	7	8	9

1 - Vishay Semiconductors product
2 - Current rating (7 A)
3 - Center tap configuration
4 - Package identifier:
W = D-PAK
5 - Schottky “Q” series
6 - Voltage rating (04 = 40 V)
7 - FN = TO-252AA (D-PAK)
8 - • None = Tube (50 pieces)
• TR = Tape and reel
• TRL = Tape and reel (left oriented)
• TRR = Tape and reel (right oriented)
9 - PbF = Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95016
Part marking information	www.vishay.com/doc?95059
Packaging information	www.vishay.com/doc?95033

D-PAK (TO-252AA)

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	0.094	
A1	-	0.13	-	0.005	
b	0.64	0.89	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	3
c	0.46	0.61	0.018	0.024	
c2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	5
D1	5.21	-	0.205	-	3
E	6.35	6.73	0.250	0.265	5
E1	4.32	-	0.170	-	3

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
e	2.29 BSC		0.090 BSC		
H	9.40	10.41	0.370	0.410	
L	1.40	1.78	0.055	0.070	
L1	2.74 BSC		0.108 REF.		
L2	0.51 BSC		0.020 BSC		
L3	0.89	1.27	0.035	0.050	3
L4	-	1.02	-	0.040	
L5	1.14	1.52	0.045	0.060	2
Ø	0°	10°	0°	10°	
Ø1	0°	15°	0°	15°	
Ø2	25°	35°	25°	35°	

Notes

(1) Dimensioning and tolerancing as per ASME Y14.5M-1994

(2) Lead dimension uncontrolled in L5

(3) Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad

(4) Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip

(5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

(6) Dimension b1 and c1 applied to base metal only

(7) Datum A and B to be determined at datum plane H

(8) Outline conforms to JEDEC outline TO-252AA

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