DATA SHEET

GPCD9001A

8-Channel Sound Controller

Preliminary

JAN. 06, 2011

Version 0.3

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8-CHANNEL SOUND CONTROLLER

1.GENERAL DESCRIPTION

GPCD9001A is ROMless and workable up to 4M bytes external ROM, 512 bytes working SRAM, three sets of 12-bit timers, 32 general I/Os, one 10-bit ADC with 8 channels input and one 14-bit DAC with push-pull amplifier. The microprocessor can implement software based on audio processing, functional control and others. For audio processing, melody and speech can be mixed into one output. GPCD9001A is implemented with a high performance SPU voice engine to play 8-channel voice with ADPCM/PCM data. It operates over a wide voltage range of 2.4V - 5.5V and includes Low Voltage Reset function. In addition, GPCD9001A provides sleep mode for power savings. It can be waked up from sleep mode by interrupt sources or by IO's state change. There is a Serial Peripheral Interface (SPI) controller built-in GPCD9001A to facilitate communicating with other devices and components.

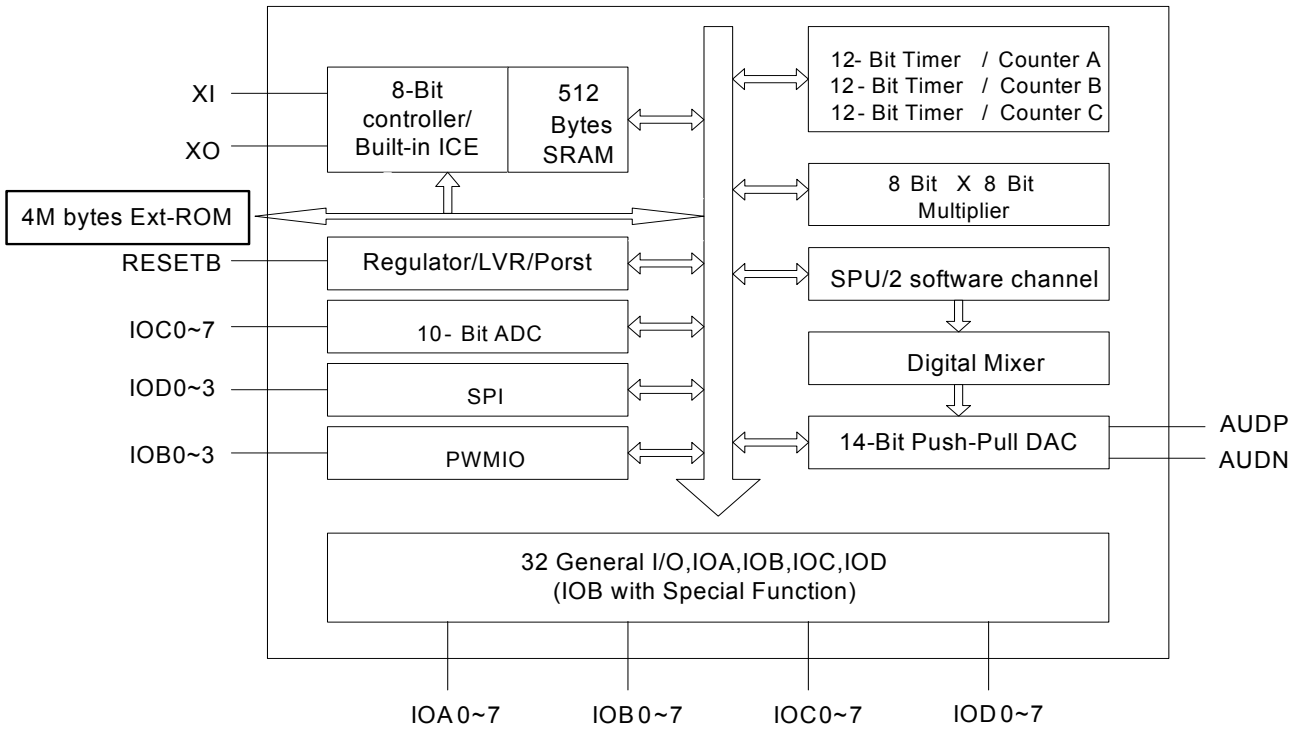
2.FEATURES

- Working Voltage: 2.4V - 5.5V
- CPU speed: Max. 8MHz.
- F_{OSC} = Max. 16MHz (2 x CPU clock)
- External ROM Max. 4M bytes
- RAM size: Max. 512 bytes
- Three 12-bit timer/counter, TMA with capture and comparison function, TMB/TMC with comparison function (Programmable and auto reload)
- Sleep mode to reduce power
- Key change wake-up function
- 16 IRQs & 7 NMI Interrupts
- Watchdog function
- 5.5V to 3.3V regulator
- Low Voltage Reset
- 32 general I/Os (bit programmable)
- 8 I/O with high sink current for LED application
- All IO with 1M pull low function to prevent current leakage from error key touch
- One 14-bit DAC with push-pull amplifier for direct drive speaker
- SPU (Sound Processing Unit) engine can output audio data with 14-bit resolution to perform high quality voice/melody
- IR PWM Output
- Hardware PWMIO supports 4 LED outputs with brightness control of 256-level
- Real-time clock
- 8-channel SPU engine with ADPCM/PCM wave table
- Two set of 14 bits software channel with noise filter to play high quality sound.
- Generalplus ICE_CORE embedded, new Application can be developed using SunMidiar® Development tools
- Interface to speed up flash program and read
- Tone color (Speech) with ADPCM algorithm to save memory usage
- 10-bit ADC with 8 channel line-in
- SPI master/slave interface

3.APPLICATION FIELD

- Talking instrument controller
- General music synthesizer
- General purpose controller
- High end toy controller
- Intelligent education toys
- And more

4.BLOCK DIAGRAM

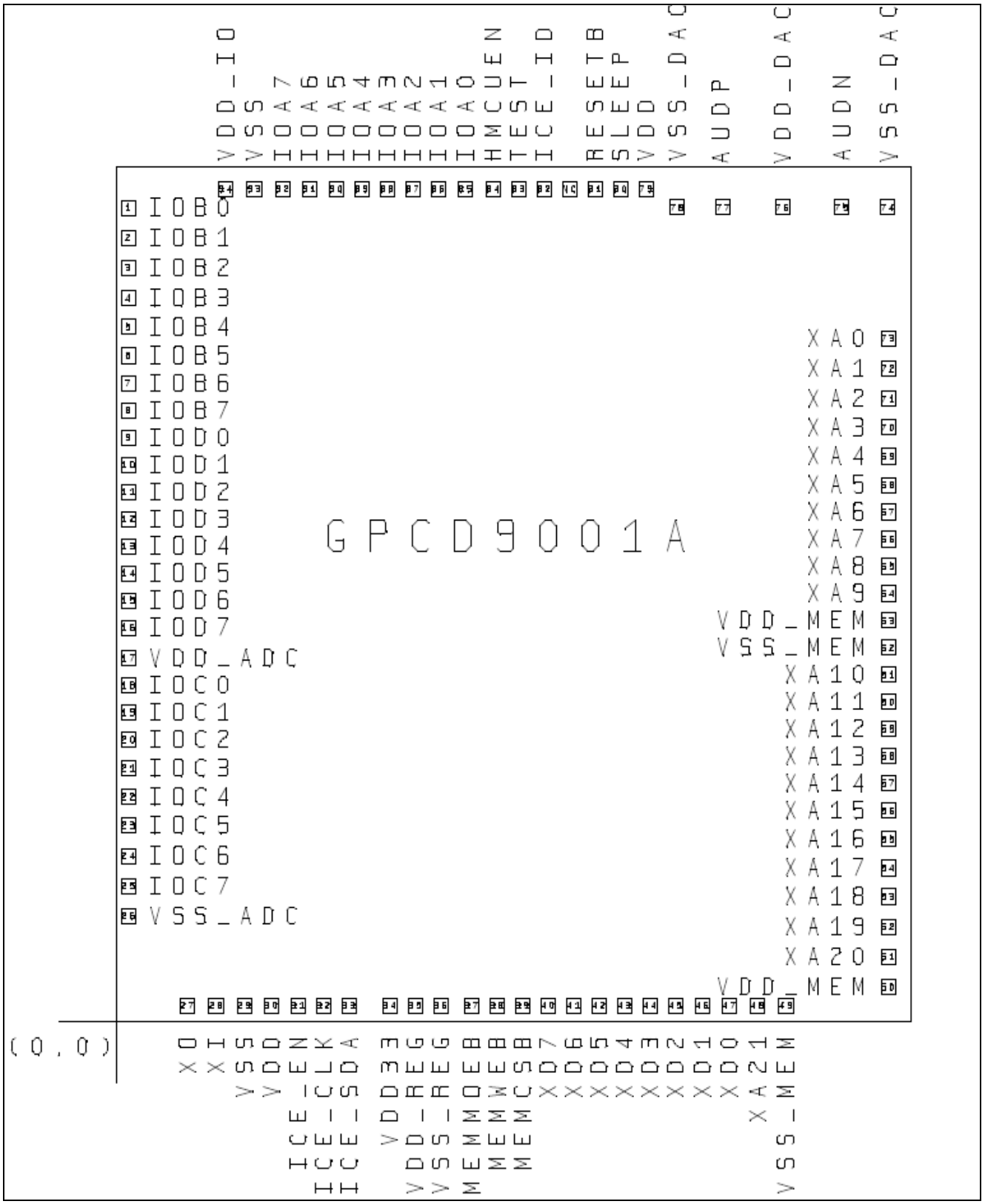


5. SIGNAL DESCRIPTION

Name	Pin No.	LQFP 128 Pin No.	Type	Description	Note
IO PORT					
IOA0~IOA7	85~92	109~116	I/O	Bi-directional IO ports, can be wakeup pins	-
IOB0~IOB7	1~8	1~8	I/O	Bi-directional IO ports, can be wakeup pins	-
IOC0~IOC7	18~25	18~25	I/O	Bi-directional IO ports, can be wakeup pins	-
IOD0~IOD7	9~16	9~16	I/O	Bi-directional IO ports, can be wakeup pins	-
ROM/OTP Address & Data Bus Interface					
XA0~XA21	73~64,61~51,48	88~79,76~66,54	O	Address of 4M byte external ROM	-
XD0~XD7	47~40	53~46	I/O	Data bus of 4M byte external ROM	-
MEMCSB	39	45	O	Memory chip select enable(active low)	-
MEMWEB	38	44	O	Memory write enable(active low)	-
MEMOEB	37	43	O	Memory output enable(active low)	-
ICE Related					
ICE_EN	31	37	I	ICE enable	Pull-low
ICE_CLK	32	38	I	ICE clock	Pull-low
ICE_SDA	33	39	I/O	ICE serial data bus	-
Clock Related					
XO	27	33	O	Oscillator Crystal output	-
XI	28	34	I	Oscillator crystal input./R_{OSC} input	Floating
POWER PAD					
VDD_ADC	17	17	I	Positive supply for ADC/IOC (2.4V~5.5V)	-
VDD_REG	35	41	I	Positive supply for regulator (2.4V~5.5V)	-
VDD_MEM	50,63	65,78	I	Positive supply for memory AD bus and its control pin (2.4V~5.5V)	X2
VDD_DAC	76	99	I	Positive supply for push-pull DAC (2.4V~5.5V)	-
VDD_IO	94	118	I	Positive supply for IOA,IOB,IOD (2.4V~5.5V)	-
VDD	30,79	36,102	I	Positive supply for core power (MUST be connected with VDD33)	X2
VDD33	34	40	O	3V power output from regulator	-
VSS_REG	36	42	I	Ground reference for regulator	-
VSS_MEM	49,62	55,77	I	Ground reference for memory	X2
VSS	29,93	35,117	I	Ground reference for IOA/IOB/IOC, ICE, core etc.	X2
VSS_ADC	26	26	I	Ground reference for ADC	-
VSS_DAC	74,78	97,101	I	Ground reference for push-pull DAC	X2
Others					
ICE_ID	82	106	I	ICE ID for flash identification	Pull-low
HMCUEN	84	108	I	Select HARDMACRO 6502(1) or RTL 6502 (0)	Pull-high
RESETB	81	104	I	External reset pin(active low)	Pull-high
TEST	83	107	I	Test mode	Pull-low
AUDP	77	100	O	Audio output of push pull DAC	-
AUDN	75	98	O	Audio output of push pull DAC	-
SLEEP	80	103	O	Sleep indicator	-

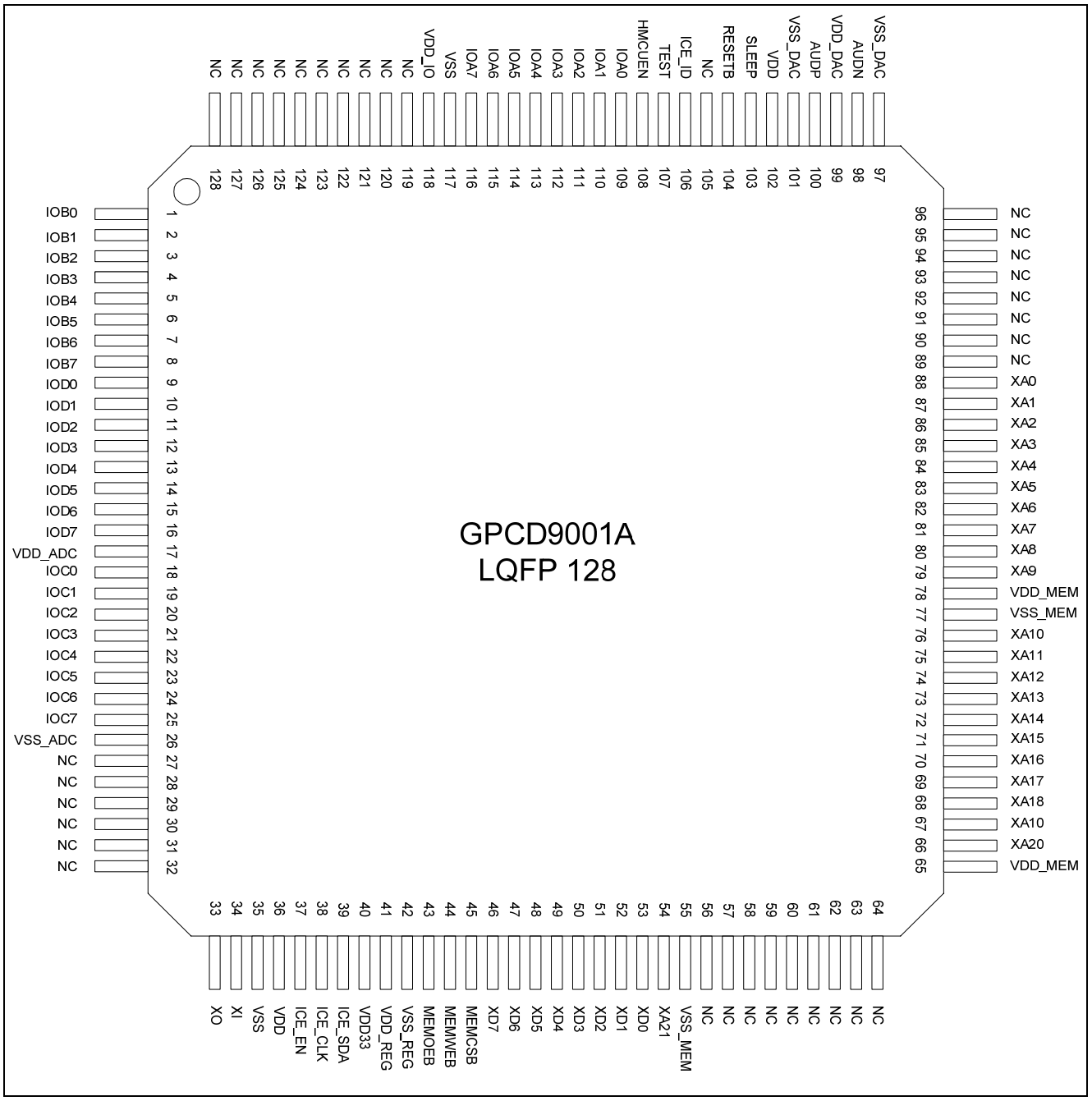
Total 94 pads

5.1. PAD Assignment



The IC substrate should be floating or connect to VSS

5.2. Pin Map – LQFP 128



6. FUNCTIONAL DESCRIPTIONS

6.1. SRAM

The 512-byte SRAM (including Stack) area is located in $000000~$0002FF.

6.2. ROM

GPCD9001A can be selected external ROM with maximum 4M bytes.

6.3. Low Voltage Reset

GPCD9001A provides another important feature, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops under LVR. Without LVR, the CPU becomes unstable and malfunction when working voltage is too low.

6.4. Interrupt

GPCD9001A has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls 16 IRQs and 7 NMIs. A NMI cannot be interrupted by any other IRQs.

Interrupt Source	Interrupt Name	Priority
Timer A	NMI_TIMER_A	NMI
Timer B	NMI_TIMER_B	NMI
Timer C	NMI_TIMER_C	NMI
CPU_CLOCK/1024	NMI_D1024	NMI
CPU_CLOCK/4096	NMI_D4096	NMI
KEY	NMI_KEY	NMI
EXT	NMI_EXT	NMI
TIMER A	IRQ_TIMER_A	IRQ1
TIMER B	IRQ_TIMER_B	IRQ2
TIMER C	IRQ_TIMER_C	IRQ3
CPU_CLOCK/1024	IRQ_D1024	IRQ4
CPU_CLOCK/4096	IRQ_D4096	IRQ5
16 Hz	IRQ_16Hz	IRQ6
2 Hz	IRQ_2 Hz	IRQ7
KEY	IRQ_KEY	IRQ8
EXT	IRQ_EXT	IRQ9
SPU	IRQ_SPU	IRQ10
SPI	IRQ_SPI	IRQ11
ADC	IRQ_ADC	IRQ12
QD1_F	IRQ_QD1_F	IRQ13
QD1_B	IRQ_QD1_B	IRQ14
QD2_F	IRQ_QD2_F	IRQ15
QD2_B	IRQ_QD2_B	IRQ16

6.5. Hardware PWMIO

Hardware PWMIO supports 4 LED outputs with brightness control of 256-level. The clock source of PWMIO can be selected by user's request.

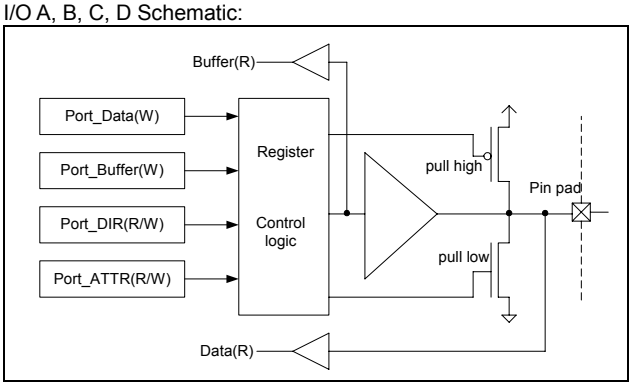
6.6. I/O

The purpose of input and output ports is to communicate with other devices. Four programmable I/O ports are built-in, including Port A, B, C, and D. All Ports are general I/O with programmable wake-up capability and 1M pull low function. In addition to general I/O function, PortB also provides some special functions in certain pins. PortA0~3 and PortB0~3 provide large sink current for LED application. The Port C, D is sharing other module's function such as ADC, SPI etc. Refer to following figure for **IO Sharing**.

6.6.1. I/O Configuration

The following diagram represents the I/O schematic.

I/O A, B, C, D Schematic:



Port_Data and Port_Buffer are written into the same register but read from different node. To activate key wakeup function, first latch data on IOX_Data and enable the key wakeup function. Wakeup is triggered when the port's state is different from first latched data.

A summary of IO sharing is listed as follows.

IO Sharing

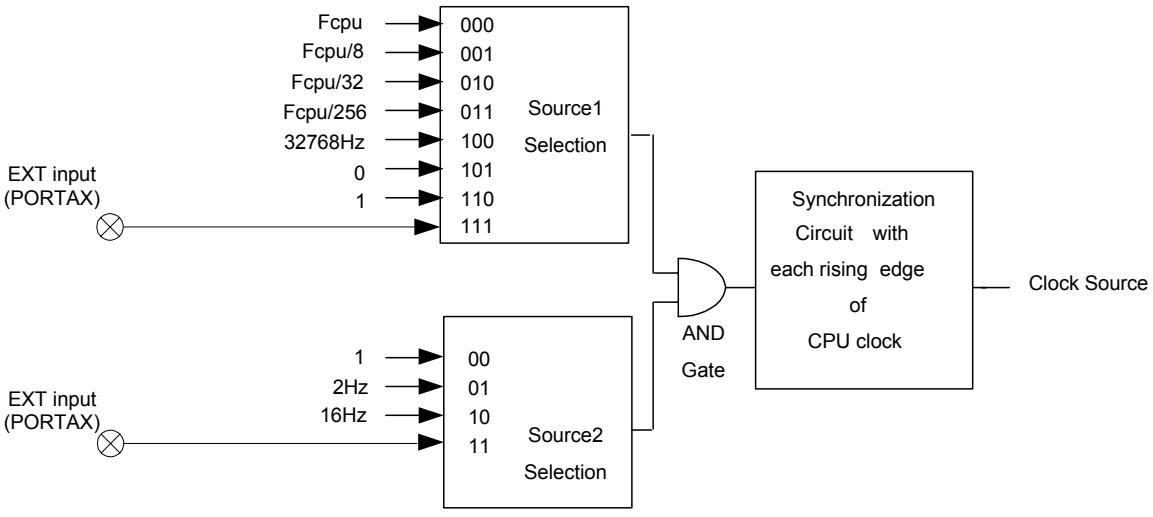
	IOA								IOB							
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Auto Wake up								V								
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
High Sink					V	V	V	V					V	V	V	V
PWMIO													V	V	V	V
IR(Output)									V							
External INT										V						
External Clock		V(TMC)	V(TMB)	V(TMA)												
RTC											V	V				
IIS Out/In	V(out)	V(out)	V(out)			V(in)	V(in)	V(in)								
QD					V(qd2)	V(qd2)	V(qd1)	V(qd1)								
CC		TMC	TMB	TMA						TMC	TMB	TMA				
1M Pull Low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

Note1: QD means quadrature decoder, CC means Capture/Comparison.

	IOC								IOD							
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
ADC	V	V	V	V	V	V	V	V								
SPI													V(rx)	V(tx)	V(ck)	V(cs)
1M pull low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

6.7. Timer/Counter (Timer A/Timer B/Timer C)

Three 12-bit timers are embedded in GPCD9001A, timer A, B and C. These three timers all have 12-bit up counter and a preload register and programmable clock source. Timer A/B can also be the clock source of the software channel 1/2 respectively. The clock source of each timer can be set individually. Two clock sources, including CPU clock and external clock, can be selected individually or their combination to be timer's clock source. Besides, capture and comparison function are supported by TMA . Comparison is supported by TMB and TMC.



6.8. Sleep, Wakeup and Watchdog

6.8.1. Sleep and Wakeup

Sleep mode is to save power by stopping clock while device is not in use. When sleep acts, the device runs from operating mode to standby mode. Wake-up from sleep mode is to turn back to operating mode.

1). Sleep: After power on reset, IC starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock and enter sleep mode.

2). Wake-up: While an IRQ/NMI interrupt signal is generated, GPCD9001A is waking up from sleep mode. While wake-up completed, program counter will continue to execute the next command.

6.8.2. Watchdog

The purpose of watchdog is to monitor system's operation normally. Within a certain period, watchdog must be cleared. It protects the system from incorrect code execution by generating a system reset when software is failed to clear watchdog flag within 0.75 seconds. Watchdog function can be removed by option.

6.9. Speech and DAC

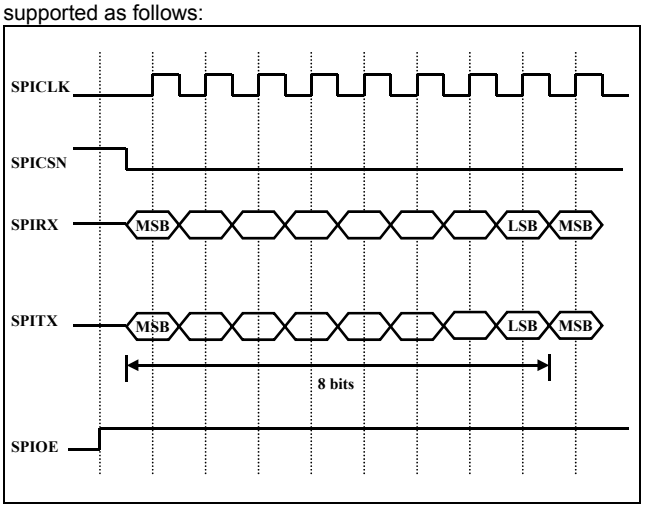
GPCD9001A features a high performance SPU voice engine to achieve 8-channel voice with ADPCM/PCM. The SPU also supports automatic zero-crossing concatenate function. A hardware multiplier is also embedded in this SPU for software usage. The fixed address of RAM area $0000 - $007F is designed as address pointers and a data buffer for the 8 channel speech/melody generation. Moreover, two sets of 14-bit software channel with noise filter are supported. There is one 14-bit DAC with push-pull amplifier for direct audio output.

6.10. Analog/Digital Converter

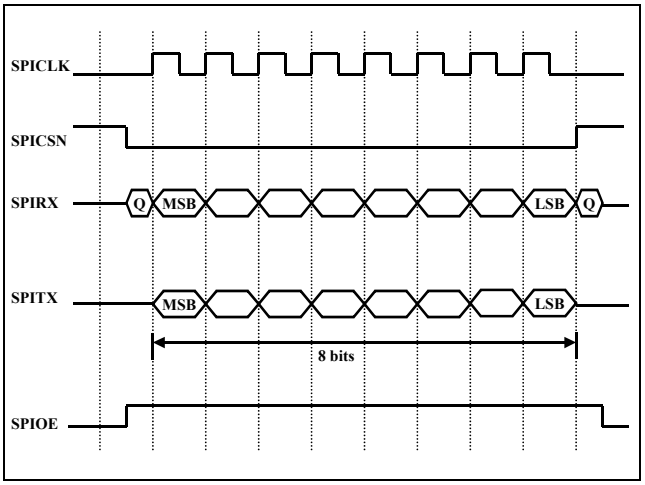
10-bit general purpose analog/digital converter(ADC) is embedded in GPCD9001A. The ADC with 8 channels input can be selected by software programming with maximum 64KHz sampling rate. Key press interrupt generation is supported.

6.11. SPI Controller

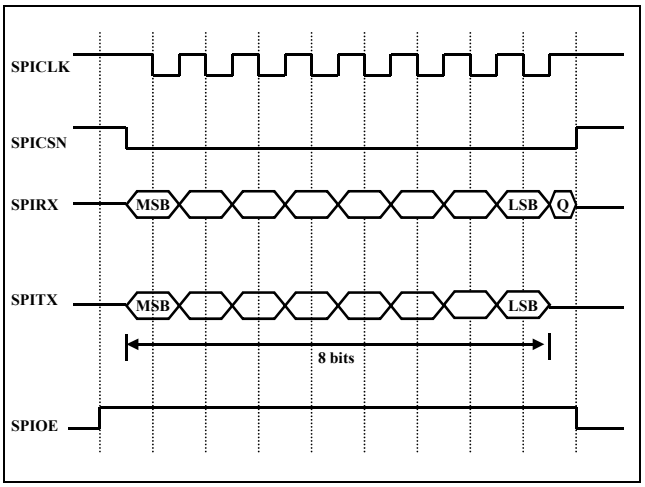
A Serial Peripheral Interface (SPI) controller is built-in GPCD9001A to facilitate communicating with other devices and components. There are four control signals on SPI including SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO); the four signals are shared with PortD0, PortD1, PortD2 and PortD3. While SPI module is enabled by corresponding control bit. These four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of timing are supported as follows:



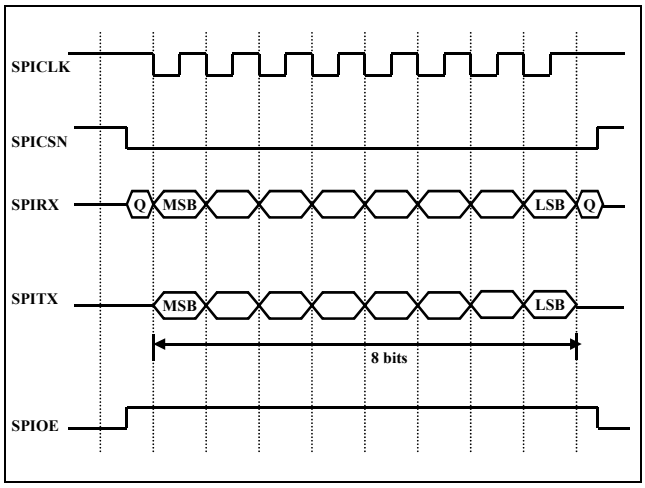
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0



Master Mode, SPO = 1, SPH=1

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2. DC Characteristics (VDD_IO/VDD_ADC/VDD_REG=3.0V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	9.8	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V F_{CPU} = 8MHz , DAC on, no load
Standby Current	I_{STBY}	-	-	10	μA	VDD_IO/VDD_ADC/VDD_REG=3.0V
OSC Frequency	F_{OSC}	-		16	MHz	VDD_IO/VDD_ADC/VDD_REG=3.0V
Input High Level	V_{IH}	0.7*VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3*VDD	V	-
Output High Current (IOA/B/C/D[7:0])	I_{OH}	-	5.0	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OH} =2.7V
Output Sink Current (IOA/B[7:4], IOC/D[7:0])	I_{OL1}	-	5.5	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OL} =0.3V
Output High Sink Current (IOA/B[3:0])	I_{OL2}	-	12.8	-	mA	VDD_IO/VDD_ADC/VDD_REG=3.0V, V_{OL} =0.3V
Input Pull-Low Resistor (IOA/B/C/D[7:0])	R_{PL}	-	1535	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=3.0V, Vin=3.0V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PL}	-	179	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=3.0V, Vin=VSS

7.3. DC Characteristics (VDD_IO/VDD_ADC/VDD_REG=5.0V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	13.6	-	mA	VDD_IO/VDD_ADC/VDD_REG=5.0V F_{CPU} = 8MHz , DAC on, no load
Standby Current	I_{STBY}	-	-	10	μA	VDD_IO/VDD_ADC/VDD_REG=5.0V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDD_IO/VDD_ADC/VDD_REG=5.0V
Input High Level	V_{IH}	0.7*VDD	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3*VDD	V	-
Output High Current (IOA/B/C/D[7:0])	I_{OH}	-	11.7	-	mA	VDD_IO/VDD_ADC/VDD_REG=5.0V, V_{OH} =4.5V
Output Sink Current (IOA/B[7:4], IOC/D[7:0])	I_{OL1}	-	12.7	-	mA	VDD_IO/VDD_ADC/VDD_REG=5.0V, V_{OL} =0.5V

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output High Sink Current (IOA/B[3:0])	I_{OL2}	-	28.5	-	mA	VDD_IO/VDD_ADC/VDD_REG=5.0V, V_{OL} =0.5V
Input Pull-Low Resistor (IOA/B/C/D[7:0])	R_{PL}	-	825	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=5.0V, Vin=5.0V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PL}	-	96	-	Kohm	VDD_IO/VDD_ADC/VDD_REG=5.0V, Vin=VSS

7.4. DAC Characteristics (VDD_IO/VDD_ADC/VDD_REG/VDD_DAC=3.0V, no load, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
Noise at No Signal	-	-	-77.6	-	dBr A
Dynamic Range(-60dB)	-	-	-74	-	dBr A

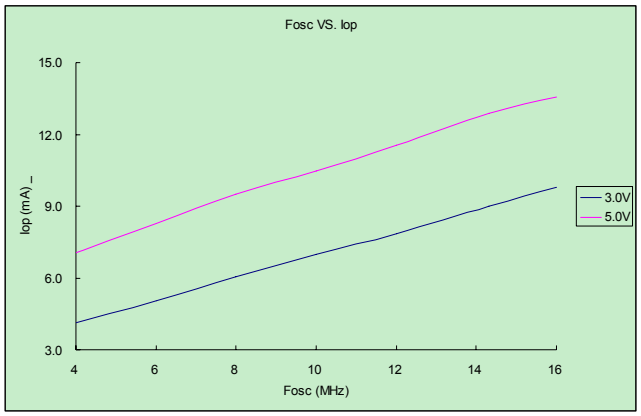
7.5. Regulator Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.4	4.5	5.5	V
Maximum Current Output	IREGO	-	-	30	mA
Output Voltage	VREGO	2.4	3.3	3.6	V
Standby Current	IREGS	-	5	-	uA

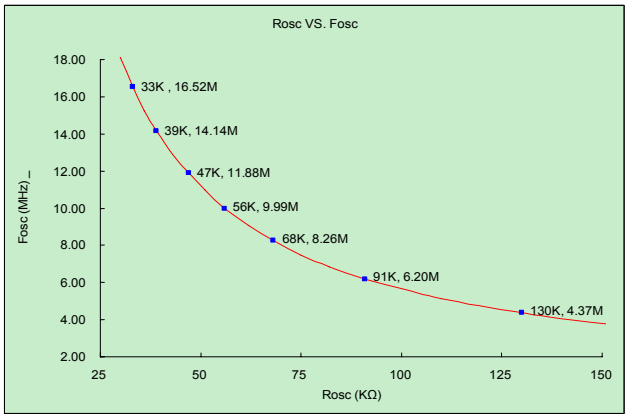
7.6. ADC Characteristics (VDD_IO/VDD_ADC/VDD_REG/VDD_DAC=3.0V, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
ADC Resolution	RESO	-	-	10	bits
Signal-to-Noise Plus Distortion of ADC from Line-in	SINAD	-	-60	-	dB
Effective Number of Bit	ENOB	-	9.7	-	bits
Integral Non-linearity of ADC	INL	-	±1.0	-	LSB
Differential Non-linearity of ADC	DNL	-	±0.6	-	LSB
No Missing Code	-	-	9	-	bits
AD Conversion Rate	F_{CONV}	-	-	100K	Hz
Supply Voltage	VADC	2.4	4.5	5.5	V

7.7. F_{osc} vs. Iop(TA=25℃)

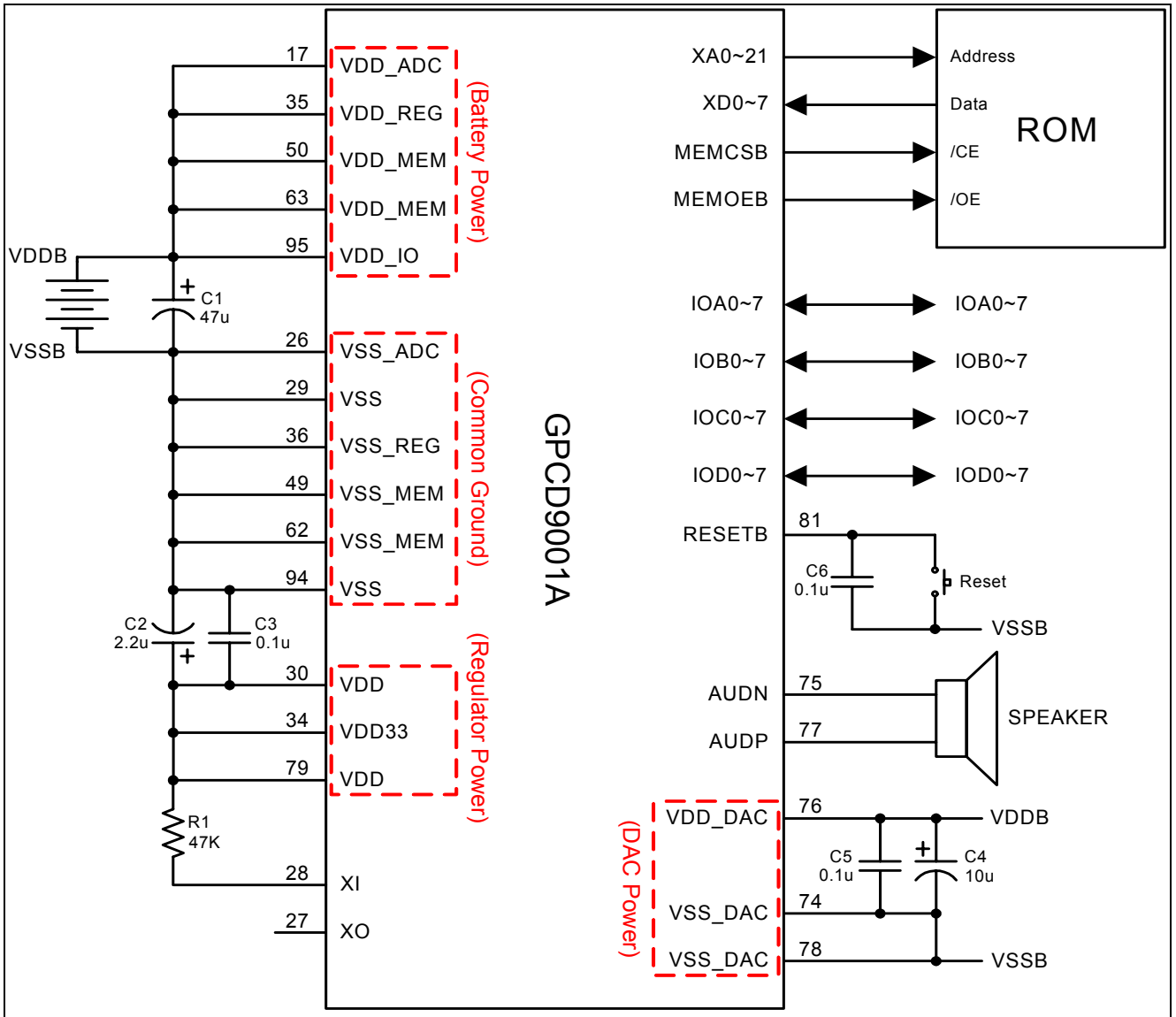


7.8. R_{osc} vs. F_{osc}(TA=25℃)



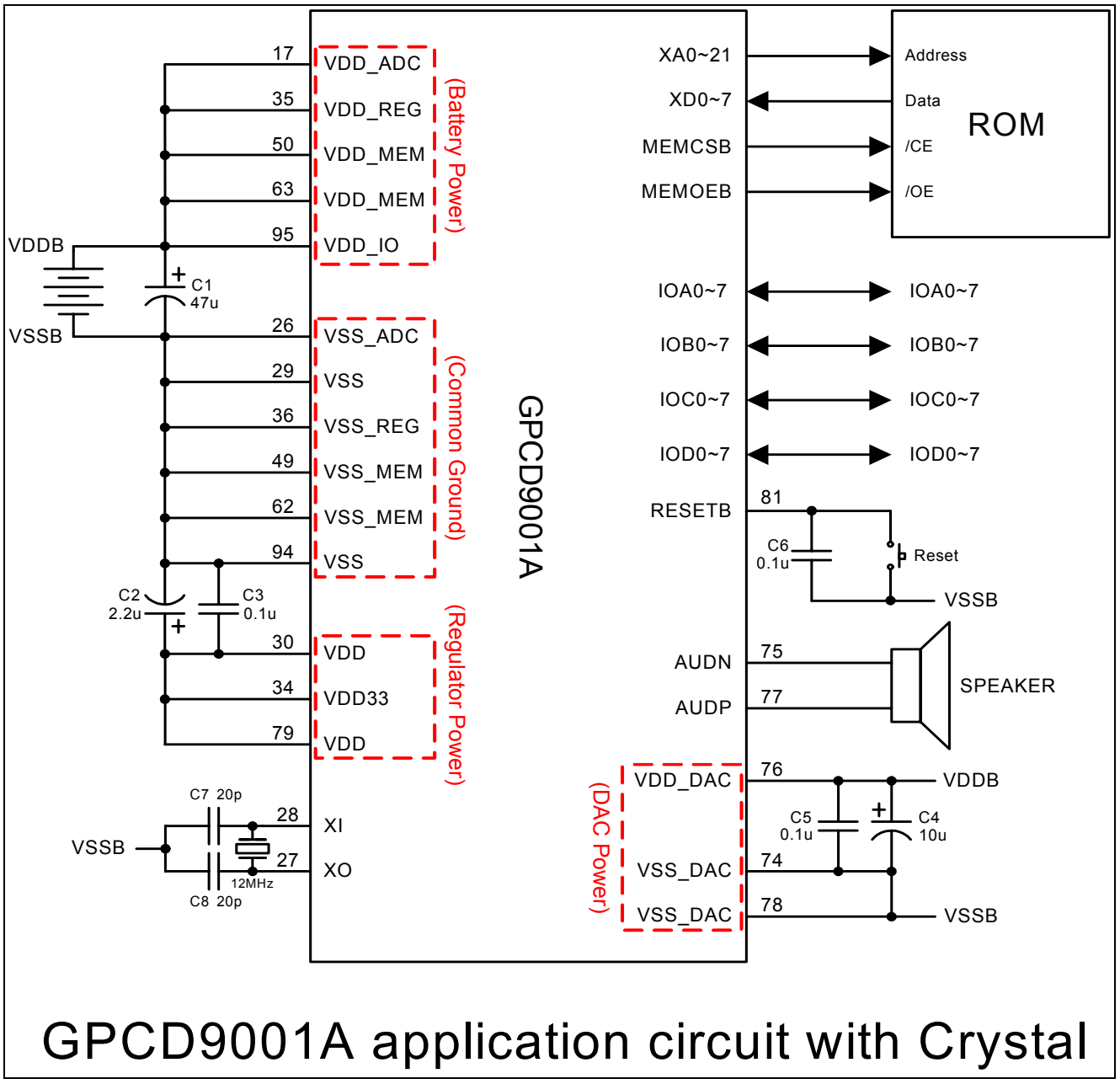
8. APPLICATION CIRCUITS

8.1. GPCD9001A Application Circuit with R_{OSC} Option



GPCD9001A application circuit with Rosc

8.2. GPCD9001A Application Circuit with Crystal Option



GPCD9001A application circuit with Crystal

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCD9001A-NnnV-C	Chip form
GPCD9001A-NnnV-HL09x	Green Package - LQFP128

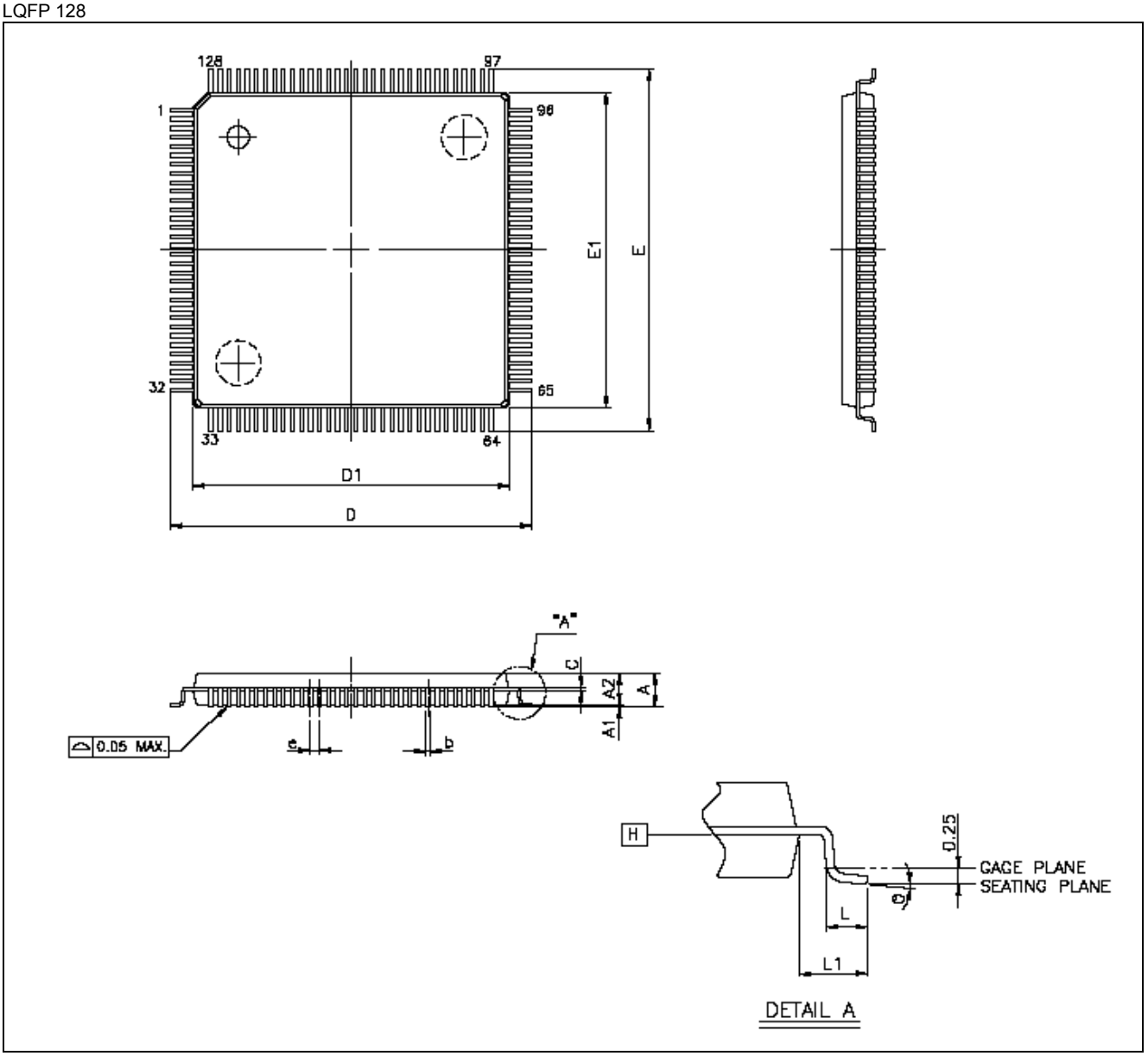
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP 128



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	16.00 BCS.		
D1	14.00 BCS.		
E	16.00 BCS.		
E1	14.00 BCS.		
e	0.40 BCS.		
θ	0°	3.5°	7°
b	0.13	0.16	0.23
c	0.09	-	0.20

Symbol	Millimeter		
	Min.	Nom.	Max.
L	0.45	0.60	0.75
L1	1.00 REF		

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 06, 2011	0.3	1. Modify 5. Signal Description	5
NOV. 18, 2009	0.2	1. Datasheet updated, including DC characteristics. 2. Change product name from GPCD8001A to GPCD9001A.	
JUN. 29, 2009	0.1	Original	19