Low Power, Pseudo Differential, 100 kSPS 12-Bit ADC in an 8-Lead SOT-23

AD7457

FEATURES

Specified for V_{DD} of 2.7 V to 5.25 V
Low power:
0.9 mW max at 100 kSPS with V_{DD} = 3 V
3 mW max at 100 kSPS with V_{DD} = 5 V
Pseudo differential analog input
Wide input bandwidth:
70 dB SINAD at 30 kHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface—SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
Automatic power-down mode
8-lead SOT-23 package

APPLICATIONS

Transducer interface
Battery-powered systems
Data acquisition systems
Portable instrumentation

FUNCTIONAL BLOCK DIAGRAM

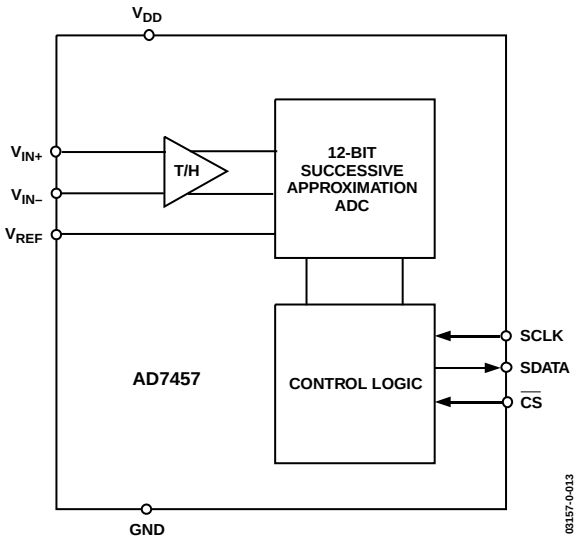


Figure 1.

GENERAL DESCRIPTION

The AD7457 is a 12-bit, low power, successive approximation (SAR) analog-to-digital converter that features a pseudo differential analog input. This part operates from a single 2.7 V to 5.25 V power supply and features throughput rates of up to 100 kSPS.

The part contains a low noise, wide bandwidth, differential track-and-hold (T/H) amplifier that can handle input frequencies in excess of 1 MHz. The reference voltage for the AD7457 is applied externally to the V_{REF} pin and can range from 100 mV to V_{DD}, depending on what suits the application.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the device to interface with microprocessors or DSPs. The SAR architecture of this part ensures that there are no pipeline delays.

The AD7457 uses advanced design techniques to achieve very low power dissipation.

PRODUCT HIGHLIGHTS

1. Operation with 2.7 V to 5.25 V power supplies.
2. Low power consumption. With a 3 V supply, the AD7457 offers 0.9 mW maximum power consumption for a 100 kSPS throughput rate.
3. Pseudo differential analog input.
4. Flexible power/serial clock speed management. The conversion rate is determined by the serial clock, allowing the power to be reduced as the conversion time is reduced through the serial clock speed increase. Automatic power-down after conversion allows the average power consumption to be reduced.
5. Variable voltage reference input.
6. No pipeline delays.
7. Accurate control of the sampling instant via the $\overline{CS}$ input and once-off conversion control.
8. ENOB > 10 bits typically with 500 mV reference.

Rev. A
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AD7457* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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DOCUMENTATION

Data Sheet

- AD7457: Low Power, Pseudo Differential, 100 kSPS 12-Bit ADC in 8-Lead SOT-23 Data Sheet

Product Highlight

- 8- to 18-Bit SAR ADCs ... From the Leader in High Performance Analog

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7457 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7457 EngineerZone Discussions.

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REVISION HISTORY

2/05—Rev. 0 to Rev. A

Changes to Table 3 ... 6
Changes to Ordering Guide ... 17

10/03—Rev. 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 10 MHz, f_S = 100 kSPS, V_{REF} = 2.5 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	B Version[1]	Unit
DYNAMIC PERFORMANCE	f_{IN} = 30 kHz		
Signal to Noise Ratio (SNR)[2]		71	dB min
Signal to (Noise + Distortion) (SINAD)[2]		70	dB min
Total Harmonic Distortion (THD)[2]	−84 dB typ	−75	dB max
Peak Harmonic or Spurious Noise[2]	−86 dB typ	−75	dB max
Intermodulation Distortion (IMD)[2]	fa = 25 kHz; fb = 35 kHz		
Second-Order Terms		−80	dB typ
Third-Order Terms		−80	dB typ
Aperture Delay[2]		5	ns typ
Aperture Jitter[2]		50	ps typ
Full-Power Bandwidth[2, 3]	@ −3 dB	20	MHz typ
	@ −0.1 dB	2.5	MHz typ
DC ACCURACY			
Resolution		12	Bits
Integral Nonlinearity (INL)[2]		±1	LSB max
Differential Nonlinearity (DNL)[2]	Guaranteed no missed codes to 12 bits	±0.95	LSB max
Offset Error[2]		±4.5	LSB max
Gain Error[2]		±2	LSB max
ANALOG INPUT			
Full-Scale Input Span	$V_{IN+} - V_{IN-}$	V_{REF}	V
Absolute Input Voltage			
V_{IN+}		V_{REF}	V
V_{IN-}[4]	V_{DD} = 2.7 V to 3.6 V	−0.1 to +0.4	V
	V_{DD} = 4.75 V to 5.25 V	−0.1 to +1.5	V
DC Leakage Current		±1	µA max
Input Capacitance	When in track/hold	30/10	pF typ
REFERENCE INPUT			
V_{REF} Input Voltage[5]	±1% tolerance for specified performance	2.5	V
DC Leakage Current		±1	µA max
V_{REF} Input Capacitance	When in track/hold	10/30	pF typ
LOGIC INPUTS			
Input High Voltage, V_{INH}		2.4	V min
Input Low Voltage, V_{INL}		0.8	V max
Input Current, I_{IN}	Typically 10 nA, V_{IN} = 0 V or V_{DD}	±1	µA max
Input Capacitance, C_{IN}[6]		10	pF max
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} = 4.75 V to 5.25 V, I_{SOURCE} = 200 µA	2.8	V min
	V_{DD} = 2.7 V to 3.6 V, I_{SOURCE} = 200 µA	2.4	V min
Output Low Voltage, V_{OL}	I_{SINK} = 200 µA	0.4	V max
Floating-State Leakage Current		±1	µA max
Floating-State Output Capacitance[6]		10	pF max
Output Coding		Straight natural binary	
CONVERSION RATE			
Conversion Time	1.6 µs with a 10 MHz SCLK	16	SCLK cycles
Track-and-Hold Acquisition Time[2]		1	µs max
Throughput Rate	See the Serial Interface section	100	kSPS max

Parameter	Test Conditions/Comments	B Version[1]	Unit
POWER REQUIREMENTS			
V_{DD}		2.7/5.25	V min/max
I_{DD}[7, 8]			
During Conversion[6]	V_{DD} = 4.75 V to 5.25 V	1.5	mA max
	V_{DD} = 2.7 V to 3.6 V	1.2	mA max
Normal Mode (Static)	SCLK on or off	0.5	mA typ
Normal Mode (Operational)	V_{DD} = 4.75 V to 5.25 V	0.7	mA max
	V_{DD}= 2.7 V to 3.6 V	0.33	mA max
Power-Down	SCLK on or off	1	µA max
Power Dissipation			
Normal Mode (Operational)	V_{DD} = 5 V	3	mW max
	V_{DD} = 3 V	0.9	mW max
Power-Down	V_{DD} = 5 V; SCLK on or off	5	µW max
	V_{DD} = 3 V; SCLK on or off	3	µW max

[1] Temperature range for B version: −40°C to +85°C.
[2] See the Terminology section.
[3] Analog inputs with slew rates exceeding 27 V/µs (full-scale input sine wave > 3.5 MHz) within the acquisition time may cause an incorrect result to be returned by the converter.
[4] A dc input is applied to V_{IN-} to provide a pseudo ground for V_{IN+}.
[5] The AD7457 is functional with a reference input range of 100 mV to V_{DD}.
[6] Guaranteed by characterization.
[7] See the Power Consumption section.
[8] Measured with a full-scale dc input.

TIMING SPECIFICATIONS[1]

V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 10 MHz, f_S = 100 kSPS, V_{REF} = 2.5 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}[2]	10	kHz min	
	10	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}		t_{SCLK} = 1/f_{SCLK}
	1.6	µs max	
t_2	10	ns min	$\overline{CS}$ rising edge to SCLK falling edge setup time
t_3[3]	20	ns max	Delay from $\overline{CS}$ rising edge until SDATA three-state disabled
t_4[3]	40	ns max	Data access time after SCLK falling edge
t_5	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_6	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_7	10	ns min	SCLK edge to data valid hold time
t_8[4]	10	ns min	SCLK falling edge to SDATA three-state enabled
	35	ns max	SCLK falling edge to SDATA three-state enabled
$t_{POWER-UP}$[5]	1	µs max	Power-up time from full power-down
$t_{POWER-DOWN}$	7.4	µs min	Minimum time spent in power-down

[1] The timing specifications are guaranteed by characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. See Figure 2 and the Serial Interface section.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V with V_{DD} = 5 V, and the time required for the output to cross 0.4 V or 2.0 V for V_{DD} = 3 V.
[4] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[5] See the Power Consumption section.

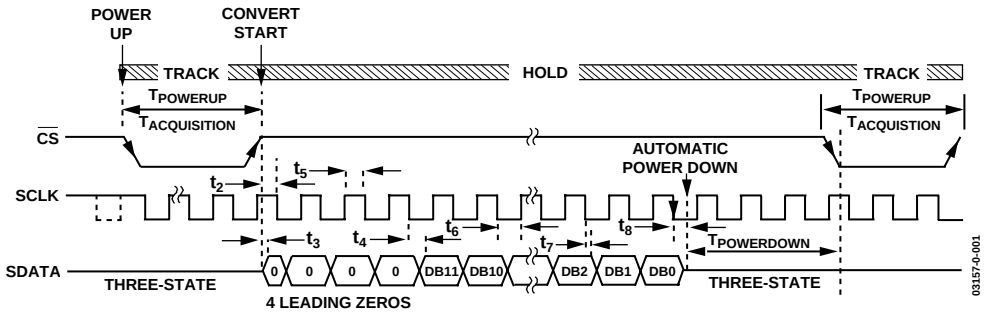


Figure 2. AD7457 Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{IN+} to GND	−0.3 V to V_{DD} + 0.3 V
V_{IN-} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	211.5°C/W (SOT-23)
θ_{JC} Thermal Impedance	91.99°C/W (SOT-23)
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Pb-Free Temperature, Soldering	
Reflow	260(+0)°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

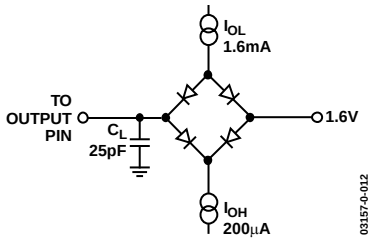


Figure 3. Load Circuit for Digital Output Timing Specifications

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

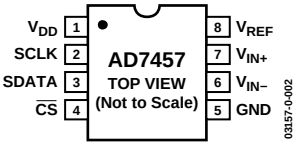


Figure 4. 8-Lead SOT-23 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. V_{DD} is 2.7 V to 5.25 V. This supply should be decoupled to GND with a 0.1 µF capacitor and a 10 µF tantalum capacitor.
2	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process.
3	SDATA	Serial Data. Logic output. The conversion result from the AD7457 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7457 consists of four leading zeros followed by the 12 bits of conversion data that are provided MSB first. The output coding is straight (natural) binary.
4	$\overline{CS}$	Chip Select. This input provides the dual function of powering up the device and initiating a conversion on the AD7457.
5	GND	Analog Ground. Ground reference point for all circuitry on the AD7457. All analog input signals and any external reference signal should be referred to this GND voltage.
6	V_{IN-}	Inverting Input. This pin sets the ground reference point for the V_{IN+} input. Connect to ground or to a dc offset to provide a pseudo ground.
7	V_{IN+}	Noninverting Analog Input.
8	V_{REF}	Reference Input for the AD7457. An external reference in the range 100 mV to V_{DD} must be applied to this input. The specified reference input is 2.5 V. This pin should be decoupled to GND with a capacitor of at least 0.33 µF.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, f_S = 100 kSPS, f_{SCLK} = 10 MHz, V_{DD} = 2.7 V to 5.25 V, V_{REF} = 2.5 V, unless otherwise noted.

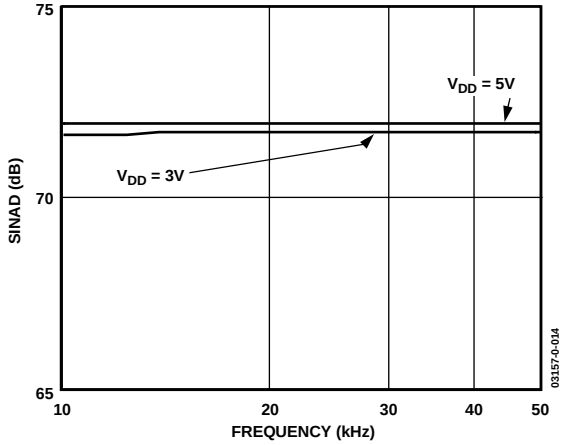


Figure 5. SINAD vs. Analog Input Frequency for V_{DD} = 3 V and 5 V

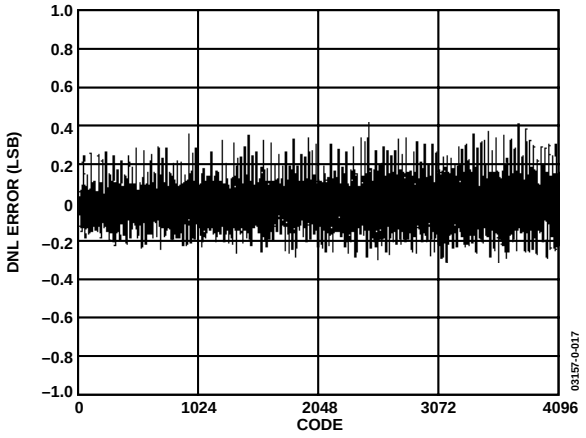


Figure 8. Typical DNL for the AD7457 for V_{DD} = 5 V

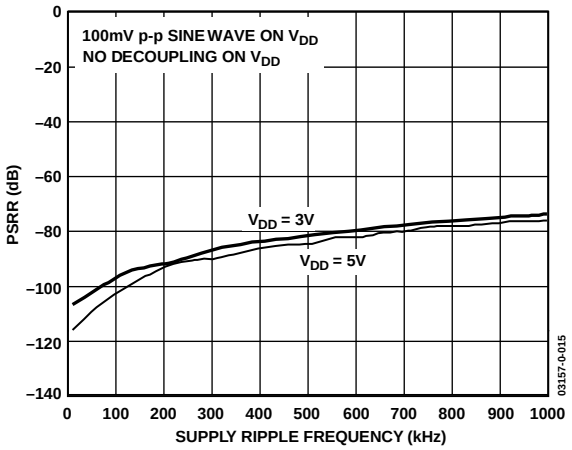


Figure 6. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

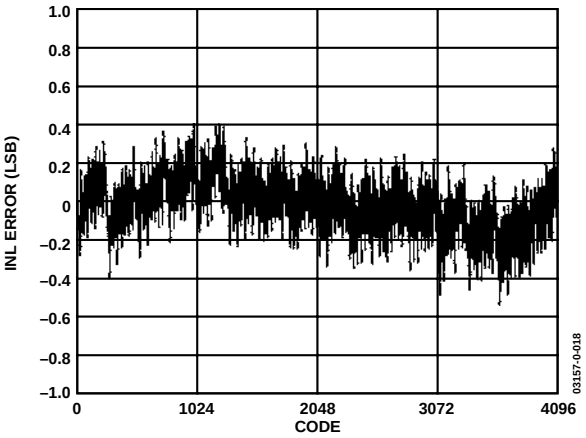


Figure 9. Typical INL for the AD7457 for V_{DD} = 5 V

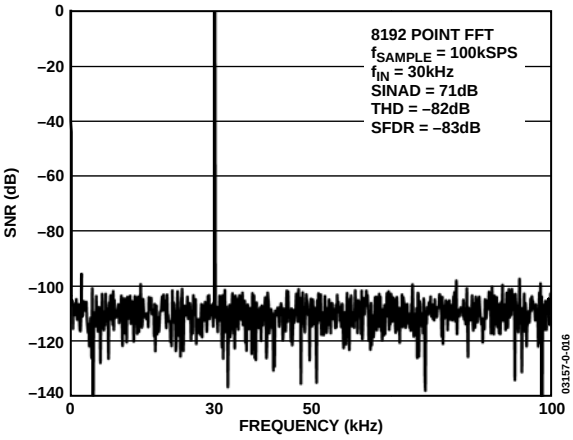


Figure 7. Dynamic Performance for V_{DD} = 5 V

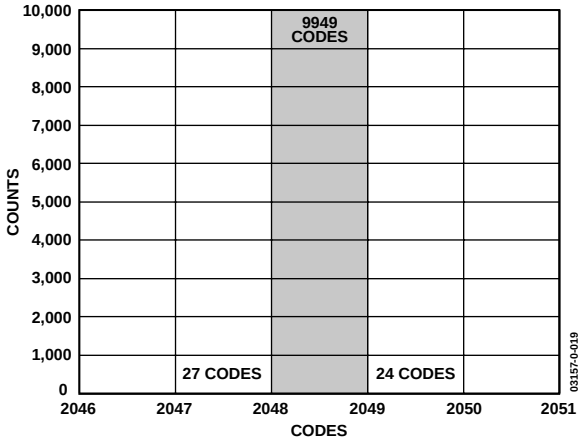


Figure 10. Histogram of 10,000 Conversions of a DC Input

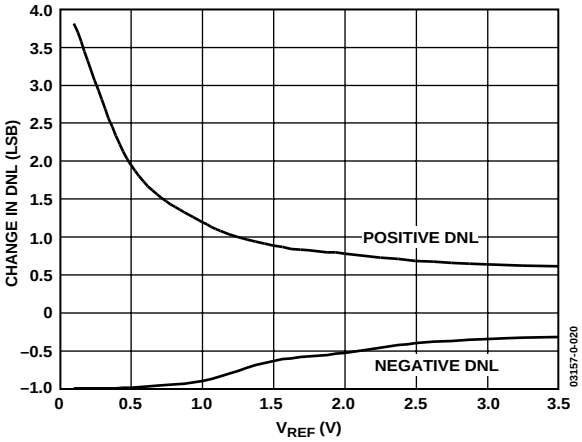


Figure 11. Changes in DNL vs. V_{REF} for V_{DD} = 5 V

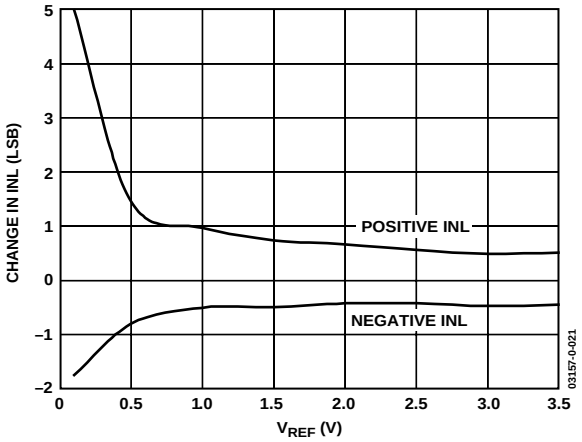


Figure 12. Change in INL vs. V_{REF} for V_{DD} = 5 V

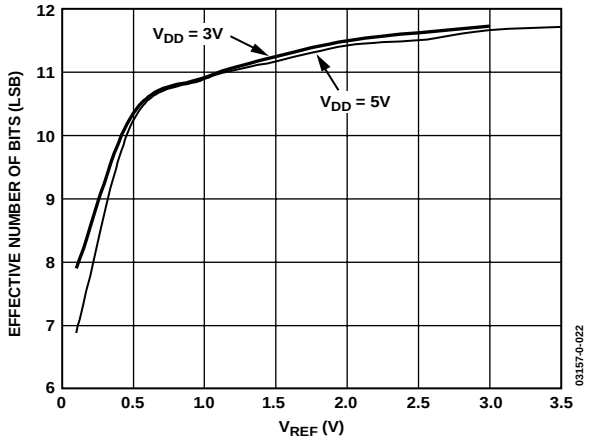


Figure 13. ENOB vs. V_{REF} for V_{DD} = 3 V and 5 V

TERMINOLOGY

Signal to (Noise + Distortion) Ratio (SINAD)
The measured ratio of SINAD at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\left(Noise + Distortion\right) = \left(6.02\ N + 1.76\right)\text{dB}$$

Therefore, for a 12-bit converter, the SINAD is 74 dB.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7457, it is defined as

$$THD\left(\text{dB}\right) = 20\ log\ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.

V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but, for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7457 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately.

The calculation of the intermodulation distortion is as per the total harmonic distortion specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

Aperture Delay
The amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter
The sample-to-sample variation in the effective point in time at which the actual sample is taken.

Full-Power Bandwidth
The full-power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (000...000 to 000...001) from the ideal (that is, AGND + 1 LSB).

Gain Error
The deviation of the last code transition (111...110 to 111...111) from the ideal (that is, V_{REF} − 1 LSB), after the offset error has been adjusted out.

Track-and-Hold Acquisition Time
The minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

Power Supply Rejection Ratio (PSRR)
The ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC V_{DD} supply of frequency fs. The frequency of this input varies from 1 kHz to 1 MHz.

$$PSRR(\text{dB}) = 10\log(Pf/Pfs)$$

Pf is the power at frequency *f* in the ADC output; *Pfs* is the power at frequency *fs* in the ADC output.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7457 is a 12-bit, low power, single supply, successive approximation analog-to-digital converter (ADC) with a pseudo differential analog input. It operates with a single 2.7 V to 5.25 V power supply and is capable of throughput rates up to 100 kSPS. It requires an external reference to be applied to the V_{REF} pin.

The AD7457 has an on-chip differential track-and-hold amplifier, a successive approximation (SAR) ADC, and a serial interface housed in an 8-lead SOT-23 package. The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The AD7457 automatically powers down after conversion, resulting in low power consumption.

CONVERTER OPERATION

The AD7457 is a successive approximation ADC based around two capacitive DACs. Figure 14 and Figure 15 show simplified schematics of the ADC in the acquisition phase and the conversion phase, respectively. The ADC is comprised of control logic, a SAR, and two capacitive DACs. In Figure 14 (acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

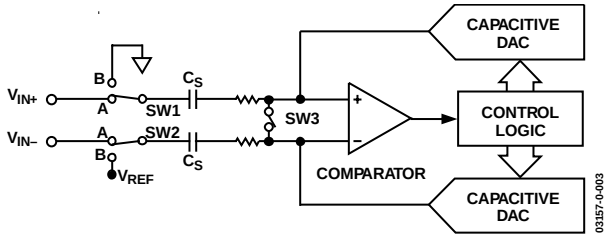


Figure 14. ADC Acquisition Phase

When the ADC starts a conversion (Figure 15), SW3 opens, and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC's output code. The output impedances of the sources driving the V_{IN+} and the V_{IN-} pins must be matched; otherwise the two inputs have different settling times, resulting in errors.

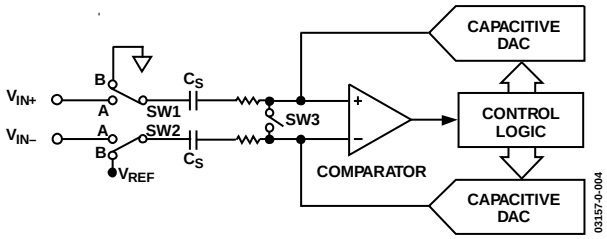


Figure 15. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding for the AD7457 is straight (natural) binary. The designed code transitions occur at successive LSB values (1 LSB, 2 LSB, and so on). The LSB size is $V_{REF}/4096$. The ideal transfer characteristics of the AD7457 are shown in Figure 16.

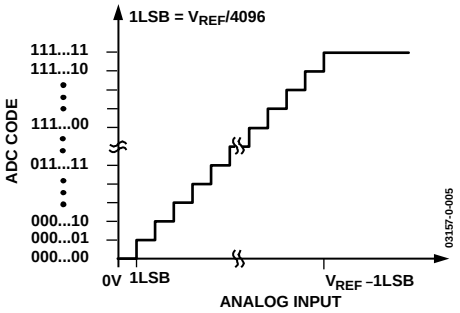


Figure 16. Ideal Transfer Characteristics

TYPICAL CONNECTION DIAGRAM

Figure 17 shows a typical connection diagram for the AD7457. In this setup, the GND pin is connected to the analog ground plane of the system. The V_{REF} pin is connected to the AD780, a 2.5 V decoupled reference source. The signal source is connected to the V_{IN+} analog input via a unity gain buffer. A dc voltage is connected to the V_{IN-} pin to provide a pseudo ground for the V_{IN+} input. The V_{DD} pin should be decoupled to AGND with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor. The reference pin should be decoupled to AGND with a capacitor of at least 0.33 µF. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit result.

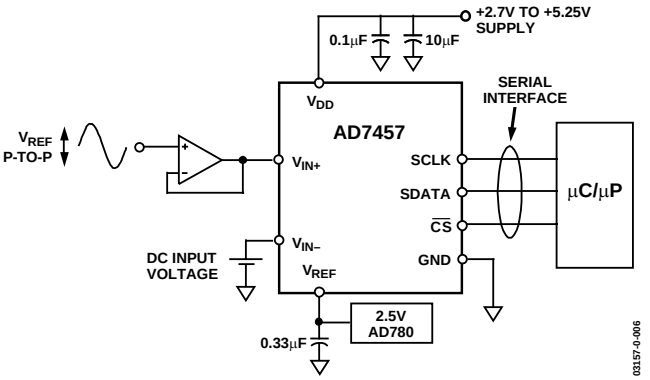


Figure 17. Typical Connection Diagram

ANALOG INPUT

The AD7457 has a pseudo differential analog input. The V_{IN+} input is coupled to the signal source and should have an amplitude of V_{REF} p-p to make use of the full dynamic range of the part. A dc input is applied to the V_{IN-}. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. Ensure that (V_{IN-} + V_{IN+}) is less than or equal to V_{DD} to avoid exceeding the maximum ratings of the ADC. The main benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC's ground, allowing dc common-mode voltages to be canceled.

Because the ADC operates from a single supply, it is necessary to level shift ground-based bipolar signals to comply with the input requirements. An op amp (for example, the AD8021) can be configured to rescale and level shift a ground-based (bipolar) signal, so that it is compatible with the input range of the AD7457. See Figure 18.

When a conversion takes place, the pseudo ground corresponds to 0 and the maximum analog input corresponds to 4096.

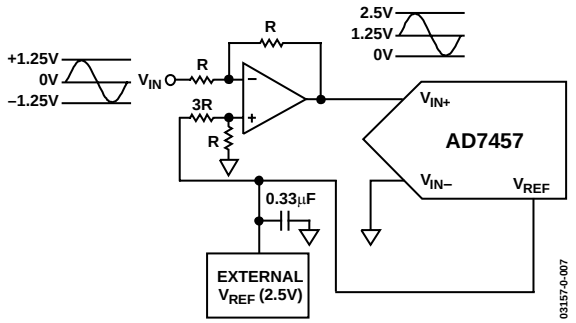


Figure 18. Op Amp Configuration to Level Shift a Bipolar Input Signal

ANALOG INPUT STRUCTURE

Figure 19 shows the equivalent circuit of the analog input structure of the AD7457. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV, which causes these diodes to become forward biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part. Typically, the C1 capacitors in Figure 19 are 4 pF and can be attributed primarily to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The capacitors, C2, are the ADC's sampling capacitors, which typically have a capacitance of 16 pF.

For ac applications, removing high frequency components from the analog input signal through the use of an RC low pass filter on the relevant analog input pins is recommended. In applications where harmonic distortion and the signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances can significantly affect the ac performance of the ADC, which may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

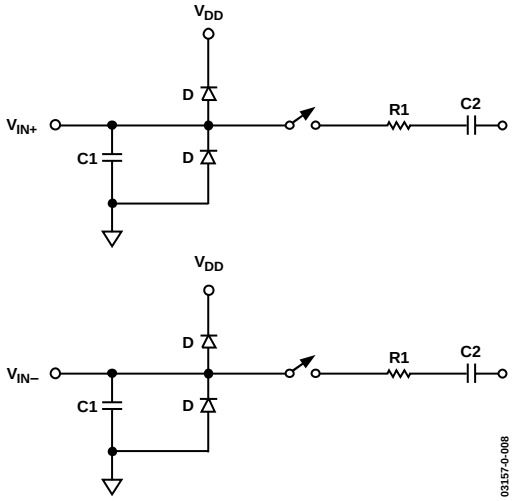


Figure 19. Equivalent Analog Input Circuit
(Conversion Phase, Switches Open; Track Phase, Switches Closed)

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 20 shows a graph of the THD vs. analog input signal frequency for different source impedances.

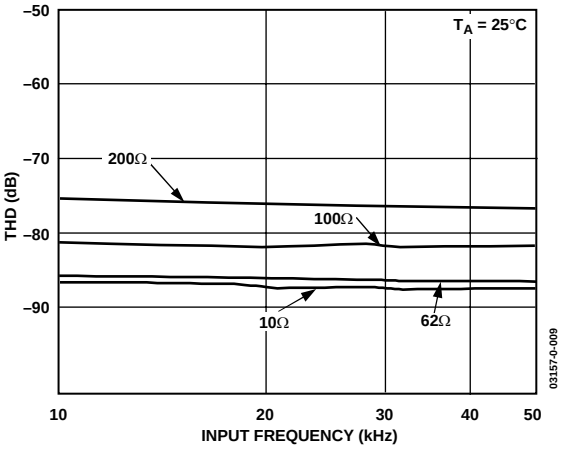


Figure 20. THD vs. Analog Input Frequency for Various Source Impedances

Figure 21 shows a graph of THD vs. analog input frequency for various supply voltages, while sampling at 100 kSPS with an SCLK of 10 MHz. In this case, the source impedance is 10 Ω.

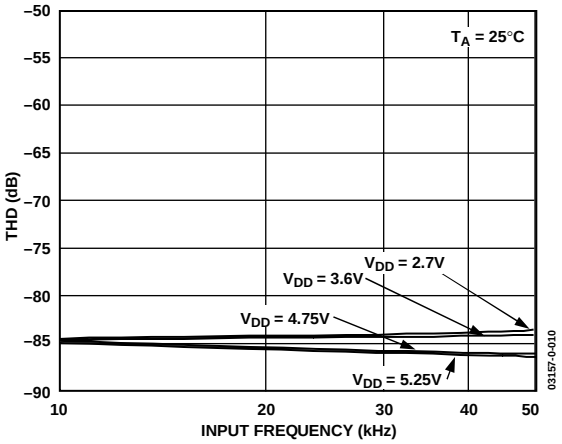


Figure 21. THD vs. Analog Input Frequency for Various Supply Voltages

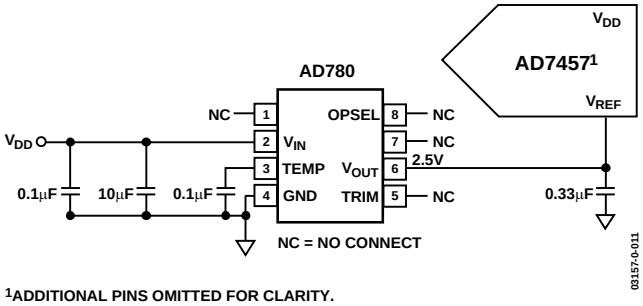
DIGITAL INPUTS

The digital inputs applied to the AD7457 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied, that is, $\overline{CS}$ and SCLK, can go to 7 V and are not restricted by the V_{DD} + 0.3 V limits as on the analog input.

The main advantage of the inputs not being restricted to the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before V_{DD}, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to V_{DD}.

REFERENCE SECTION

An external source is required to supply the reference to the AD7457. This reference input can range from 100 mV to V_{DD}. The specified reference is 2.50 V for the power supply range 2.70 V to 5.25 V. Errors in the reference source result in gain errors in the AD7457 transfer function. A capacitor of at least 0.33 µF should be placed on the V_{REF} pin. Suitable reference sources for the AD7457 include the AD780 and the ADR421. Figure 22 shows a typical connection diagram for the V_{REF} pin.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 22. Typical V_{REF} Connection Diagram for V_{DD} = 5 V

SERIAL INTERFACE

Figure 2 shows a detailed timing diagram of the serial interface of the AD7457. The serial clock provides the conversion clock and also controls the transfer of data from the device during conversions.

The falling edge of $\overline{CS}$ powers up the AD7457 and also puts the track-and-hold into track. Power-up time is 1 µs minimum and, in this time, the device also acquires the analog input signal. $\overline{CS}$ must remain low for the duration of power-up. The rising edge of $\overline{CS}$ initiates the conversion process, puts the track-and-hold into hold mode, and takes the serial data bus out of three-state. The conversion requires 16 SCLK cycles to complete.

On the sixteenth SCLK falling edge, after the time t_8, the serial data bus goes back into three-state and the device automatically enters full power-down. It remains in power-down until the next falling edge of $\overline{CS}$. For specified performance, the throughput rate should not exceed 100 kSPS, which means that there should be no less than 10 µs between consecutive $\overline{CS}$ falling edges.

The conversion result from the AD7457 is provided on the SDATA output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream of the AD7457 consists of four leading zeros, followed by the 12 bits of conversion data that are provided MSB first. The output coding is straight (natural) binary.

Sixteen serial clock cycles are, therefore, required to perform a conversion and to access data from the AD7457. A rising edge of $\overline{CS}$ provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out on the subsequent SCLK falling edges, beginning with the second leading zero. Thus, the first falling clock edge on the serial clock after $\overline{CS}$ has gone high provides the second leading zero. The final bit in the data transfer, before the device goes into power-down, is valid on the sixteenth falling edge of SCLK, having been clocked out on the previous (fifteenth) falling edge.

In applications with a slow SCLK, it is possible to read in data on each SCLK rising edge. In this case, the first falling edge of SCLK after the $\overline{CS}$ rising edge clocks out the second leading zero and can be read in on the following rising edge. If the first SCLK edge after the $\overline{CS}$ rising edge is a falling edge, the first leading zero that was clocked out when $\overline{CS}$ went high is missed, unless it was not read on the first SCLK falling edge. The fifteenth falling edge of SCLK clocks out the last bit of data, which can be read in by the following rising SCLK edge.

POWER CONSUMPTION

The AD7457 automatically enters power-down at the end of each conversion. When in the power-down mode, all analog circuitry is powered down and the current consumption is 1 μA. To achieve the specified power consumption (which is the lowest), there are a few things the user should keep in mind.

The conversion time of the device is determined by the serial clock frequency. The faster the SCLK frequency, the shorter the conversion time. Therefore, as the clock frequency used is increased, the ADC is dissipating power for a shorter period of time (during conversion) and it remains in power-down for a longer percentage of the cycle time or throughput rate. This can be seen in Figure 23, which shows typical I_{DD} vs. SCLK frequency for V_{DD} of 3 V and 5 V, when operating the device at the maximum throughput of 100 kSPS.

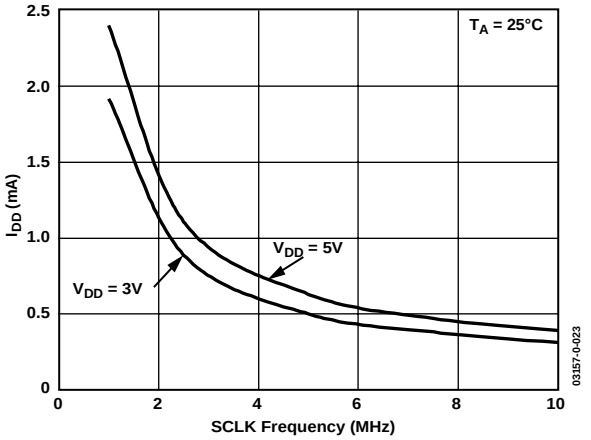


Figure 23. I_{DD} vs. SCLK Frequency for V_{DD} = 3 V and 5 V when Operating at 100 kSPS

Figure 24 shows typical power consumption vs. throughput rate for the maximum SCLK frequency of 10 MHz. In this case, the conversion time is the same for all throughputs, because the SCLK frequency is fixed. As the throughput rate decreases, the average power consumption decreases, because the ADC spends more time in power-down.

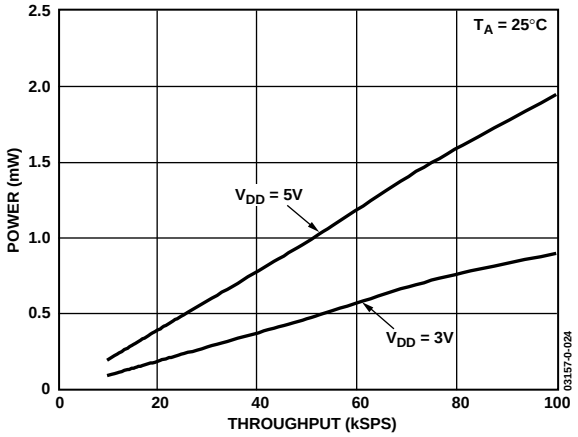


Figure 24. Power vs. Throughput Rate for SCLK = 10 MHz for V_{DD} = 3 V and 5 V

MICROPROCESSOR INTERFACING

The serial interface of the AD7457 allows the part to be connected to a range of different microprocessors. This section explains how to interface the AD7457 with the ADSP-218x serial interface.

AD7457 to ADSP-218x

The ADSP-218x family of DSPs can be interfaced directly to the AD7457 without any glue logic. The serial clock for the ADC is provided by the DSP. SDATA from the ADC is connected to the data receive (DR) input of the serial port and $\overline{CS}$ can be controlled by a flag (FL0). The connection diagram is shown in Figure 25.

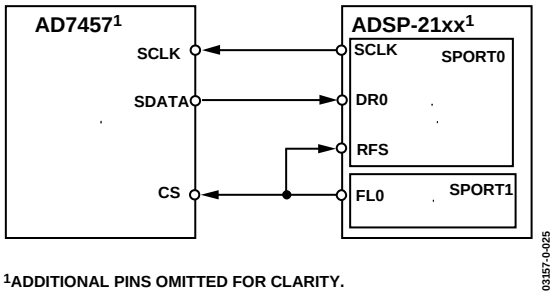


Figure 25. AD7457 to ADSP-218x

SPORT0 must be enabled to receive the conversion data and to provide the SCLK, while SPORT1 must be configured for flags and so on.

Table 5. SPORT0 Configuration

Bit	Setting	Comment/Description
ISCLK	1	Serial clock is generated internally
SLEN	1111	16 bits of conversion data
RFSR	0	Receive frame sync required every word
TFSR	Don't care	Not used
IRFS	0	RFS is set to be an input and is generated externally.
ITFS	Don't care	Not used
RFSW	1	Alternate receive framing
TFSW	Don't care	Not used
INVRFS	0	RFS is active high
INVTFS	Don't care	Not used

SPORT0 is configured by setting the bits in its control register, as listed in Table 5.

The flag to generate the $\overline{CS}$ signal is generated by SPORT1. It is connected to both the ADC and the RFS input of SPORT0 to provide the frame sync signal for the DSP.

APPLICATION HINTS

GROUNDING AND LAYOUT

The printed circuit board that houses the AD7457 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes, because it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close as possible to the GND pin on the AD7457.

Avoid running digital lines under the device, because this couples noise onto the die. The analog ground plane should be allowed to run under the AD7457 to avoid noise coupling. The power supply lines to the AD7457 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A micro strip technique is the best, but is not always possible with a double-sided board.

In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side. Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum capacitors in parallel with 0.1 μF capacitors to GND. To achieve the best from these decoupling components, place them as close as possible to the device.

OUTLINE DIMENSIONS

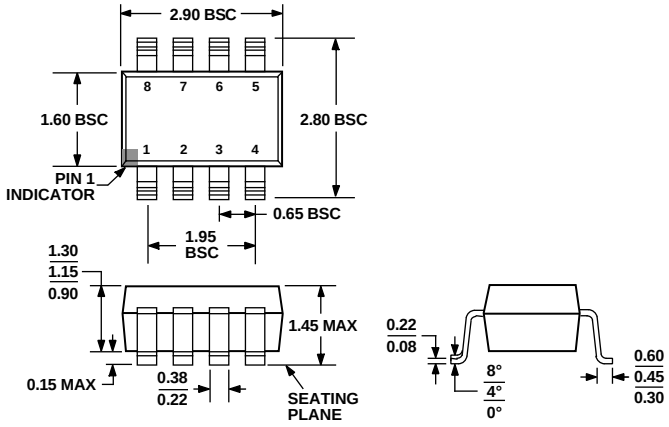


Figure 26. 8-Lead Small Outline Transistor Package [SOT-23]
(RT-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Description	Package Option	Branding
AD7457BRT-R2	–40°C to +85°C	±1	8-Lead SOT-23	RT-8	COJ
AD7457BRT-REEL7	–40°C to +85°C	±1	8-Lead SOT-23	RT-8	COJ
AD7457BRTZ-REEL7[2]	–40°C to +85°C	±1	8-Lead SOT-23	RT-8	COD

[1] Linearity error here refers to integral nonlinearity error.
[2] Z = Pb-free part.

NOTES

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