DUAL SYNCHRONOUS RECTIFICATION CONTROL IC

Features

- Secondary-side high speed synchronous rectification controller for resonant half bridge converters
- Direct sensing of MOSFET drain voltage up to 200V
- Operates up to 400kHz switching frequency
- Programmable Minimum On Time
- Anti-bounce logic and UVLO protection
- Linear turn-off phase to compensate for premature switch off due to parasitic inductance
- 4A peak turn off drive current
- Micropower start-up & ultra-low quiescent current
- 50ns turn-off propagation delay
- Wide Vcc operating range 4.75V to 18V
- Cycle by Cycle MOT Protection
- Auto low power mode standby mode
- Improved noise immunity
- Compatible with Energy Star low standby power
- Lead-free

Typical Applications

- Desktop SMPS, Server SMPS, AC-DC adapters, LCD & PDP TV, Telecom SMPS

Product Summary

Topology	LLC Half-bridge
VD	200V
V_{OUT}	Vcc
I_{o+} & I_{o-}	+1A & -4A

Package Options



8-Pin SOIC

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IR11688S	SOIC8N	Tape and Reel	2500	IR11688STRPBF

Typical Connection Diagram

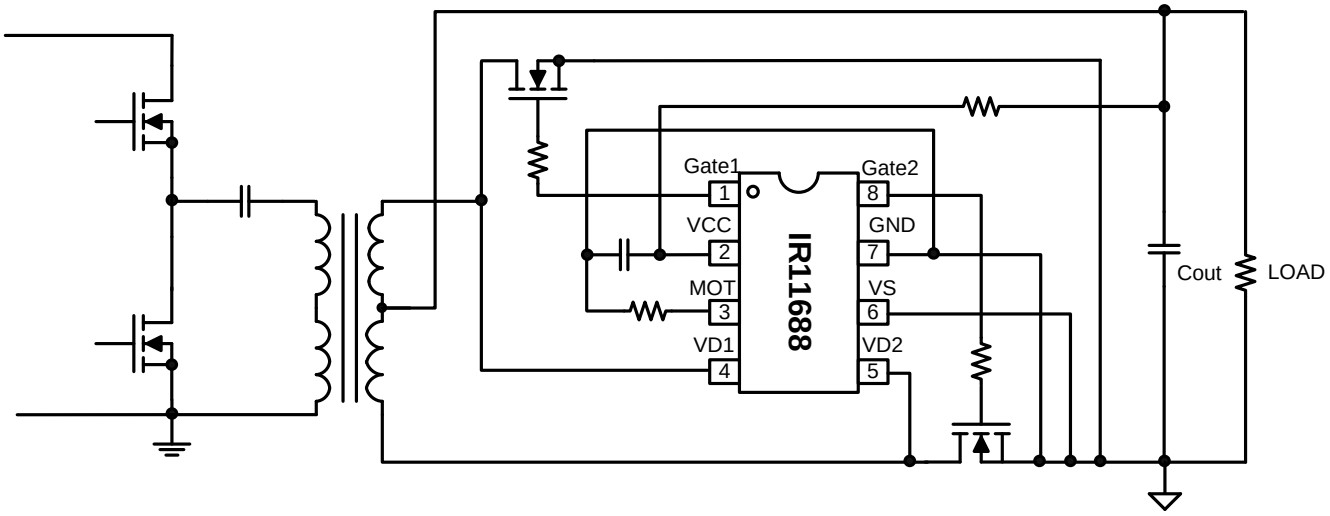


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Description

The IR11688 is a dual smart secondary-side controller IC optimized to drive two N-Channel power MOSFETs configured for synchronous rectification in resonant converter applications. Each channel can drive one or multiple parallel MOSFETs to emulate the behavior of Schottky diode rectifiers, bypassing the body diodes for the majority of each conduction period to minimize power dissipation and remaining off during the blocking period.

The drain to source voltage of each rectifier MOSFET is sensed to determine the source to drain current and turn each gate on rapidly at the start of each conduction cycle and off in close proximity to the zero current transitions for each branch of the output rectifier circuit. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression that allows reliable operation in fixed and variable frequency applications.

The programmable minimum on time (MOT) function provides flexibility to work over a wide range of switching frequencies. The cycle-by-cycle MOT protection circuit is able to automatically detect a light or no load condition so that the gate drives may be disabled to avoid unwanted reverse currents flowing through the MOSFETs.

The IR11688 has a wide Vcc supply voltage range from 4.75V to 18V, enabling its supply to be derived from the output and eliminating the need for an auxiliary supply circuit in systems with output voltage as low as 5V.

The IR11688 also has very low quiescent current when the gate drives are not switching to offer minimal power consumption in standby mode.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any pin. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Parameters	Symbol	Min.	Max.	Units	Remarks
Supply Voltage	V_{CC}	-0.3	20	V	
Cont. Drain Sense Voltage	$V_{D1,2}$	-1	200	V	
Pulse Drain Sense Voltage	$V_{D1,2}$	-3	200	V	
Source Sense Voltage	V_S	-1	5	V	
Gate Voltage	$V_{GATE1,2}$	-0.3	Vcc+0.3	V	
MOT Voltage	V_{MOT}	-0.3	3.5	V	
Operating Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance	$R_{\theta JA}$		128	°C/W	SOIC-8
Package Power Dissipation	P_D		970	mW	SOIC-8, T_{AMB}=25°C

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Supply voltage	4.75	18	V
V_D	Drain Sense Voltage	-3 ①	200	
T_J	Junction Temperature	-40	125	°C
Fsw	Switching Frequency	---	400	kHz

① V_D -3V negative spike width ≤100ns

Recommended Component Values

Symbol	Component	Min.	Max.	Units
R_{MOT}	MOT pin resistor value	20	150	kΩ

Electrical Characteristics

VCC=12V, T_A = 25°C unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to GND (pin7).

Supply Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Supply Voltage Operating Range	V_{CC}	4.75		18	V	
V_{CC} Turn On Threshold	$V_{CC\ ON}$	4.35	4.55	4.75	V	
V_{CC} Turn Off Threshold (Under Voltage Lock Out)	$V_{CC\ UVLO}$	4.15	4.35	4.55	V	
V_{CC} Turn On/Off Hysteresis	$V_{CC\ HYST}$	---	0.2	---	V	
Operating Current	I_{CC}	---	13	15	mA	C_{LOAD} =1nF, f_{SW} = 400kHz, R_{MOT}=50kΩ
Quiescent Current	I_{QCC}	---	320	500	µA	No switching at VD pins and after T_{WAIT} is exceeded, VD=2V, R_{MOT}=50kΩ
Start-up Current	$I_{CC\ START}$	---	40	80	µA	V_{CC}=$V_{CC\ ON}$ - 0.1V
Quiescent waiting time	T_{WAIT}	340	570	800	µS	

Comparator Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Turn-off Threshold	V_{TH1}	-7	-4	0	mV	V_S=0V
Regulation Threshold	V_{THR}	-50	-40	-30	mV	10mV hysteresis (-50mV/-40mV)
Turn-on Threshold	V_{TH2}	-263	-230	-197	mV	
Hysteresis	V_{HYST}	---	230	---	mV	GBD
Input Bias Current	I_{IBIAS1}	-7.5	-5	---	µA	V_D = -50mV
Input Bias Current	I_{IBIAS2}	---	7	10	µA	V_D = 200V
Turn-on Blanking time	T_{Bon}	---	150	---	ns	GBD

One-Shot Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Blanking pulse duration	t_{BLANK}	8	15	24	µs	
Reset Threshold	V_{TH3}	1.06	1.18	1.31	V	
Reset Delay	t_{BRST}	---	400	---	ns	
Hysteresis	V_{HYST3}	---	40	---	mV	GBD

Minimum On Time Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Minimum on time	T_{Onmin}	375	500	625	ns	R_{MOT} =24kΩ, V_{CC}=5V
		0.75	1	1.25	µs	R_{MOT} =50kΩ, V_{CC}=5V

Electrical Characteristics

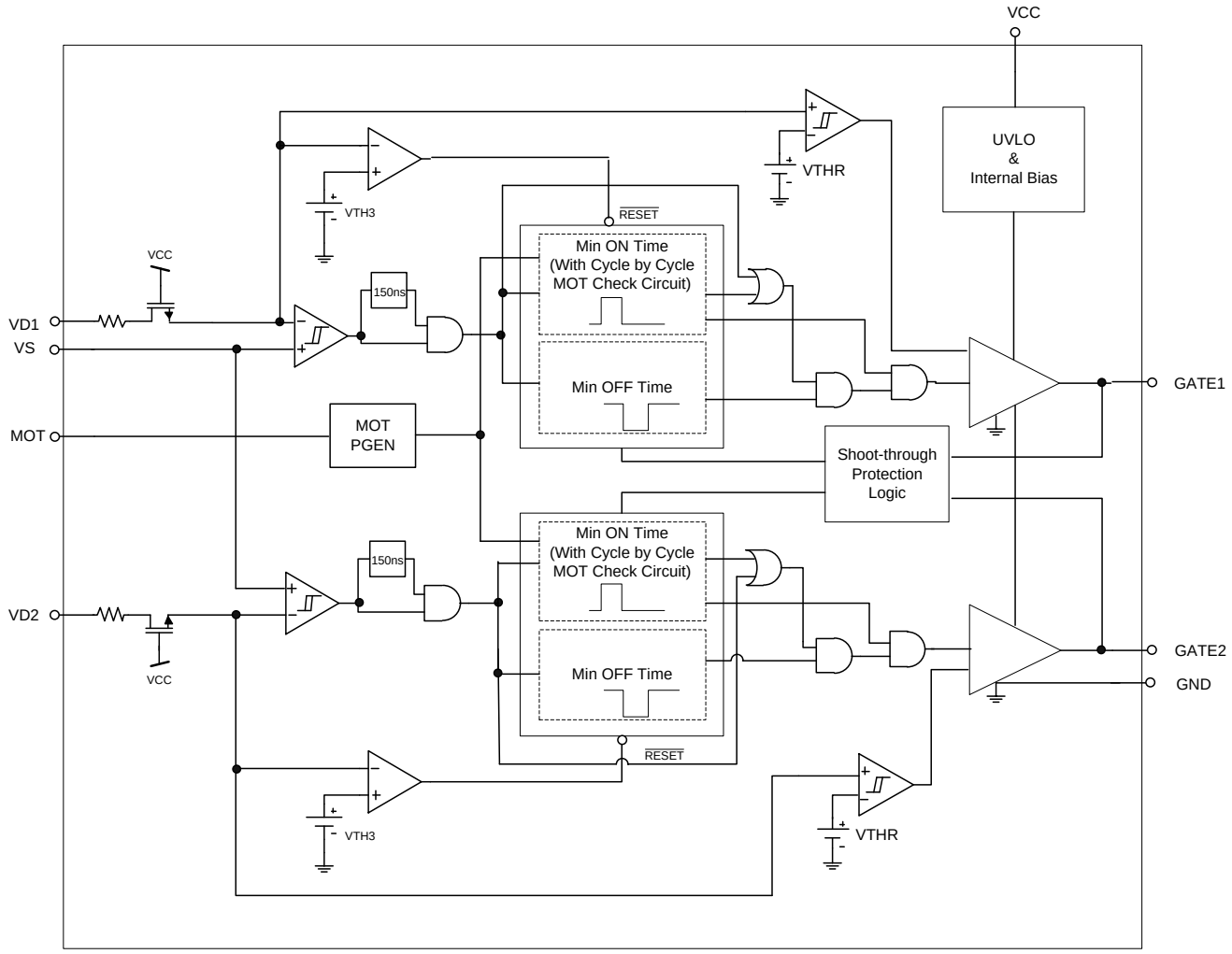
VCC=12V, T_A = 25°C unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to GND (pin7).

Gate Driver Section

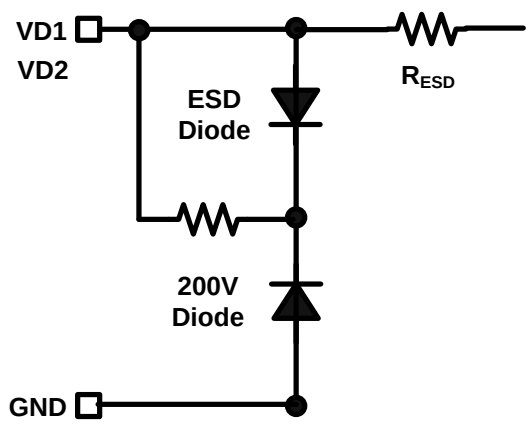
Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Gate Low Voltage	V_{GLO}	---	0.15	0.25	V	I_{GATE} = 100mA
Gate High Voltage	V_{GTH}	---	11.9	---	V	GBD
		---	4.9	---		GBD
Rise Time	t_r	---	20	38	ns	C_{LOAD} = 1nF
Fall Time	t_f	---	10	22	ns	C_{LOAD} = 1nF
Turn on Propagation Delay	t_{Don}	---	200	250	ns	V_{DS} to V_{GATE} – V_{DS} goes down from 6V to -1V
Turn off Propagation Delay	t_{Doff}	---	42	60	ns	V_{DS} to V_{GATE} –V_{DS} goes up from -1V to 6V
Pull up Resistance	r_{up}	---	6	---	Ω	GBD
Pull down Resistance	r_{down}	---	1.5	---	Ω	I_{GATE} = -100mA
Output Peak Current (source)	$I_{O\ source}$	---	1	---	A	GBD
Output Peak Current (sink)	$I_{O\ sink}$	---	4	---	A	GBD

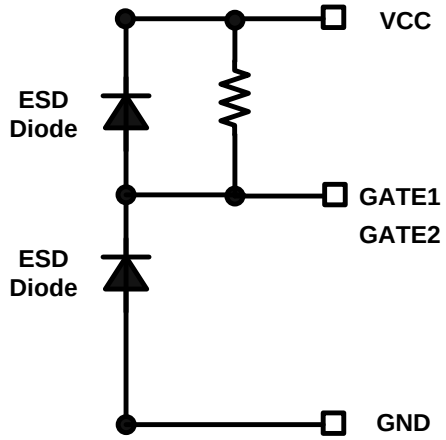
GBD – parameter is guaranteed by design and is not tested.

Functional Block Diagram



I/O Pin Equivalent Circuit Diagram

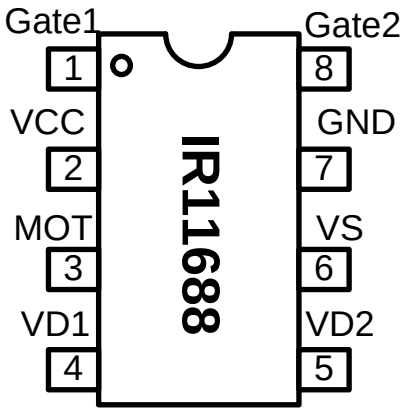




Pin Definitions

PIN#	Symbol	Description
1	GATE1	Gate Drive Output 1
2	VCC	Supply Voltage
3	MOT	Minimum On Time Programmable pin
4	VD1	Sync FET 1 Drain Voltage Sense
5	VD2	Sync FET 2 Drain Voltage Sense
6	VS	Sync FET Source Voltage Sense
7	GND	Analog and Power Ground
8	GATE2	Gate Drive Output 2

Pin Assignments



Detailed Pin Description

VCC: Power Supply
This is the supply voltage pin of the IC, monitored by the under voltage lockout circuit. It is possible to turn off the IC entering UVLO mode by pulling this pin below the minimum turn off threshold voltage for micro power consumption.
To prevent noise interfering with operation, a ceramic decoupling capacitor should be connected from Vcc to GND and located as close to the IC as possible. A low value series resistor may also be added to the Vcc supply circuit for filtering if required. Vcc is internally clamped at around 20V.

GND: Ground
This is power ground connection to the IC. Internal circuit blocks and gate drivers are referenced to this point.

MOT: Minimum On Time
The MOT programming pin controls the amount of minimum on time. Once V_{TH2} is crossed at either VD input, the corresponding gate drive output will transition high to turn on the SR MOSFET. Spurious ringing and oscillations can falsely trigger the input comparator to prematurely switch the output off. During the MOT period the input comparator is disabled maintaining conduction through the MOSFET on for this preset minimum period.
The MOT is typically programmed between 500ns and 2us by means of an external resistor referenced to GND.

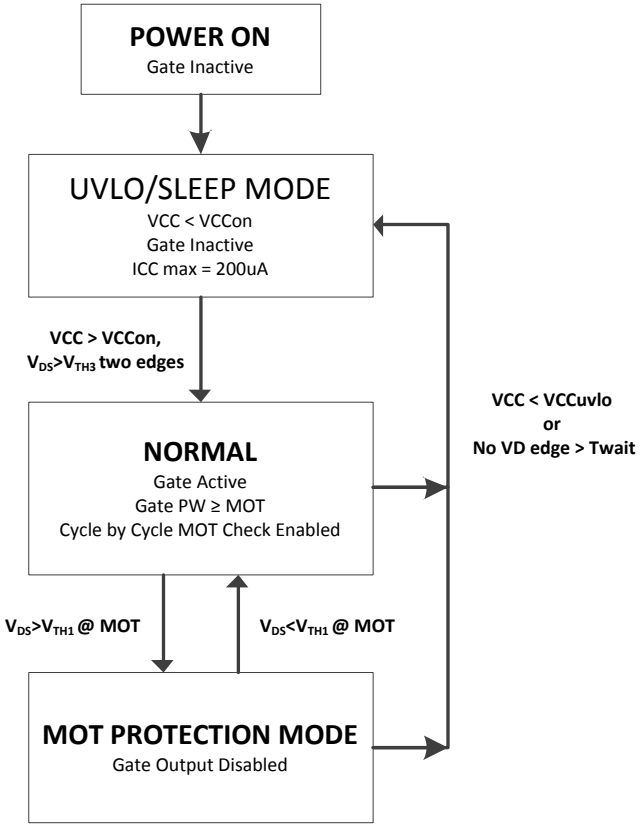
VD1 and VD2: Drain Voltage Sense
The VD pins are the voltage sensing inputs for the SR MOSFET drains. These are high voltage inputs therefore particular care must be taken in properly routing the connections. Additional RC filters can be placed at these inputs to improve noise immunity, however only a small resistor (≤1kΩ) and capacitor value (in the pF range) may be used to avoid introducing excessive delay to the control input.

VS: Source Voltage Sense
This is the signal ground for the sources of the two SR power MOSFETs to provide an accurate differential voltage measurement. Kelvin connect this pin to the source of MOSFET2 (channel 2 MOSFET) is recommended if the two MOSFETs are far apart to each other.

GATE1 and GATE2: Gate Drive Outputs
Each gate driver output has +1A/-4A peak drive capability. Although these pins can be directly connected to the SR MOSFET gates the use of gate resistors is recommended, especially when using several MOSFETs in parallel. Care must be taken to keep the gate loop as short and as tight as possible in order to achieve optimal switching performance.

Application Information and Additional Details

State Diagram



UVLO/SLEEP Mode

The IC remains in the UVLO/SLEEP condition until the voltage at the VCC pin first exceeds the VCC turn on threshold voltage, $V_{CC\ ON}$. While in the UVLO/SLEEP state, the gate drive outputs are inactive and only a very small quiescent current of $I_{CC\ START}$ is drawn. UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of Vcc < $V_{CC\ UVLO}$ occurs. If during normal operation, the drain inputs remain inactive such that no edges are detected for a period longer than T_{WAIT} the IC enters SLEEP mode. It remains in a low power state until woken up by a voltage transition at either VD input.

Normal Mode

The IC enters into normal operating mode when the $V_{CC\ ON}$ threshold has been exceeded. On entering Normal Mode from the UVLO Mode the GATE outputs remain disabled until V_{DS} transitions above V_{TH3} two times. This ensures that the GATE output cannot be enabled in the middle of a switching cycle since this can cause undesired reverse conduction. The cycle by cycle minimum on time (MOT) protection circuit also becomes activated to prevent reverse currents occurring when conduction time is short, which may also happen during system power up and down. The gate drives will continuously drive the MOSFETs after this startup sequence is completed.

MOT Protection Mode

If secondary current conduction time in either rectifier circuit branch is shorter than the set MOT, the subsequent gate driver output pulse is skipped. This function avoids reverse current from occurring when the system is switching at very low duty-cycles under very light or zero load conditions. The cycle by cycle MOT check circuit always remains active in Normal Mode and MOT Protection Mode so that the IC will automatically resume normal operation only after the load increases to a level where the secondary current conduction time exceeds MOT. System standby power consumption is significantly reduced in this mode while the gate outputs are inactive.

General Description

The IR11688 dual *SMART RECTIFIER*™ controller is a high-voltage IC for synchronous rectification designed for resonant converter applications. As stated, it emulates the operation of two diodes configured with a center tapped transformer secondary by correctly switching on and off the synchronous rectifier MOSFETs in the two rectifier circuit branches.
The core of this device consists of two high-voltage drain sensing inputs feeding high speed comparators to differentially sense the drain to source voltage at each SR MOSFET. The SR MOSFET source to drain current is detected from the voltage across the conducting body diode or the R_{DSON} resistance when switched on. Internal control logic allows the corresponding gate drive output to be switched on and off at the correct time to bypass the body diode for the majority of the conduction period.

The IR11688 further simplifies synchronous rectifier control by offering the following power management features:

- Wide VCC operating range allows the IC to be supplied from the converter output
- Shoot through protection logic that prevents both GATE outputs from ever being high at the same time
- Turn-off phase regulation to compensate for power device package inductance and avoid premature turn-off
- Optimized negative turn on voltage threshold detection and leading edge noise filter to minimize false triggering due to ringing oscillations

The IR11688 control technique senses SR MOSFET source to drain voltages comparing them with three different negative thresholds (V_{TH1}, V_{TH2} and V_{THR}) to precisely control gate turn on and off as shown in figure 1:

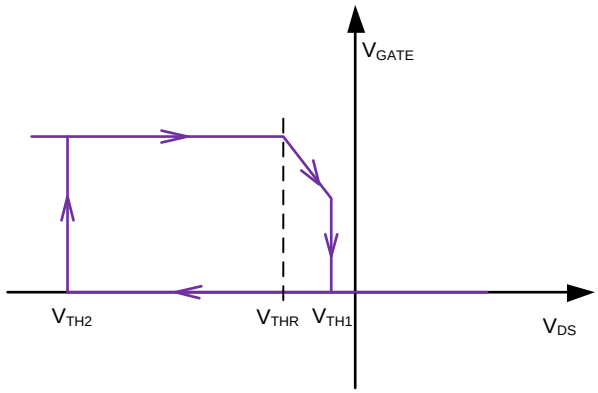


Figure 1: Input comparator thresholds

Turn-on phase

When the conduction phase of each SR MOSFET begins, the device is off so therefore current starts to flow through the body diode producing a negative V_{DS} voltage across it. The body diode has a much higher voltage drop than the one resulting from the MOSFET on resistance and is therefore sufficient to trigger the turn-on threshold V_{TH2}.
When either V_{DS} input remains below V_{TH2} for more than T_{Bon} (150ns), the gate of the corresponding SR MOSFET is driven high, which causes V_{DS} to reduce rapidly to I_D x R_{DSON}. The internal delay timer will be reset if V_{DS} rises above V_{TH2} before T_{Bon} times out. This turn-on blanking time helps to avoid misfiring that could be triggered by high frequency ringing in DCM operation. The voltage drop at switch on is usually accompanied by some amount of ringing, which could potentially trigger the input comparator to turn off the gate drive very quickly. However the minimum on time (MOT) blanking period prevents this. The turn-on blanking time (T_{Bon}) and the MOT limit the minimum conduction time for the secondary rectifiers determining the switching frequency upper limit that the IR11688 may effectively operate at.

Regulation phase

After the gate has been driven high at switch on, the SR MOSFET remains on until the source to drain current falls to the level where V_{DS} reaches the regulation threshold V_{THR}. At the end of the MOT, the gate output is no longer driven high and reverts to a high impedance state. When $V_{DS}<V_{THR}$ a weak pull down gradually discharges the gate voltage held by the SR MOSFET input capacitance. As the gate voltage drops, the MOSFET channel resistance increases as it enters the linear region. This causes V_{DS} to once again exceed V_{THR} so that weak pull down will cease until the conduction current falls to the point where V_{DS} again drops below $V_{THR.}$ This regulating process continues so that the conduction period is extended until the current has fallen to a very low level. In this way premature turn off, which can arise due to parasitic inductances in PCB traces and the MOSFET package, is prevented. This period of conduction through the SR MOSFET body diodes is thereby reduced to a minimum improving overall system efficiency.

Turn-off and reset phases

At the end of the switching cycle the conduction rectifier current reduces to zero so the V_{DS} voltage will cross the turn-off threshold V_{TH1}. When this happens the gate is driven low to switch off the SR MOSFET. Any residual current will again start flowing through the body diode causing a negative step in V_{DS}. When this occurs V_{DS} could potentially trigger turn-on once again by crossing V_{TH2}. To prevent this possibility, turn on is blanked for a time period, t_{BLANK} after turn off has occurred. The blanking time is internally set and can be reset only when V_{DS} crosses the positive threshold $V_{TH3.}$ Reset occurs only when V_{DS} remains higher than V_{TH3} for more than the reset blanking time, t_{BRST}. This protects against false triggering due to ringing after the turn-off phase. Once reset the IR11688 is re-armed so that turn on may be triggered for the next conduction cycle.

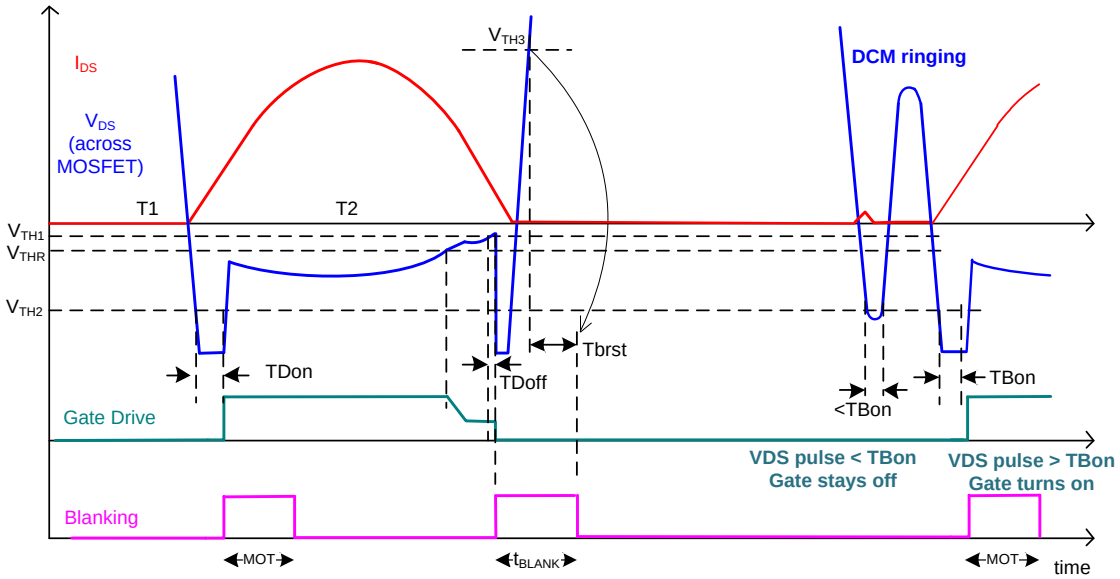


Figure 2: Secondary currents and voltages

Programmable Minimum On Time

The minimum on time is set by an external resistor (RMOT) connected between the MOT pin and ground. The minimum on time can be calculated based on below equation:

$$T_{MOT} = R_{MOT} \times 2 \times 10^{-11} + 20ns$$

where 20ns is the typical internal comparator propagation delay.

RMOT value should remain within the upper and lower limits specified under recommended operating conditions.

MOT protection

Under very light load or zero load conditions, the current in the SR MOSFETs becomes discontinuous and may be shorter than the MOT time in some cases. If this happens, reverse current will flow from the drain to source at the end of the MOT since the gate drive has been kept on. This reverse current discharges the converter output capacitor sending energy back to the transformer and resonating to cause voltage ringing at V_{DS} at switch off. Such ringing may potentially trigger gate turn on leading to further reverse current and subsequent multiple falsely triggered erroneous gate pulses as illustrated below in Figure 4:

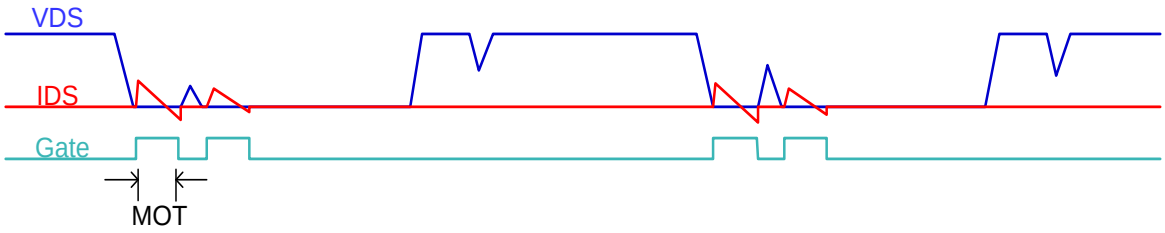


Figure 3: Waveform without MOT protection

The cycle-by-cycle MOT protection function detects reverse current at the end of the MOT period and disables the following gate output pulse preventing further reverse current. The internal comparator and MOT pulse generator continue to operate under the protection mode even when the gate drive is disabled. This enables the circuit to continuously monitor the system load current and automatically revert to normal operating mode once the load current conduction time has again increased to be longer than the MOT. This protection function reduces standby power losses and can also prevent voltage spikes caused by false triggering at light load.

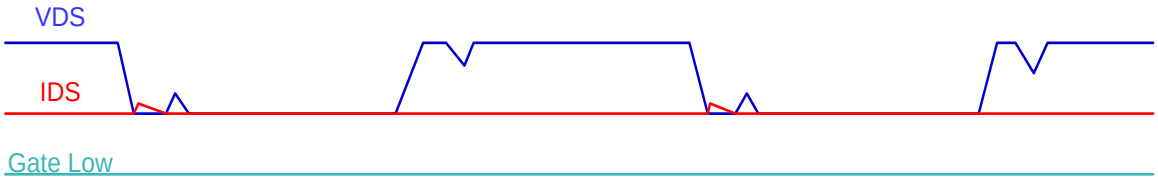


Figure 4: Waveform under MOT protection mode

Synchronized Enable Function

Sync Enable function ensures that gate turn on always occurs at the beginning of a switching cycle.

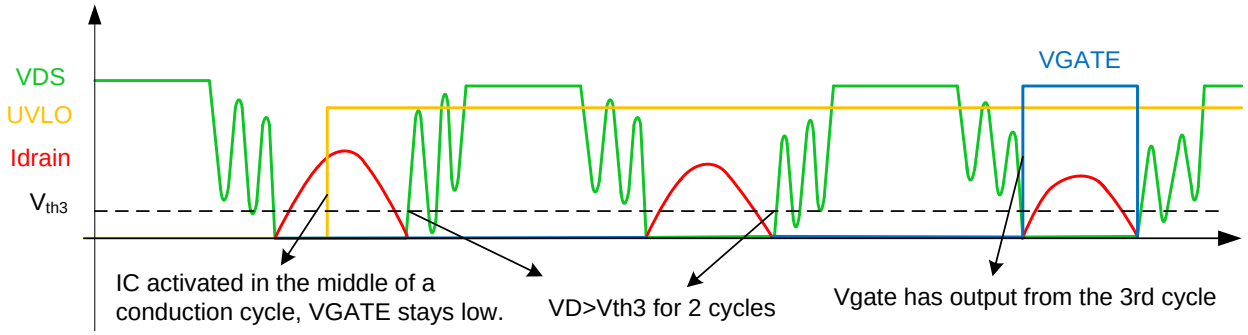


Figure 5: Synchronized Enable Function

Driving Logic Level MOSFET

An external gate clamping circuit is recommended when driving logic level SR MOSFETs. The clamping circuit keeps the gate voltage below 1V during system power up when the IR11688 is not fully biased in UVLO mode, especially when Vcc is less than 2V. It is not recommended to drive logic level MOSFETs with the IR11688 without a safety clamping circuit.

Note the gate regulation feature will be lost when using PNP transistor clamping circuit. Use MOSFET clamping circuit (figure 7) if regulation function is needed.

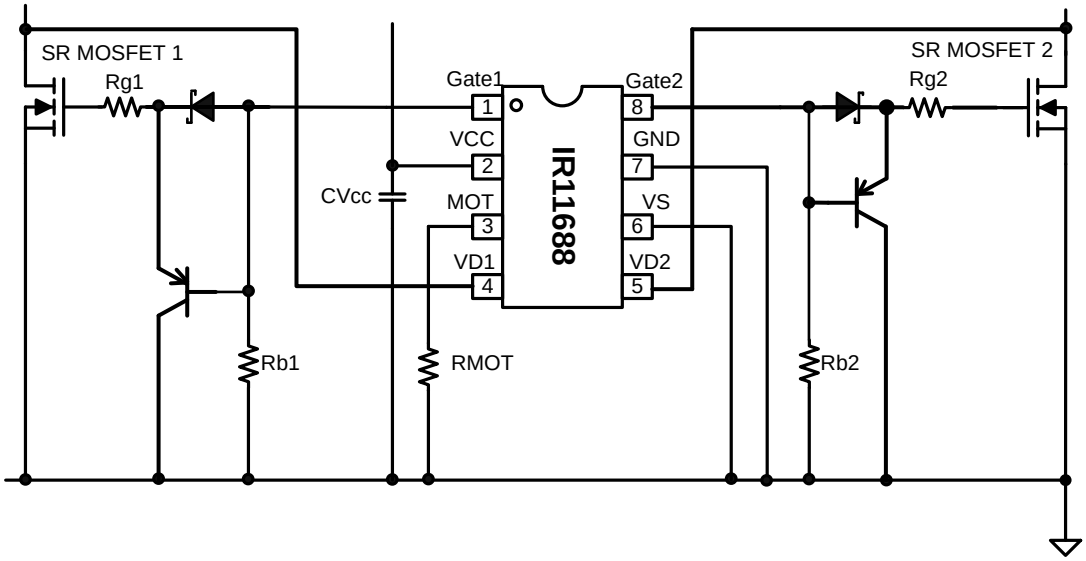


Figure 6: PNP transistor gate clamping circuit for driving logic level MOSFET

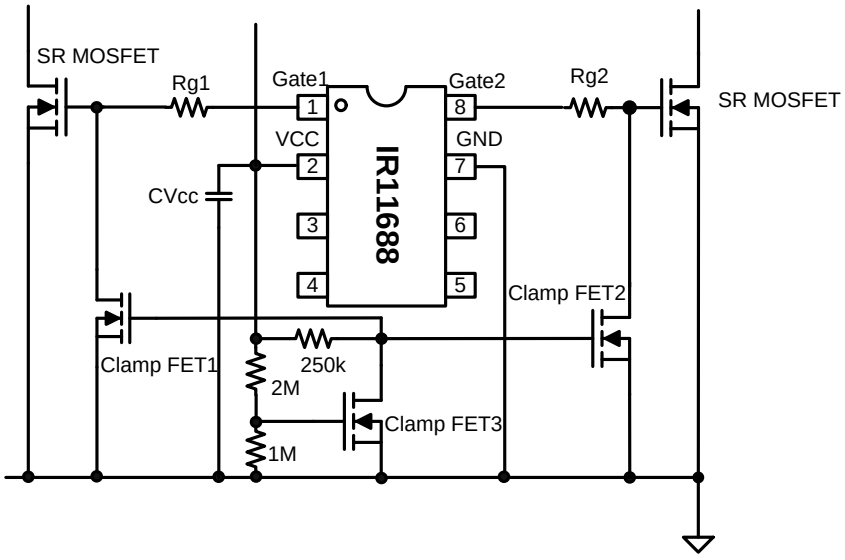


Figure 7: Signal MOSFET gate clamping circuit for driving logic level MOSFET

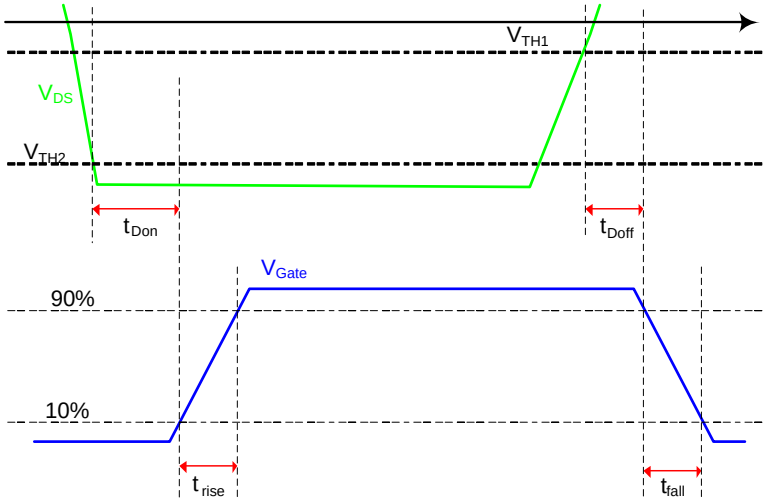


Figure 8: VD and gate drive output timing

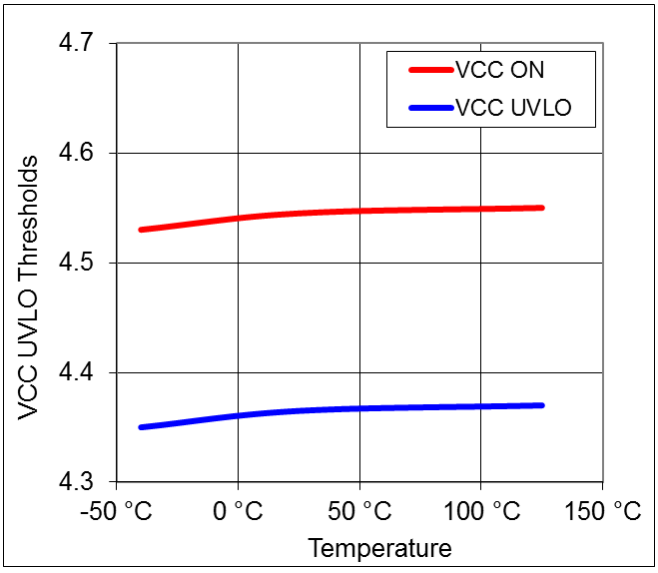


Figure 9: Undervoltage Lockout vs. Temperature

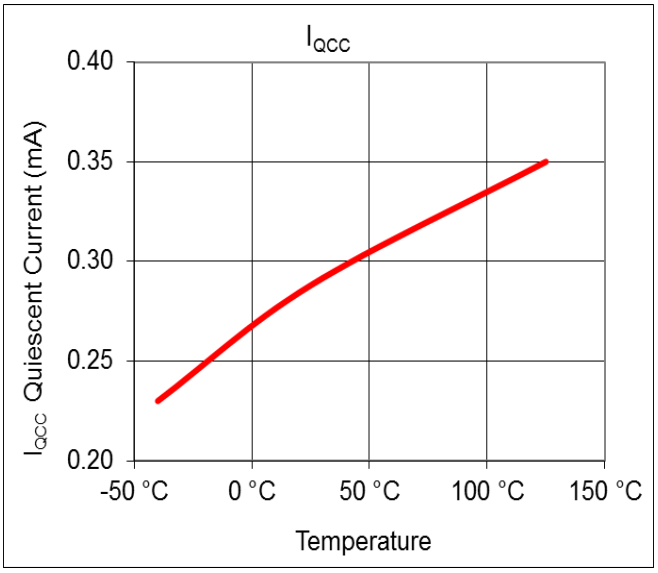


Figure 10: Icc Quiescent Current vs. Temperature

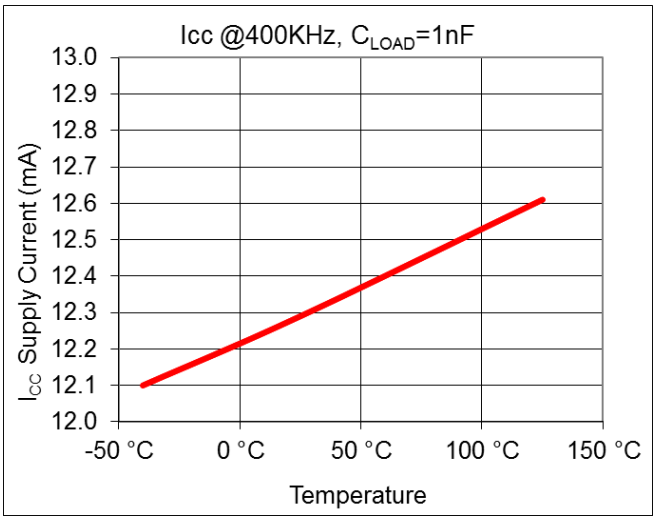


Figure 11: Icc supply current at 1nF load vs. Temperature

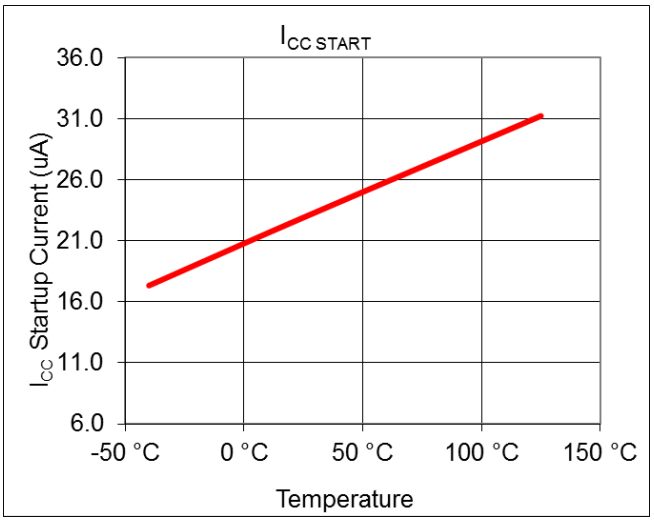


Figure 12: Icc Startup Current vs. Temperature

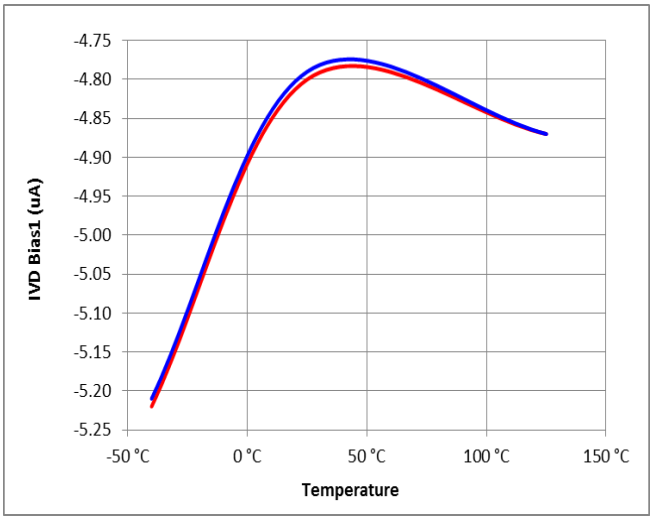


Figure 13: VD bias at -50mV vs. Temperature

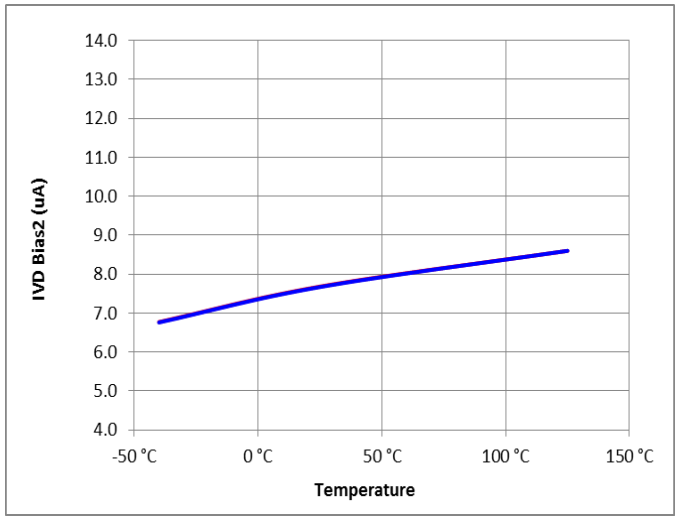


Figure 14: VD bias at 200V vs. Temperature

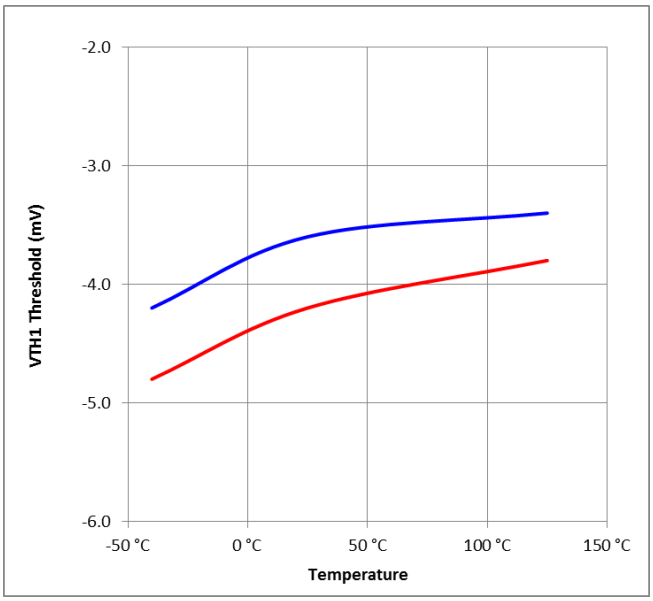


Figure 15: V_{TH1} Threshold vs. Temperature

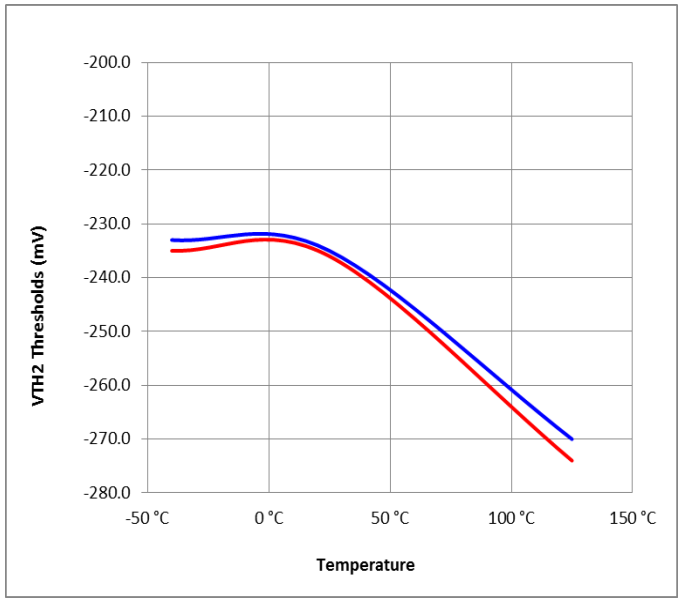


Figure 16: V_{TH2} Threshold vs. Temperature

(Red curve channel 1, Blue curve channel 2)

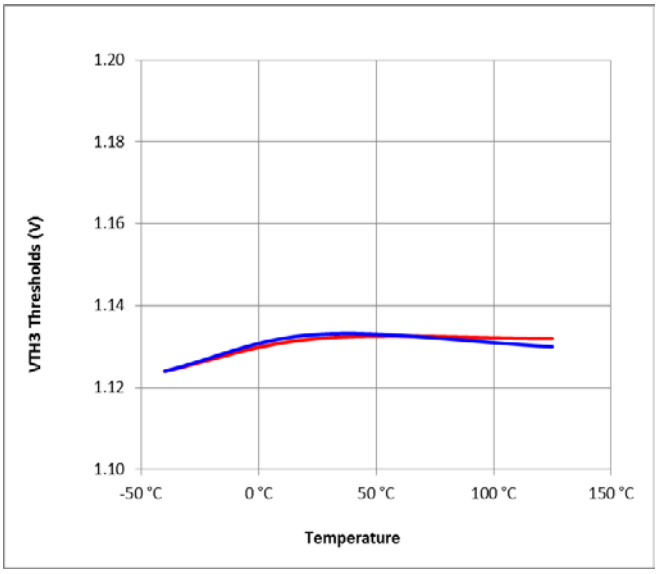


Figure 17: V_{TH3} Threshold vs. Temperature

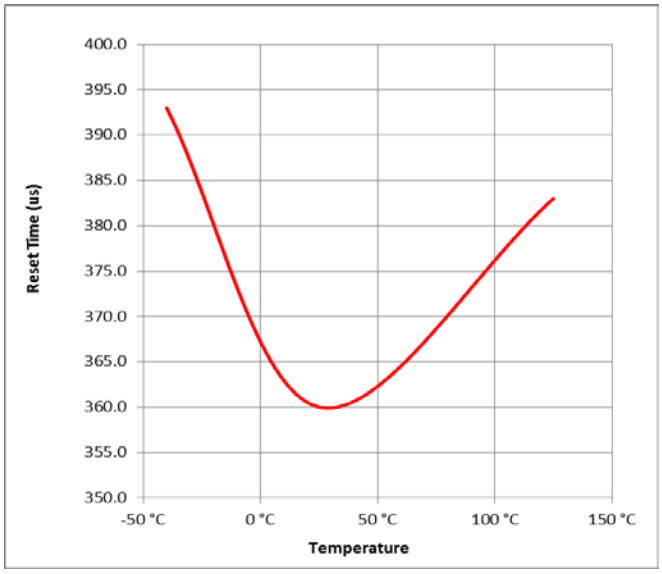


Figure 18: T_{BRST} Reset Time vs. Temperature

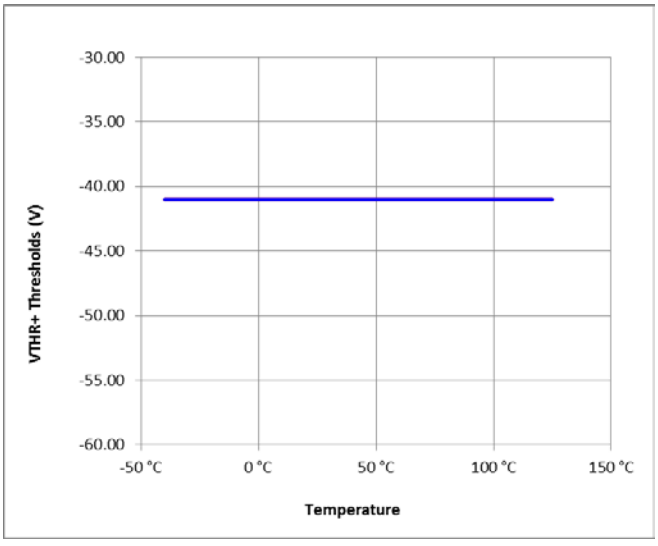


Figure 19: V_{THR+} Threshold vs. Temperature

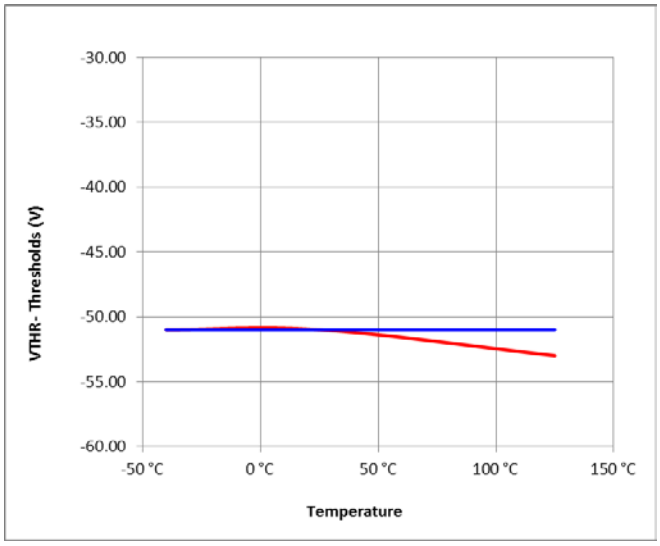


Figure 20: V_{THR-} Threshold vs. Temperature

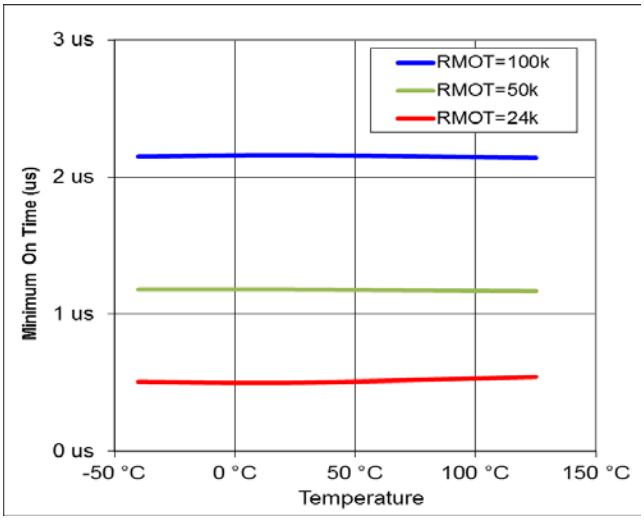


Figure 21: Minimum On Time vs. Temperature

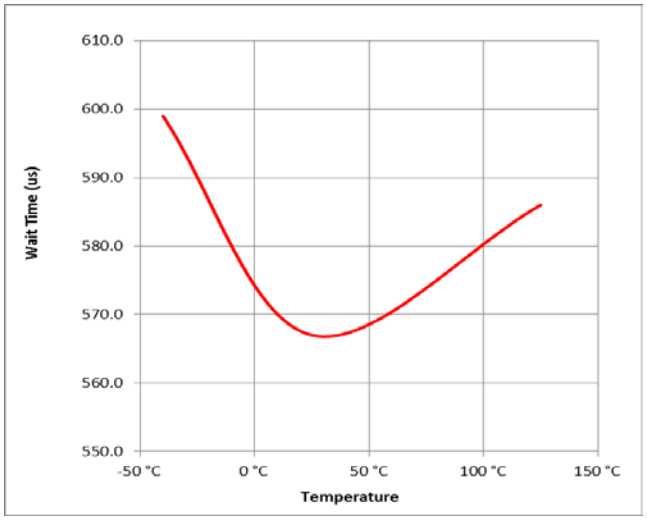


Figure 22: T_{WAIT} Wait Time vs. Temperature

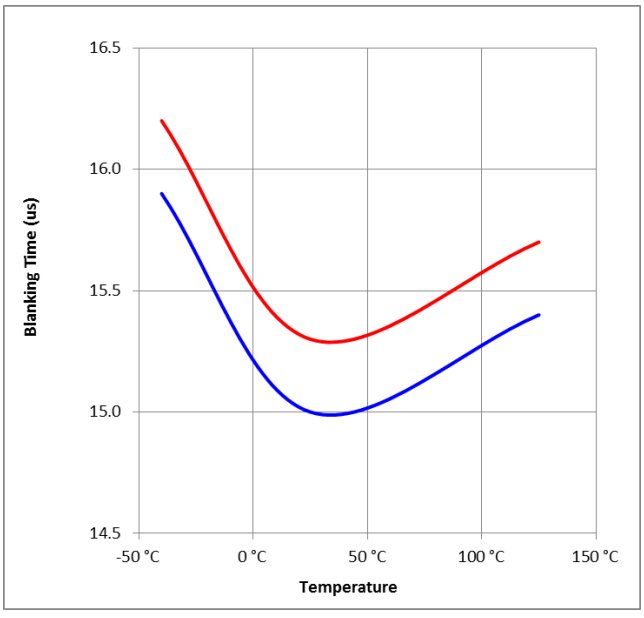


Figure 23: T_{BLANK} Blanking Time vs. Temperature

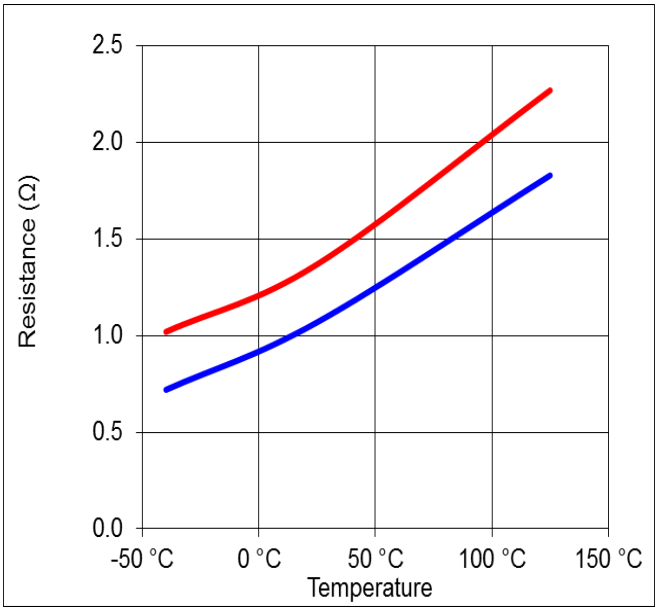


Figure 24: Gate Pull Down Resistance vs. Temperature

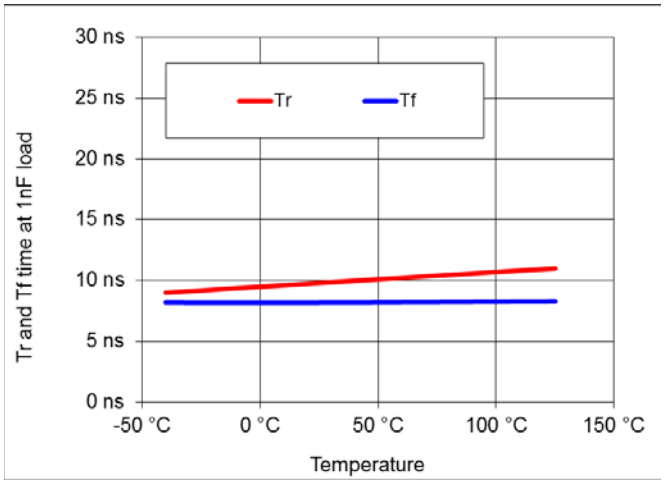


Figure 25: Gate Rise and Fall Time vs. Temperature (CH1)

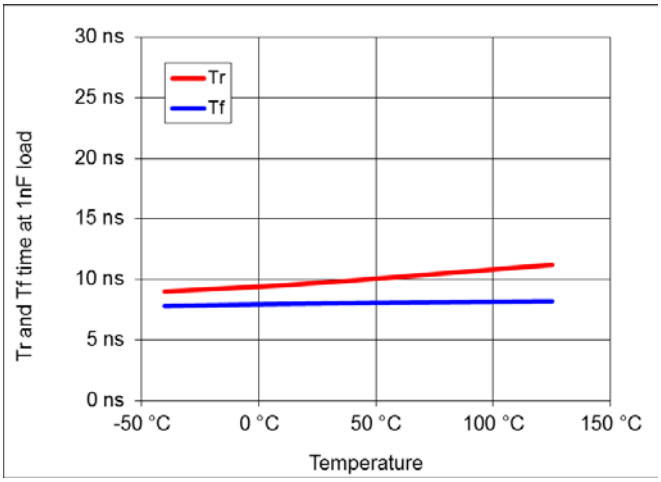


Figure 26: Gate Rise and Fall Time vs. Temperature (CH2)

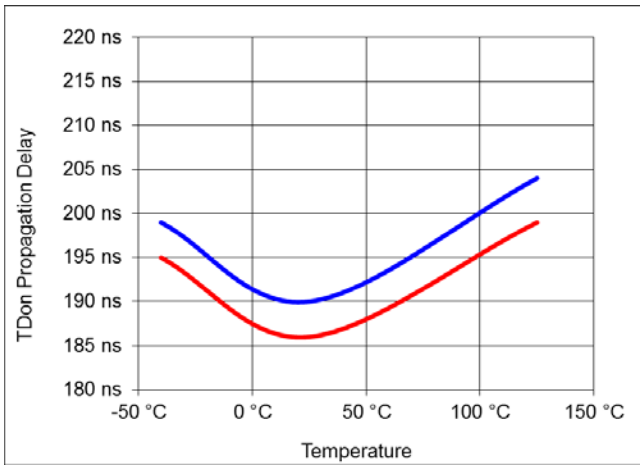


Figure 27: TD_{ON} Propagation Delay vs. Temperature

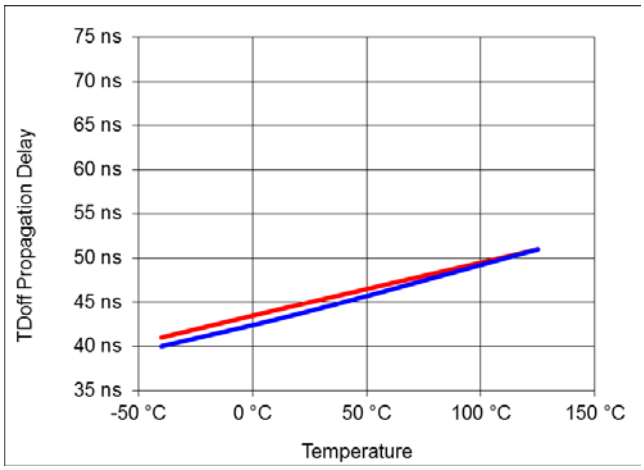
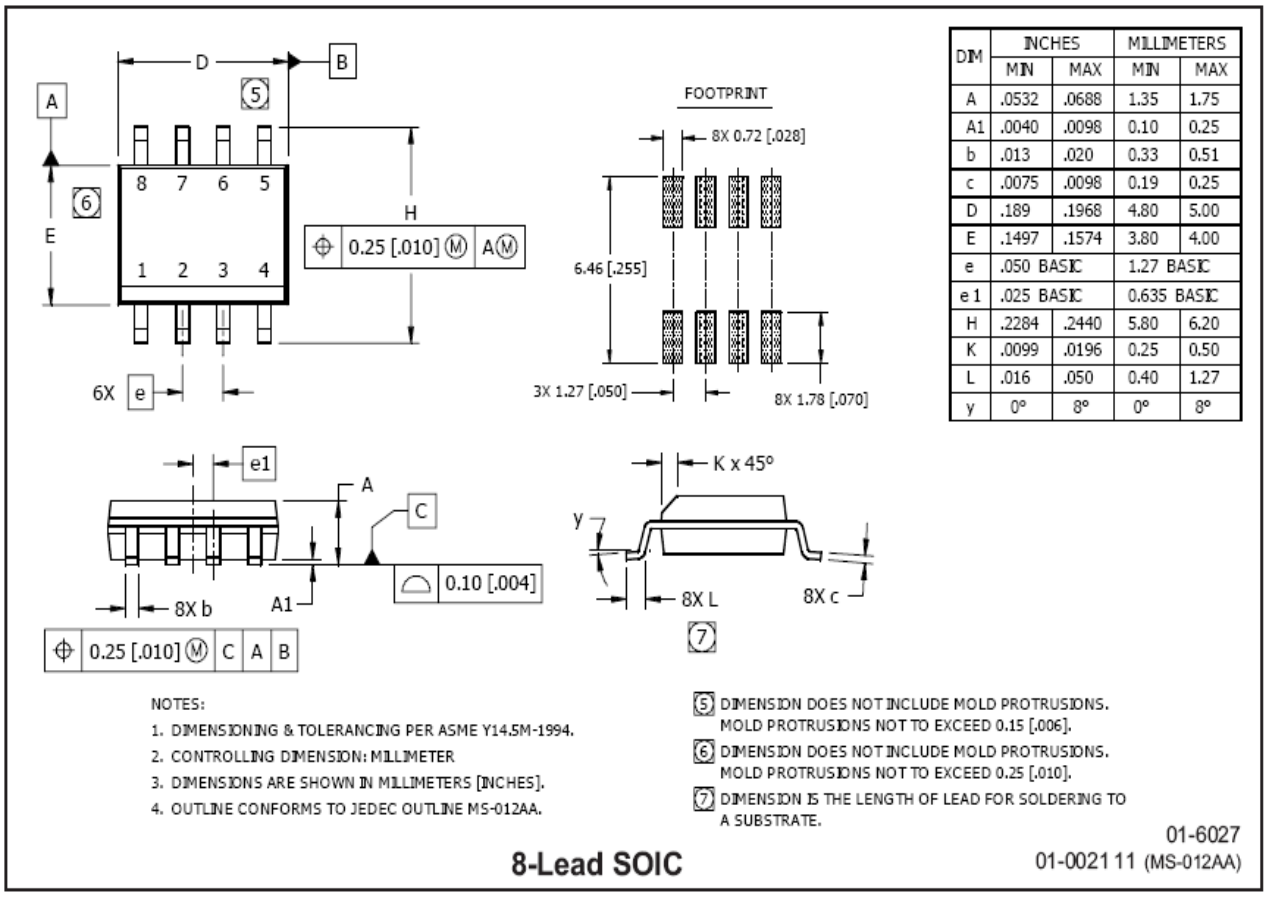


Figure 28: TD_{OFF} Propagation Delay vs. Temperature

Package Details: SOIC8N



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

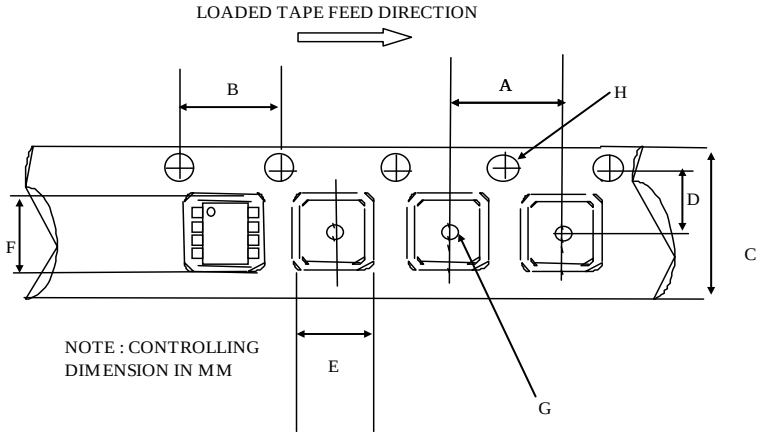
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

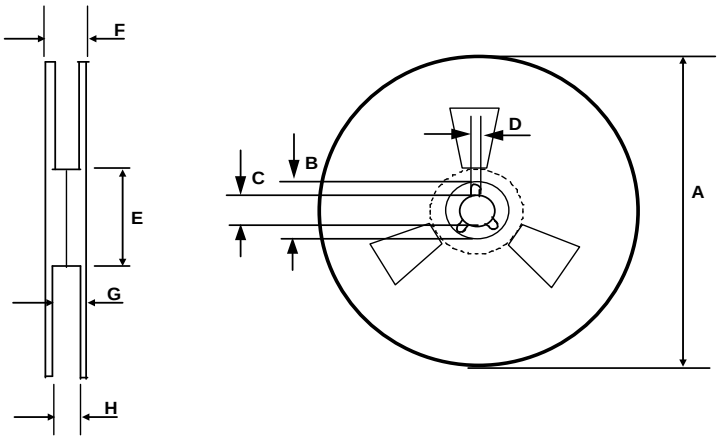
8-Lead SOIC

Tape and Reel Details: SOIC8N



CARRIER TAPE DIMENSION FOR 8SOICN

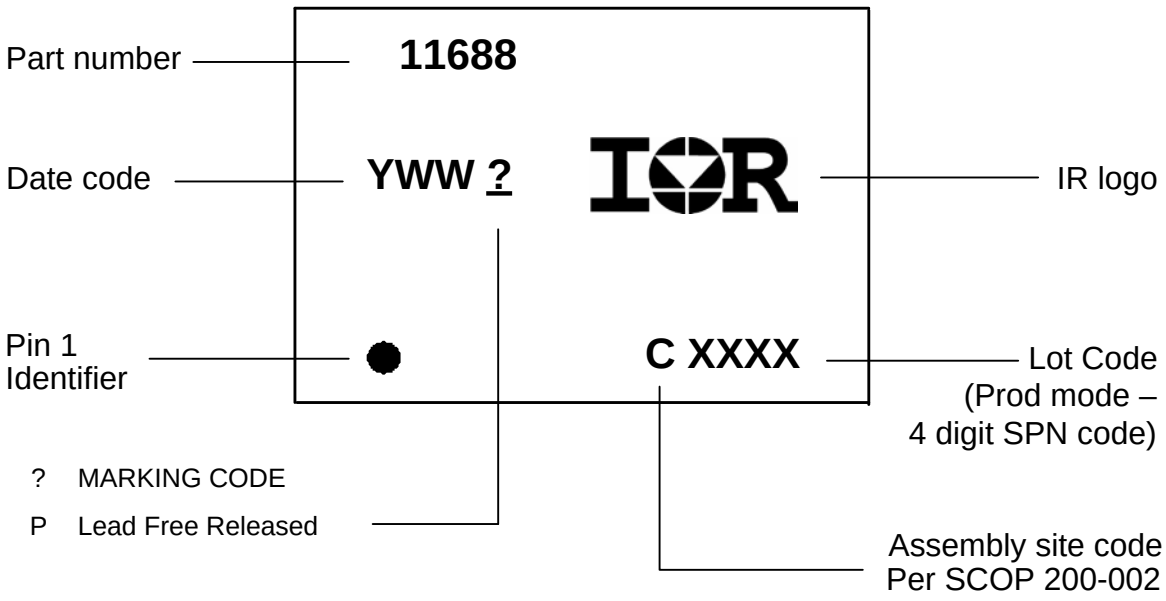
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC8N	MSL2††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 1C (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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