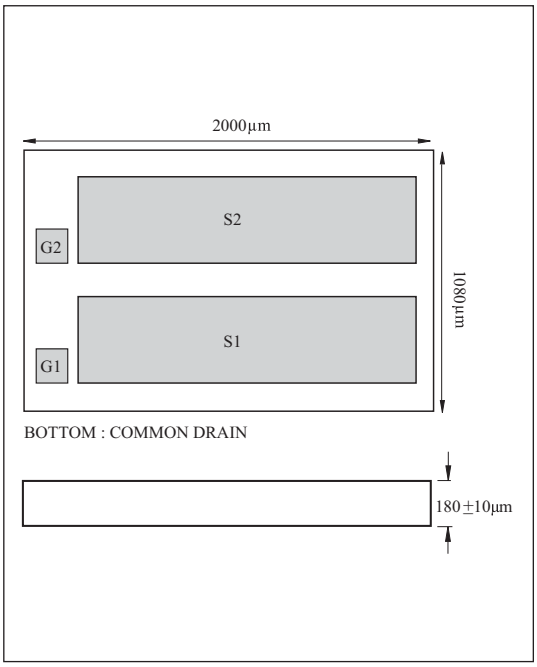
K3520PQ-XH

Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

The K3520PQ-XH is a Dual N-channel MOSFET designed for use as a bi-directional load switch, facilitated by its common-drain configuration.



FEATURES

· Low on-state resistance

$R_{DS(ON)1}$ = 16mΩ MAX (V_{GS}=4.5V, I_S=1.0A)

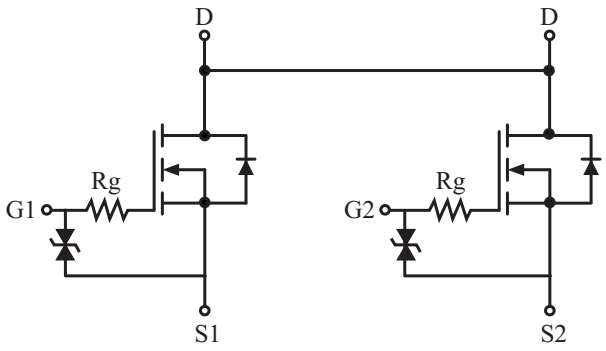
$R_{DS(ON)2}$ = 17mΩ MAX (V_{GS}=3.9V, I_S=1.0A)

$R_{DS(ON)3}$ = 20mΩ MAX (V_{GS}=3.5V, I_S=1.0A)

MAXIMUM RATING (Ta=25℃ Unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain-Source Voltage	V_{DSS}	24	V
Gate-Source Voltage	V_{GSS}	±12	V
Storage Temperature Range	T_{stg}	-55 150	℃

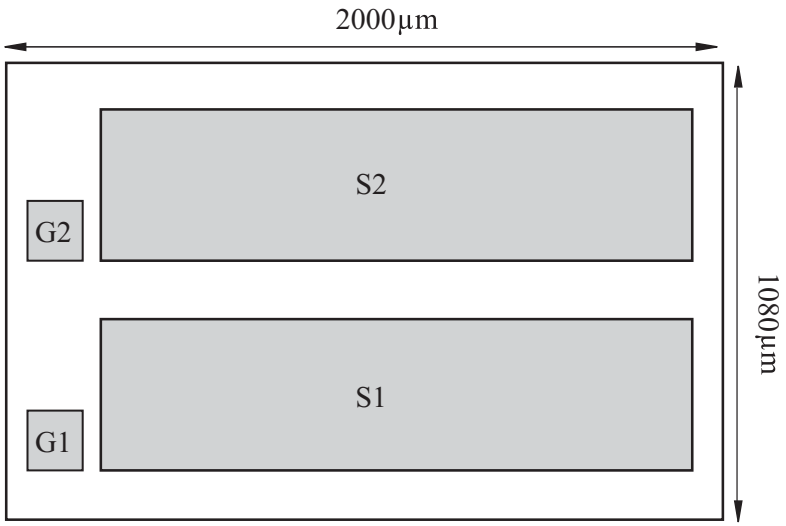
Equivalent Circuit



Electrical Characteristics (Ta=25℃ Unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 250 μA, V_{GS} = 0V	24	-	-	V
Gate to Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = ±100μA, V_{DS} = 0V	±12	±14	-	V
Drain Cut-off Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	-	-	1.0	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0V	-	-	±10	μA
Gate to Source Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250μA	0.5	1.1	1.5	V
Drain to Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 1.0A	-	12.5	16.0	mΩ
		V_{GS} = 3.9V, I_D = 1.0A	-	13.5	17.0	mΩ
		V_{GS} = 3.5V, I_D = 1.0A	-	15.0	20.0	mΩ
Gate Resistance	R_g	f=1MHz	-	3.0	-	kΩ
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V, f=1MHz	-	600	-	pF
Output Capacitance	C_{oss}		-	115	-	
Reverse Transfer Capacitance	C_{rss}		-	83	-	
Total Gate Charge	Q_g	V_{DD}=10V, V_{GS}=3.9V, I_S=4.0A	-	6.0	-	nC
Gate-Source Charge	Q_{gs}		-	0.8	-	
Gate-Drain Charge	Q_{gd}		-	2.5	-	
Source-Drain Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 1.0A	0.50	0.70	0.86	V

DIE INFORMATION



BOTTOM : COMMON DRAIN

CONTENTS	VALUE
Wafer size	8 inch notch type
Wafer thickness	180um
Front Metal	Aℓ-4um
Back Metal	Ti/Ni/Ag-1.4um
Passivation Layer	Yes
Die Size (with scribe lane)	$2000 \times 1080 \mu m^2$
Scribe lane width	60μm
Gate Pad Size	$170 \times 163 \mu m^2$
Die edge to gate Pad	93μm
Die edge to Source Pad	70μm
Gross Die(per Wafer)	13,470ea