Document Number: MC33880
Rev. 7.0, 1/2009

Configurable Octal Serial Switch with Serial Peripheral Interface I/O

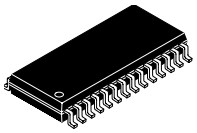
33880

HIGH/LOW-SIDE SWITCH

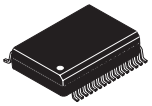
The 33880 device is an eight-output hardware-configurable high-side/low-side switch with 8-bit serial input control. Two of the outputs can be controlled directly via microcontroller for Pulse Width Modulation (PWM) applications.

The 33880 controls various inductive or incandescent loads by directly interfacing with a microcontroller.

The circuit's innovative monitoring and protection features include very low standby currents, “cascadable” fault reporting, internal 40 V output clamping for low-side configurations, internal -20 V output clamping for high-side configurations, output-specific diagnostics, and independent shutdown of outputs.



DW SUFFIX
EG SUFFIX (PB-FREE)
98ASB42345B
28-PIN SOICW



DWB SUFFIX
EW SUFFIX (PB-FREE)
98ARH99137A
32-PIN SOICW

Features

- Designed to Operate 5.5 V ≤ V_{PWR} ≤ 24.5 V
- 8-Bit SPI for Control and Fault Reporting, 3.3 V/5.0 V Compatible
- Outputs Are Current Limited (0.8 A to 2.0 A) to Drive Incandescent Lamps
- Output Voltage Clamp Is +45 V (Typical) (Low-Side Drive) and -20 V (Typical) (High-Side Drive) During Inductive Switching
- Internal Reverse Battery Protection on V_{PWR}
- Loss of Ground or Supply Will Not Energize Loads or Damage IC
- Maximum 5.0 µA I_{PWR} Standby Current at 13 V V_{PWR} up to 95°C
- $R_{DS(ON)}$ of 0.55 Ω at 25°C Typical
- Short Circuit Detect and Current Limit with Automatic Retry
- Independent Overtemperature Protection
- 32-Pin SOICW Has Pins 8, 9, 24, and 25 Grounded for Thermal Performance
- Pb-Free Packaging Designated by Suffix Code EG and EW

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33880DW/R2	-40°C to 125°C	28 SOICW
MCZ33880EG/R2		
MC33880DWB/R2		32 SOICW
MCZ33880EW/R2		

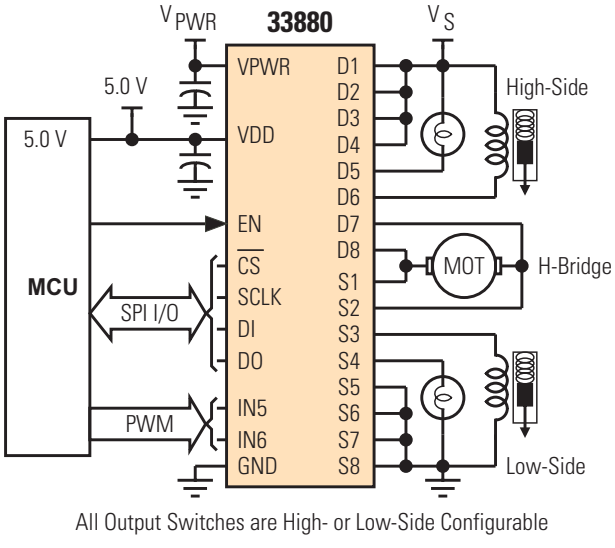


Figure 1. 33880 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

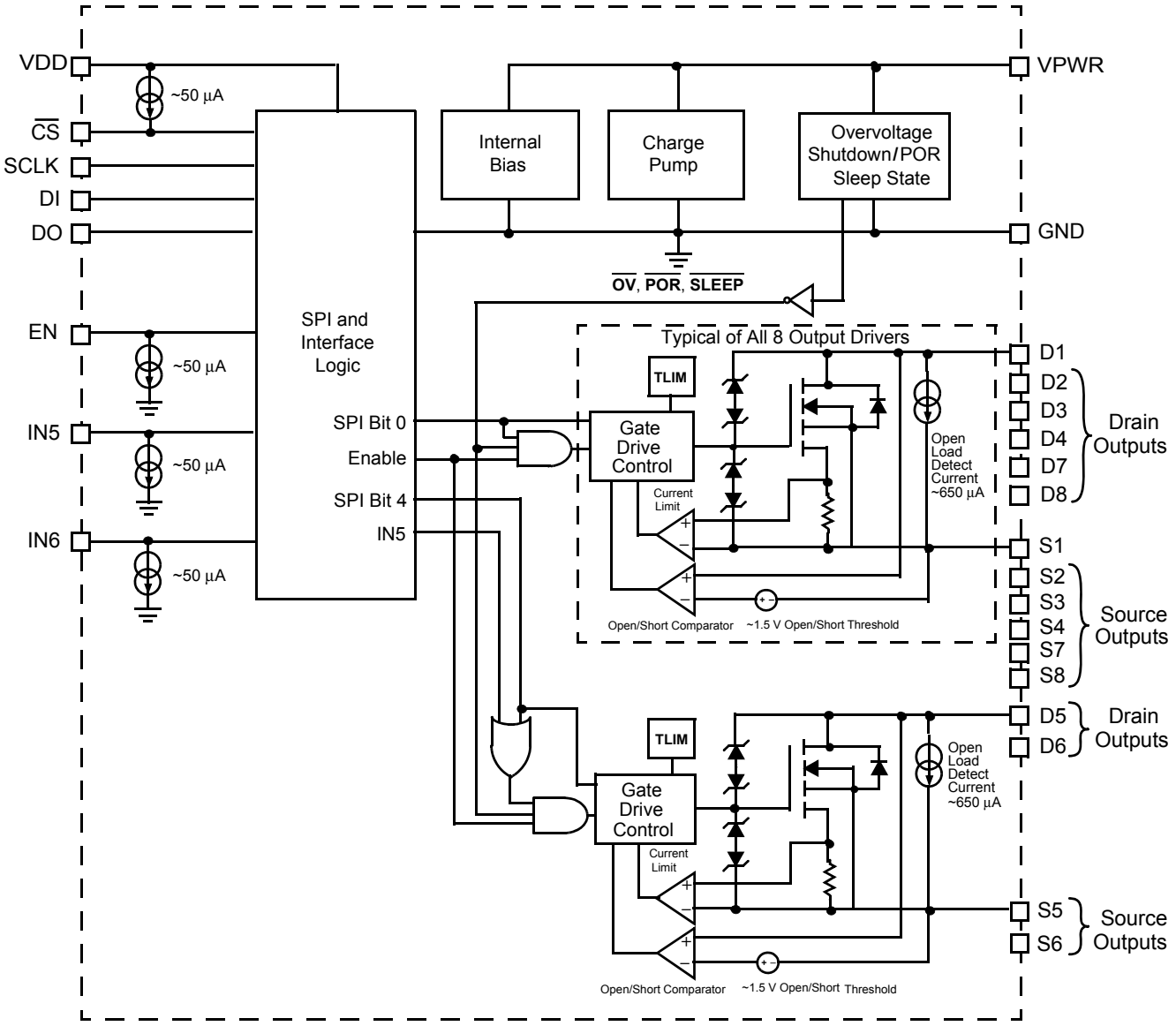


Figure 2. 33880 Simplified Internal Block Diagram

PIN CONNECTIONS

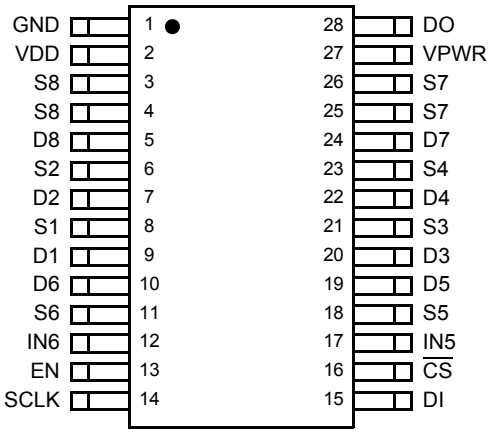


Figure 3. 28-Pin Connections

Table 1. SOICW 28-Pin Definitions

Pin Number	Pin Name	Definition
1	GND	Digital ground.
2	VDD	Logic supply voltage. Logic supply must be switched off for low current mode (V_{DD} below 3.9 V).
3, 4	S8	Output 8 MOSFET source pins.
5	D8	Output 8 MOSFET drain pin.
6	S2	Output 2 MOSFET source pin.
7	D2	Output 2 MOSFET drain pin.
8	S1	Output 1 MOSFET source pin.
9	D1	Output 1 MOSFET drain pin.
10	D6	Output 6 MOSFET drain pin.
11	S6	Output 6 MOSFET source pin.
12	IN6	PWM direct control input pin for output 6. IN6 is “OR” with SPI bit.
13	EN	Enable input. Allows control of outputs. Active high.
14	SCLK	SPI control clock input pin.
15	DI	SPI control data input pin from MCU to the 33880. Logic [1] activates output.
16	$\overline{CS}$	SPI control chip select input pin from MCU to the 33880. Logic [0] allows data to be transferred in.
17	IN5	PWM direct control input pin for output 5. IN5 is “OR” with SPI bit.
18	S5	Output 5 MOSFET source pin.
19	D5	Output 5 MOSFET drain pin.
20	D3	Output 3 MOSFET drain pin.
21	S3	Output 3 MOSFET source pin.
22	D4	Output 4 MOSFET drain pin.
23	S4	Output 4 MOSFET source pin.
24	D7	Output 7 MOSFET drain pin.
25, 26	S7	Output 7 MOSFET source pins.
27	VPWR	Power supply pin to the 33880. VPWR has internal reverse battery protection.
28	DO	SPI control data output pin from the 33880 to the MCU. DO = 0 no fault, DO = 1 specific output has fault.

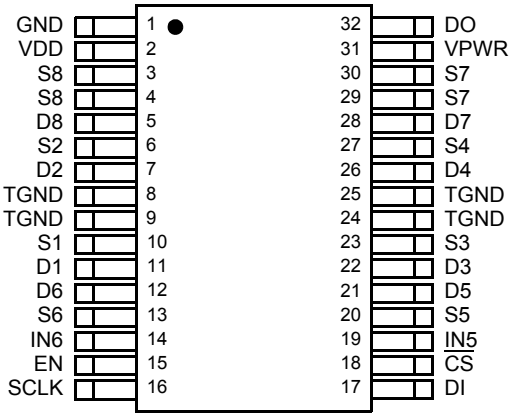


Figure 4. 32-Pin Connections

Table 2. SOICW 32-Pin Definitions

Pin Number	Pin Name	Definition
1	GND	Digital ground.
2	VDD	Logic supply voltage. Logic supply must be switched off for low current mode (V_{DD} below 3.9 V).
3, 4	S8	Output 8 MOSFET source pins.
5	D8	Output 8 MOSFETdrain pin.
6	S2	Output 2 MOSFET source pin.
7	D2	Output 2 MOSFET drain pin.
8, 9, 24, 25	TGND	Thermal Ground pins are connected internally to the substrate of the die and are used for heat transfer. Connect thermal ground pins to the PCB ground and ground plane for heat sinking.
10	S1	Output 1 MOSFET source pin.
11	D1	Output 1 MOSFET drain pin.
12	D6	Output 6 MOSFETdrain pin.
13	S6	Output 6 MOSFET source pin.
14	IN6	PWM direct control input pin for output 6. IN6 is “OR” with SPI bit.
15	EN	Enable input. Allows control of outputs. Active high.
16	SCLK	SPI control clock input pin.
17	DI	SPI control data input pin from MCU to the 33880. Logic [1] activates output.
18	$\overline{CS}$	SPI control chip select input pin from MCU to the 33880. Logic [0] allows data to be transferred in.
19	IN5	PWM direct control input pin for output 5. IN5 is “OR” with SPI bit.
20	S5	Output 5 MOSFET source pin.
21	D5	Output 5 MOSFET drain pin.
22	D3	Output 3 MOSFET drain pin.
23	S3	Output 3 MOSFET source pin.
26	D4	Output 4 MOSFET drain pin.
27	S4	Output 4 MOSFET source pin.
28	D7	Output 7 MOSFET drain pin.
29, 30	S7	Output 7 MOSFET source pins.
31	VPWR	Power supply pin to the 33880. VPWR has internal reverse battery protection.
32	DO	SPI control data output pin from the 33880 to the MCU. DO = 0 no fault, DO = 1 specific output has fault.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
VDD Supply Voltage (1)	V_{DD}	-0.3 to 7.0	V_{DC}
$\overline{CS}$, DI, DO, SCLK, IN5, IN6, and EN (1)	–	-0.3 to 7.0	V_{DC}
VPWR Supply Voltage (1)	V_{PWR}	-16 to 50	V_{DC}
Drain 1–8 (2) 5.0 mA ≤ I_{OUT} ≤ 0.3 A	–	 -18 to 40	V_{DC}
Source 1–8 (3) 5.0 mA ≤ I_{OUT} ≤ 0.3 A	–	 -28 to 40	V_{DC}
Output Voltage Clamp Low-Side Drive (4)	V_{OC}	40 to 55	V_{DC}
Output Voltage Clamp High-Side Drive (4)	V_{OC}	-15 to -25	V_{DC}
Output Clamp Energy (5)	E_{CLAMP}	50	mJ
ESD Voltage (6) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Case Temperature	T_C	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Maximum Junction Temperature	–	-40 to 150	°C
Power Dissipation (T_A = 25°C) (7) 28 SOIC, Case 751F-05 32 SOIC, Case 1324-02	P_D	 1.3 1.7	W
Thermal Resistance, Junction-to-Ambient, 28 SOIC, Case 751F-05	$R_{\theta JA}$	94	°C/W
Thermal Resistance, Junction-to-Ambient, 32 SOIC, Case 1324-02 Thermal Resistance, Junction-to-Thermal Ground Leads, 32 SOIC, Case 1324-02	$R_{\theta JA}$ $R_{\theta JL}$	70 18	°C/W
Peak Package Reflow Temperature During Reflow (8), (9)	T_{PPRT}	Note 9	°C

Notes

1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. Configured as low-side driver with 300 mA load as current limit.
3. Configured as high-side driver with 300 mA load as current limit.
4. With outputs OFF and 10 mA of test current for low-side driver, 30 mA test current for high-side driver.
5. Maximum output clamp energy capability at 150°C junction temperature using single non-repetitive pulse method.
6. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
7. Maximum power dissipation with no heatsink used.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range Fully Operational	$V_{PWR(FO)}$	5.5	–	24.5	V
Supply Current	$I_{PWR(ON)}$	–	8.0	14	mA
Sleep State Supply Current (VDD and EN = 0 V, VPWR = 16 V) Temperature = -40°C to 95°C Temperature = 95°C to 125°C	$I_{PWR(SS)}$	 – –	 2.0 5.0	 5.0 20	µA
Overvoltage Shutdown	V_{OV}	25	27	30	V
Overvoltage Shutdown Hysteresis	$V_{OV(HYS)}$	0.15	0.8	2.5	V
Logic Supply Voltage	V_{DD}	4.75	–	5.25	V
Logic Supply Current	I_{DD}	0.5	2.6	4.0	mA
Logic Supply Undervoltage Lockout Threshold	$V_{DD(UNVOL)}$	3.9	4.3	4.7	V
Logic Supply Undervoltage Hysteresis	$V_{DD(UNVOL-HYS)}$	100	150	300	mV
POWER OUTPUT					
Drain-to-Source ON Resistance (V_{PWR} = 16 V) I_{OUT} = 0.25 A, T_J = 125°C I_{OUT} = 0.25 A, T_J = 25°C I_{OUT} = 0.25 A, T_J = -40°C	$R_{DS(ON)}$	 – – –	 0.75 0.55 0.45	 1.1 0.85 0.80	Ω
Output Self-Limiting Current High-Side and Low-Side Configurations V_{PWR} = 16 V	$I_{OUT(LIM)}$	0.8	1.4	2.0	A
Output Fault Detect Threshold (10), (11) Outputs Programmed OFF	$V_{OUTth(F)}$	1.0	–	3.0	V
Output Off Open Load Detect Current (10) Outputs Programmed OFF	I_{OCO}	0.30	0.55	1.0	mA
Output Clamp Voltage Low-Side Drive I_D = 10 mA	$V_{OC(LSD)}$	40	45	55	V
Output Clamp Voltage High-Side Drive I_S = -30 mA	$V_{OC(HSD)}$	-15	-20	-25	V
Output Leakage Current High-Side and Low-Side Configuration V_{DD} = 0 V, V_{DS} = 16 V	$I_{OUT(LKG)}$	–	1.0	7.0	µA
Overtemperature Shutdown (11)	T_{LIM}	155	–	185	°C
Overtemperature Shutdown Hysteresis (11)	$T_{LIM(HYST)}$	5.0	10	15	°C

Notes
10. Output Fault Detect Thresholds with outputs programmed OFF. Output fault detect threshold are the same for output open and shorts.
11. This parameter is guaranteed by design but is not production tested.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic Voltage Thresholds (12)	$V_{INLOGIC}$	0.8	–	2.2	V
IN5, IN6, and EN Input Logic Current IN5, IN6, EN = 0 V	$I_{IN5, IN6, EN}$	-10	–	10	µA
IN5, IN6, and EN Pull-Down Current 0.8 V to V_{DD}	$I_{IN5, IN6, EN}$	30	45	100	µA
SCLK, DI, and Tri-State DO Input 0 V to V_{DD}	$I_{SCK, SI, TriSO}$	-10	–	10	µA
$\overline{CS}$ Input Current $\overline{CS}$ = V_{DD}	I_{ICS}	-10	–	10	µA
$\overline{CS}$ Pull-Up Current $\overline{CS}$ = 0 V	I_{ICS}	-30	–	-100	µA
DO High-State Output Voltage $I_{DO-HIGH}$ = -200 µA	V_{DOHIGH}	V_{DD} - 0.8	–	V_{DD}	V
DO Low-State Output Voltage $I_{DO-HIGH}$ = 1.6 mA	V_{DOLOW}	–	–	0.4	V
Input Capacitance on SCLK, DI, Tri-State DO, IN5, IN6, EN (13)	C_{IN}	–	–	20	pF

Notes
12. Upper and lower logic threshold voltage levels apply to DI, $\overline{CS}$, SCLK, IN5, IN6, and EN.
13. This parameter is guaranteed by design but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Slew Rate Low-Side Configuration (14) R_L = 620 Ω	t_R	0.1	0.5	1.2	V/µs
Output Slew Rate Low-Side Configuration (14) R_L = 620 Ω	t_F	0.1	0.5	1.2	V/µs
Output Slew Rate High-Side Configuration (14) R_L = 620 Ω	t_R	0.1	0.3	1.2	V/µs
Output Slew Rate High-Side Configuration (14) R_L = 620 Ω	t_F	0.1	0.3	1.2	V/µs
Output Turn ON Delay Time, High-Side and Low-Side Configuration (15)	$t_{DLY(ON)}$	1.0	15	50	µs
Output Turn OFF Delay Time, High-Side and Low-Side Configuration (15)	$t_{DLY(OFF)}$	1.0	30	100	µs
Output Fault Delay Time (16)	t_{FAULT}	100	–	300	µs
DIGITAL INTERFACE TIMING					
Recommended Frequency of SPI Operation	–	–	4.0	6.0	MHz
Required Low State Duration on V_{DD} for Reset (17) V_{DD} ≤ 0.2 V	t_{RESET}	–	4.0	10	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)	t_{LEAD}	100	–	–	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)	t_{LAG}	50	–	–	ns
DI to Falling Edge of SCLK (Required Setup Time)	$t_{DI(su)}$	16	–	–	ns
Falling Edge of SCLK to DI (Required Hold Time)	$t_{DI(HOLD)}$	20	–	–	ns
DI, $\overline{CS}$, SCLK Signal Rise Time (18)	$t_{R(DI)}$	–	5.0	–	ns
DI, $\overline{CS}$, SCLK Signal Fall Time (18)	$t_{F(DI)}$	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to DO Low Impedance (19)	$t_{DO(EN)}$	–	–	60	ns
Time from Rising Edge of $\overline{CS}$ to DO High Impedance (20)	$t_{DO(DIS)}$	–	–	60	ns
Time from Rising Edge of SCLK to DO Data Valid (21)	t_{VALID}	–	25	60	ns

Notes
14. Output Rise and Fall time respectively measured across a 620 Ω resistive load at 10 to 90 percent and 90 to 10 percent voltage points.
15. Output turn ON and OFF delay time measured from 50 percent rising edge of $\overline{CS}$ to 90 and 10 percent of initial voltage.
16. Duration of fault before fault bit is set. Duration between access times must be greater than 300 µs to read faults.
17. This parameter is guaranteed by design but is not production tested.
18. Rise and Fall time of incoming DI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
19. Time required for output status data to be available for use at DO pin.
20. Time required for output status data to be terminated at DO pin
21. Time required to obtain valid data out from DO following the rise of SCLK.

TIMING DIAGRAMS

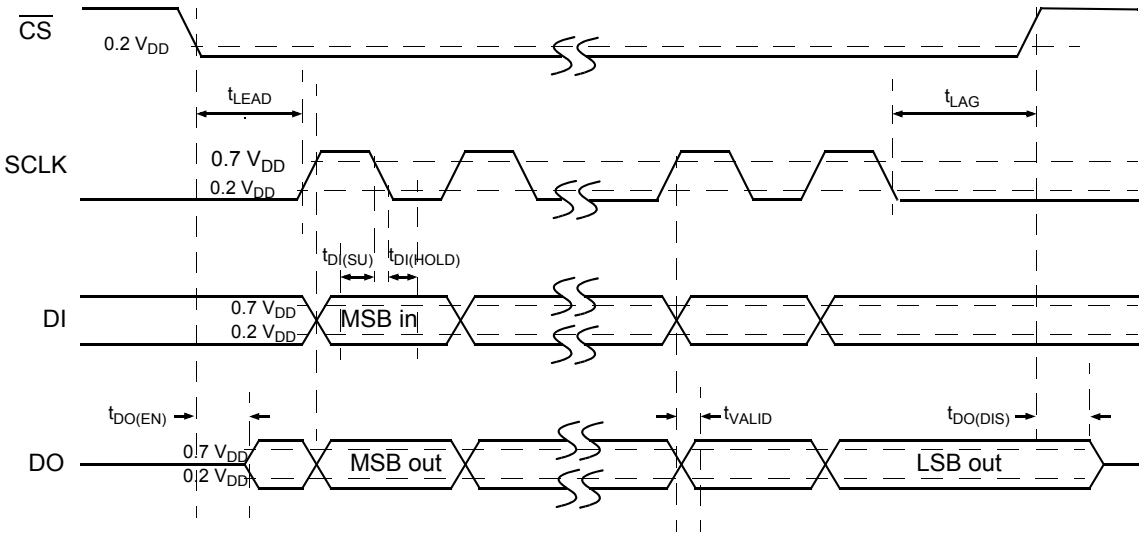
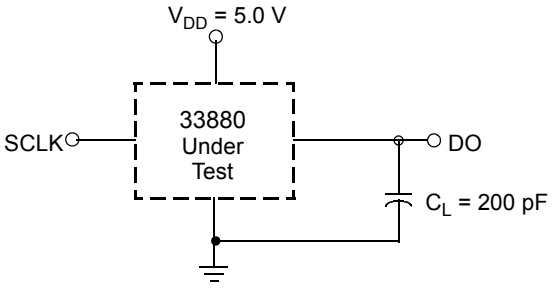
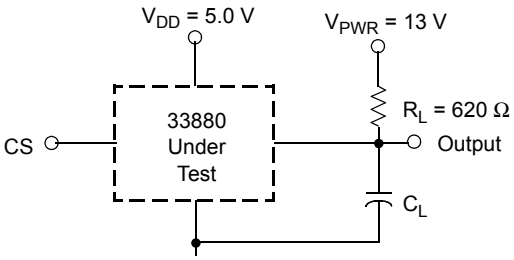


Figure 5. SPI Timing Diagram



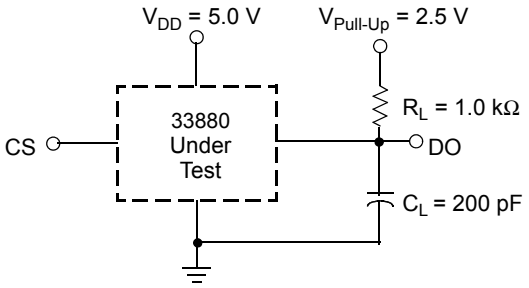
NOTE: C_L represents the total capacitance of the test fixture and probe.

Figure 6. Valid Data Delay Time and Valid Time Test Circuit



NOTE: C_L represents the total capacitance of the test fixture and probe.

Figure 8. Switching Time Test Circuit



NOTE: C_L represents the total capacitance of the test fixture and probe.

Figure 7. Enable and Disable Time Test Circuit

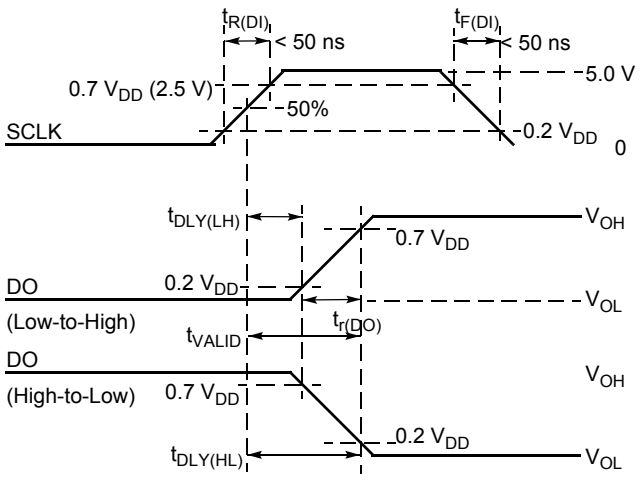


Figure 9. Valid Data Delay Time and Valid Time Waveforms

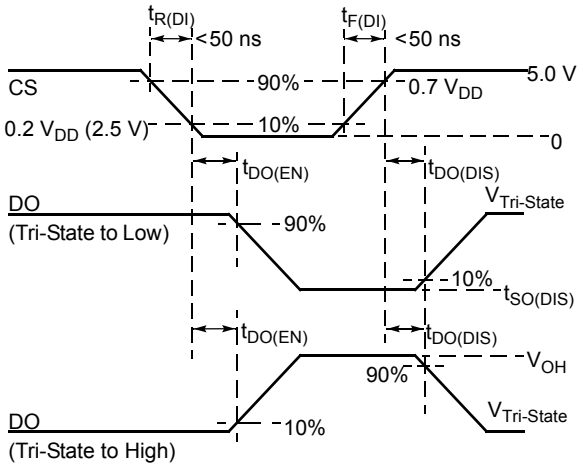


Figure 10. Enable and Disable Time Waveforms

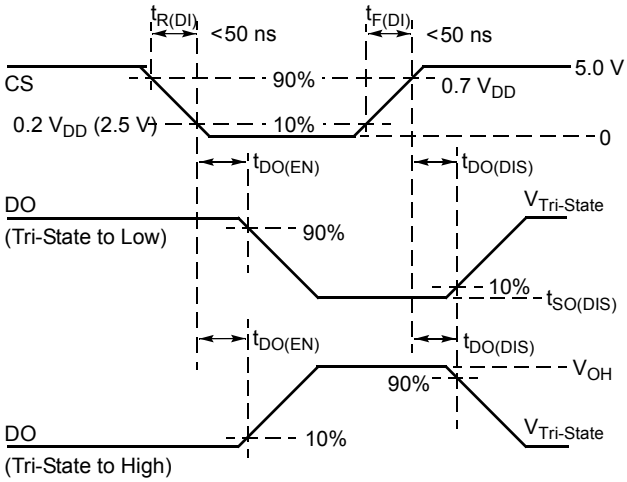


Figure 11. Turn-ON/OFF Waveforms

TYPICAL ELECTRICAL CHARACTERISTICS

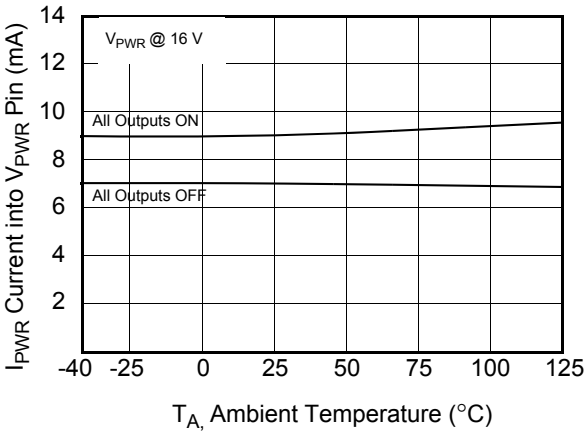


Figure 12. I_{PWR} vs. Temperature

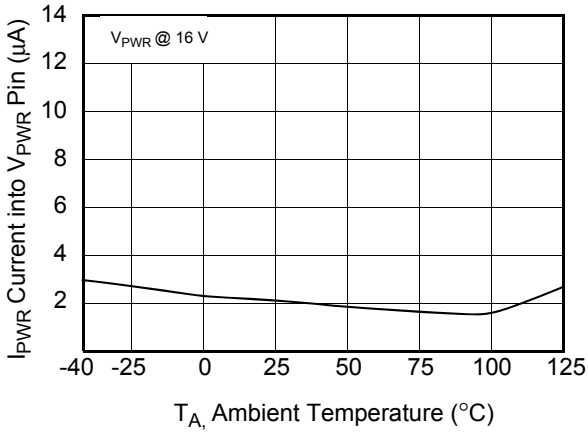


Figure 13. Sleep State I_{PWR} vs. Temperature

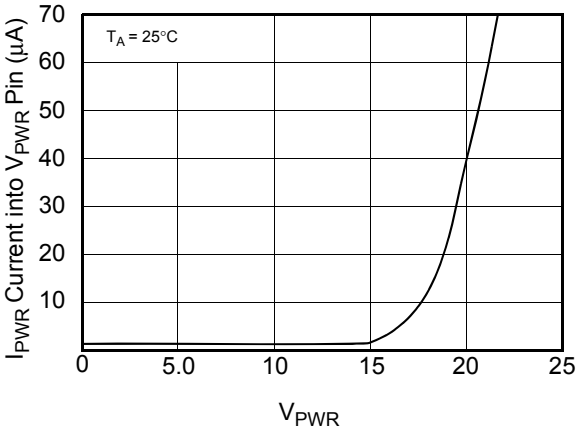


Figure 14. Sleep State I_{PWR} vs. V_{PWR}

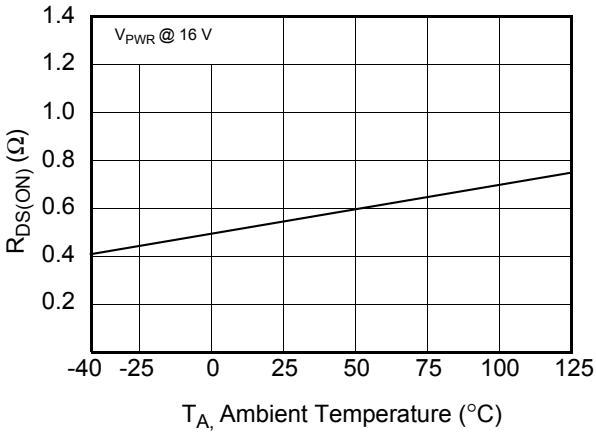


Figure 15. $R_{DS(ON)}$ vs. Temperature @ 250 mA

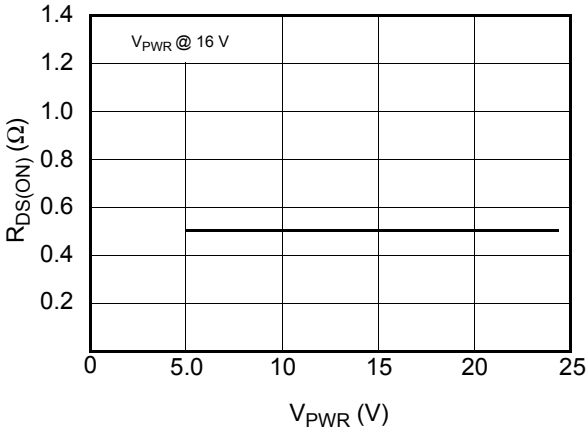


Figure 16. $R_{DS(ON)}$ vs. V_{PWR} @ 250 mA

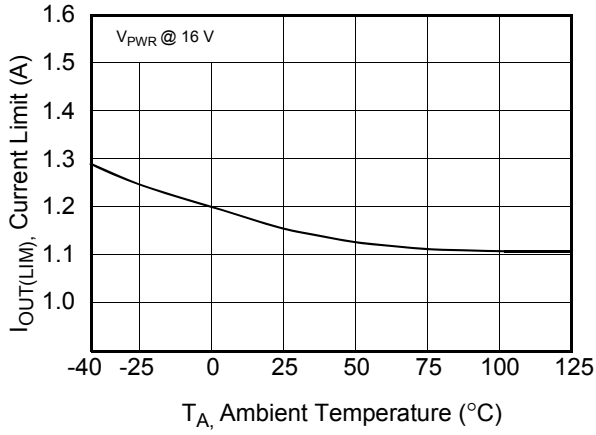


Figure 17. Current Limit $I_{OUT(LIM)}$ vs. Temperature

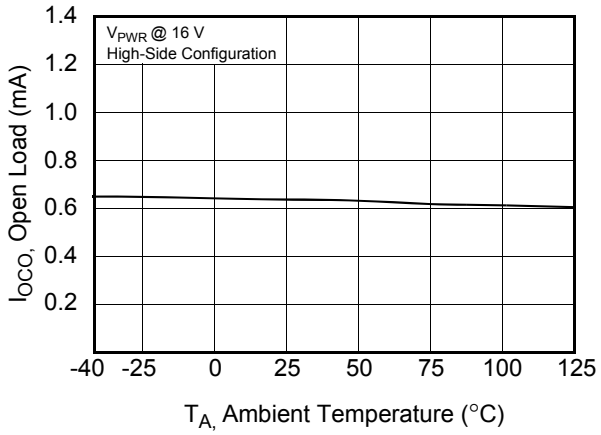


Figure 18. Open Load Detect Current vs. Temperature

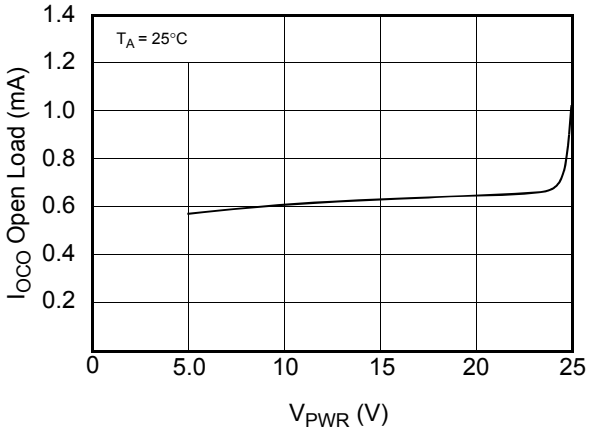


Figure 19. Open Load Detect Current vs. V_{PWR}

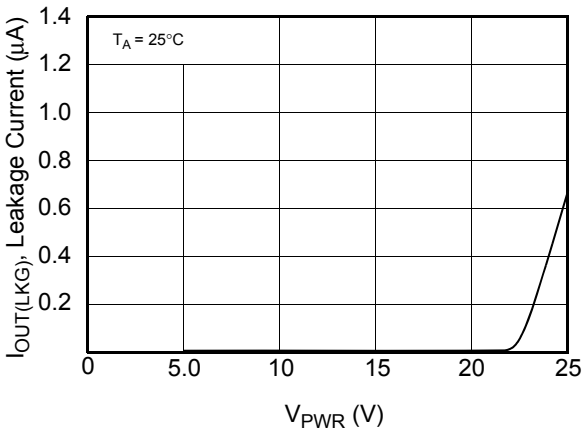


Figure 20. Sleep State Output Leakage vs. V_{PWR}

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33880 is an eight-output hardware configurable power switch with 8-bit serial control. The 33880 incorporates SMARTMOS™ 5 technology with CMOS logic, bipolar/MOS analog circuitry, and independent double diffused DMOS power output transistors. Many benefits are realized as a direct result of using this mixed technology. A simplified internal block diagram of the 33880 is shown in Figure 2, page 2.

The 33880 device uses high-efficiency updrain power DMOS output transistors exhibiting low drain-to-source ON resistance values ($R_{DS(ON)} \leq 0.55\ \Omega$ at 25°C) and dense CMOS control logic. All outputs have independent voltage clamps to provide fast inductive turn-off and transient protection. Operational bias currents of less than 4.0 mA on V_{DD} and 12 mA on V_{PWR} with any combination of outputs ON are a direct result of using SMARTMOS™ 5 technology.

FUNCTIONAL PIN DESCRIPTION

CHIP SELECT ($\overline{CS}$)

The system MCU selects the 33880 to communicate through the use of the $\overline{CS}$ pin. Whenever the pin is in a logic low state, data can be transferred from the MCU to the 33880 device and vice versa. Clocked-in data from the MCU is transferred from the 33880 shift register and latched into the power outputs on the rising edge of the $\overline{CS}$ signal. On the falling edge of the $\overline{CS}$ signal, output status information is transferred from the power outputs status register into the device's shift register. The falling edge of $\overline{CS}$ enables the DO output driver. Whenever the $\overline{CS}$ pin goes to a logic low state, the DO pin output is enabled, thereby allowing information to be transferred from the 33880 to the MCU. To avoid any spurious data, it is essential the high-to-low transition of the $\overline{CS}$ signal occurs only when SCLK is in a logic low state.

SYSTEM CLOCK (SCLK)

The system clock pin (SCLK) clocks the internal shift registers of the 33880. The serial data input (DI) is latched into the input shift register on the falling edge of the SCLK. The serial data output pin (DO) shifts data out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to guarantee validity of data. It is essential the SCLK pin be in a logic low state whenever chip select pin ($\overline{CS}$) makes any transition. For this reason, it is recommended the SCLK pin is commanded to a logic low state when the device is not accessed ($\overline{CS}$ in logic high state). When the $\overline{CS}$ is in a logic high state, any signal at the SCLK and DI pin is ignored and the DO is tri-stated (high impedance).

DATA INPUT (DI)

This pin is used for serial instruction data input. DI information is latched into the input register on the falling edge of SCLK. A logic high state present on DI will program a specific output on. The specific output will turn on with the rising edge of the $\overline{CS}$ signal. Conversely, a logic low state present on the DI pin will program the output *off*. The specific output will turn *off* with the rising edge of the $\overline{CS}$ signal. To program the eight outputs of the 33880 device *on* or *off*, enter the DI pin beginning with Output 8, followed by Output 7, Output 6, and so on to Output 1. For each falling edge of the SCLK while $\overline{CS}$ is logic low, a data bit instruction (*on* or *off)* is loaded into the shift register per the data bit DI state. Eight bits of entered information fills the shift register. To preserve data integrity, do not transition DI as SCLK transitions from a high to low logic state.

DATA OUTPUT (DO)

The serial data output (DO) pin is the output from the shift register. The DO pin remains tri-state until the $\overline{CS}$ pin goes to a logic low state. All faults on the 33880 device are reported as logic [1] through the DO data pin. Regardless of the configuration of the driver, open loads and shorted loads are reported as logic [1]. Conversely, normal operating outputs with non-faulted loads are reported as logic [0]. The first positive transition of SCLK will make output eight status available on DO pin. Each successive positive clock will make the next output status available. The DI/DO shifting of data follows a first-in-first-out protocol with both input and output words transferring the most significant bit (MSB) first.

ENABLE (EN)

The EN pin on the 33880 device either enables or disables the internal charge pump. The EN pin must be high for this device to enhance the gates of the output drivers, perform fault detection, and reporting. Active outputs during a low transition of the EN pin will become active again when the EN transitions high. If this feature is not required, it is recommended the EN pin be connected to V_{DD}.

COMMAND INPUT (IN5 AND IN6)

The IN5 and IN6 pins command inputs allowing outputs five and six to be used in PWM applications. IN5 and IN6 pins are ORed with the SPI communication input. For SPI control of outputs five and six, the IN5 and IN6 pins should be grounded or held low by the microprocessor. In the same manner, when using the PWM feature the SPI port must command the outputs *off*. Maximum PWM frequency for each output is 2.0 kHz.

LOGIC POWER (VDD)

The V_{DD} pin supplies logic power to the 33880 device and is used for power-on reset (POR). To achieve low standby current on V_{PWR} supply, power must be removed from the V_{DD} pin. The device will be in reset with all drivers off when V_{DD} is below 3.9 V_{DC}.

OPEN DRAIN OUTPUT (D1–D8)

The D1–D8 pins are the open drain outputs of the 33880. For High-Side Drive configurations, the drain pins are connected to battery supply. In Low-Side Drive configurations, the drain pins are connected to the low side of the load. All outputs may be configured individually as desired. When Low-Side Drive is used, the 33880 limits the positive transient for inductive loads to 45 V.

SOURCE OUTPUT (S1–S8)

The S1–S8 pins are the source outputs of the 33880. For High-Side Drive configurations, the source pins are connected directly to the load. In Low-Side Drive configurations the source is connected to ground. All outputs may be configured individually as desired. When High-Side drive is used, the 33880 will limit the negative transient for inductive loads to -20 V.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

MCU INTERFACE DESCRIPTION

In operation, the 33880 functions as an eight-output serial switch serving as a microcontroller (MCU) bus expander and buffer, with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions. This device directly interfaces to an MCU using a Serial Peripheral Interface (SPI) for control and diagnostic readout. Figure 21 and Figure 24, page 16, illustrate the basic SPI configuration between an MCU and one 33880.

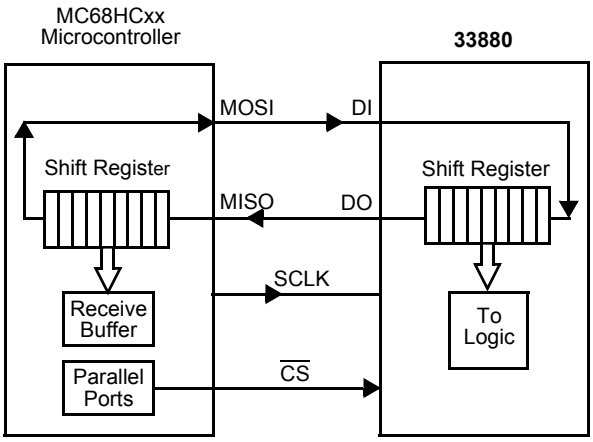


Figure 21. SPI Interface with Microcontroller

All inputs are compatible with 5.0 V and 3.3 V CMOS logic levels and incorporate positive logic. Whenever an input is programmed to a logic low state (<0.8 V) the corresponding output will be OFF. Conversely, whenever an input is programmed to a logic high state (>2.2 V), the output being controlled will be ON. Diagnostics are treated in a similar manner. Outputs with a fault will feedback (via DO) to the microcontroller as a logic [1] while normal operating outputs will provide a logic [0].

Figure 22 illustrates the Daisy Chain configuration using the 33880. Data from the MCU is clocked daisy chain through each device while the Chip Select ($\overline{CS}$) bit is commanded low by the MCU. During each clock cycle output status from the daisy chain, the 33880 is being transferred to the MCU via the Master In Slave Out (MISO) line. On rising edge of $\overline{CS}$ data stored in the input register is then transferred to the output driver.

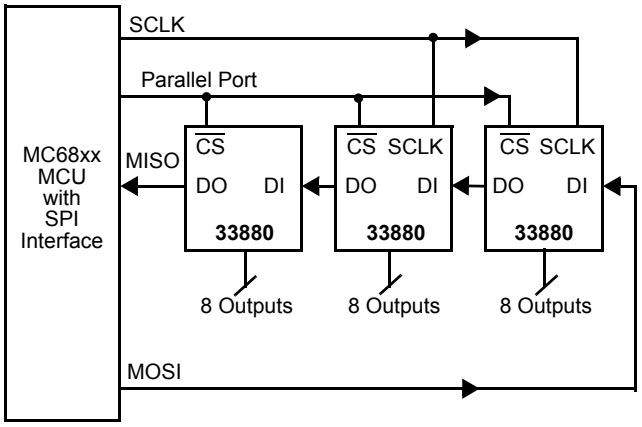


Figure 22. 33880 SPI System Daisy Chain

Multiple 33880 devices can be controlled in a parallel input fashion using the SPI. Figure 23 illustrates 24 loads being controlled by three dedicated parallel MCU ports used for chip select.

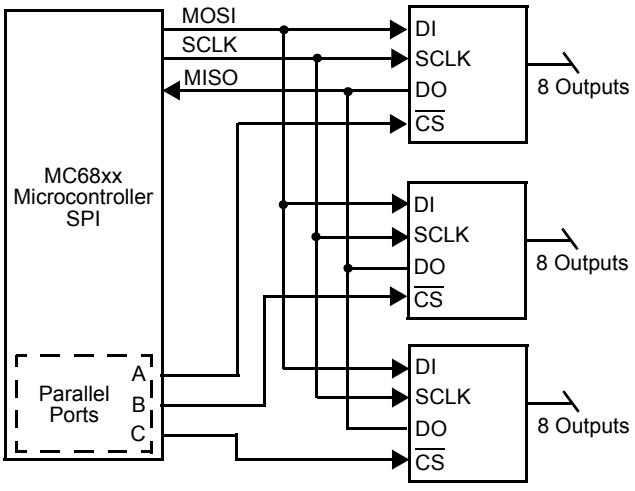
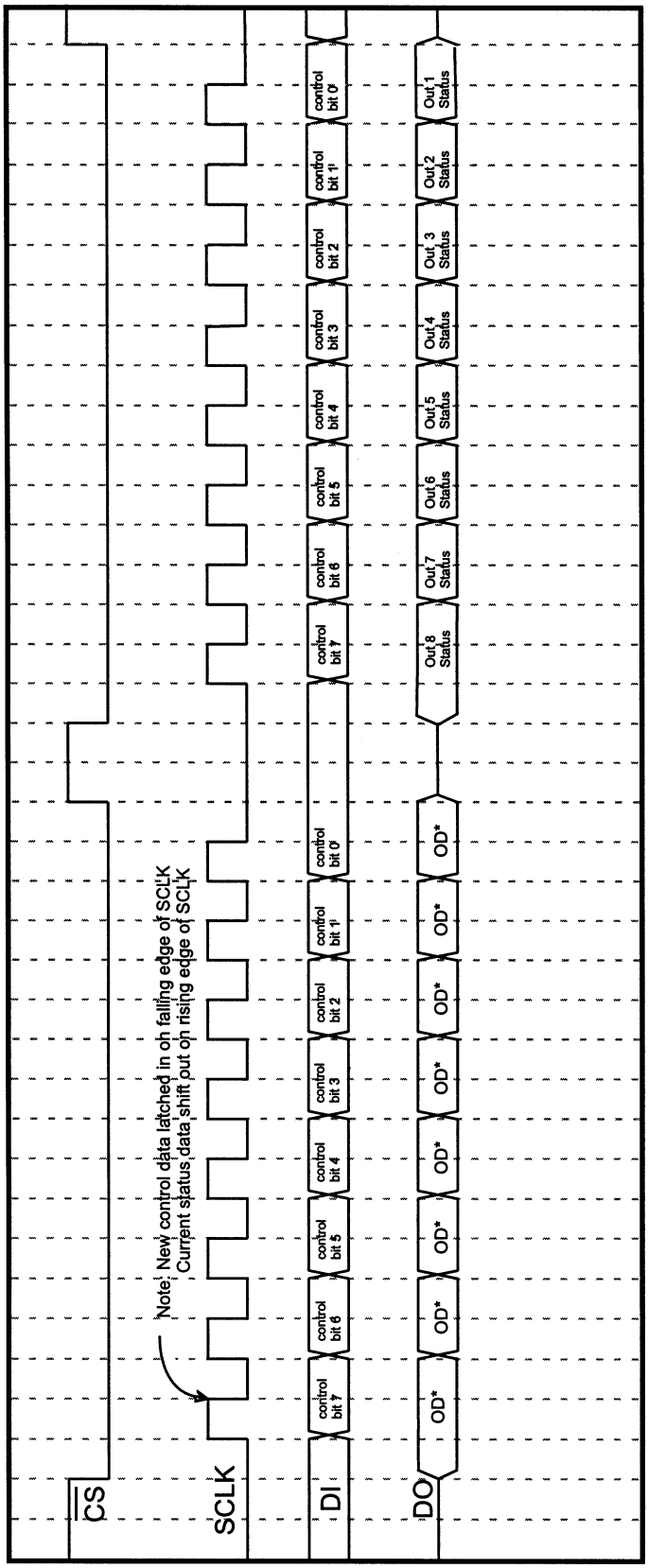


Figure 23. Parallel Input SPI Control



NOTES: 1. Most Significant Bit is clocked in first and corresponds to output 8.
2. OD* corresponds to Old Databits.

Figure 24. Data Transfer Timing

POWER CONSUMPTION

The 33880 device has been designed with one sleep and one operational mode. In the sleep mode ($V_{DD} \leq 2.0$ V), the current consumed by the VPWR pin is less than 25 μA. To place the 33880 in the sleep mode, turn all outputs off, then remove power from VDD and the EN (enable) input pin. Prior to removing power from the device, it is recommended all control inputs from the microcontroller are low. During normal operation, 4.0 mA will be drawn from the V_{DD} supply and 12 mA from the V_{PWR} supply.

PARALLELING OF OUTPUTS

Using MOSFETs as output switches allows the connection of any combination of outputs together. $R_{DS(ON)}$ of MOSFETs have an inherent positive temperature coefficient, providing balanced current sharing between outputs without destructive operation. The device can even be operated with all outputs tied together. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $R_{DS(ON)}$ while the outputs OFF open load detect currents and the output current limits increase correspondingly (by a factor of eight if all outputs are paralleled). Paralleling outputs from two or more different IC devices are possible but not recommended.

FAULT LOGIC OPERATION

Fault logic of the 33880 device has been greatly simplified over other devices using SPI communications. As command word one is being written into the shift register, a fault status word is being simultaneously written out and received by the MCU. Regardless of the configuration, with no outputs faulted, all status bits being received by the MCU will be zero. When outputs are faulted (off state open circuit or on state short circuit/overtemperature), the status bits being received by the MCU will be one. The distinction between open circuit fault and short circuit/overtemperature is completed via the command word. For example, when a zero command bit is sent and a one fault is received in the following word, the fault is open/short-to-battery for high-side drive or open/short to ground for low-side drive. In the same manner, when a one command bit is sent and a one fault is received in the following word the fault is a short-to-ground/overtemperature for high-side drive or short-to-battery/overtemperature for low-side drive. The timing between two write words must be greater than 300 μs to allow adequate time to sense and report the proper fault status.

SPI INTEGRITY CHECK

It is recommended that one check the integrity of the SPI communication with the initial power-up of the VDD and EN pins. After initial system start-up or reset, the MCU will write one 16-bit pattern to the 33880. The first eight bits read by the MCU will be the fault status of the outputs, while the second eight bits will be the first byte of the bit pattern. Bus integrity is confirmed by the MCU receiving the same bit pattern it sent. Please note that the second byte the MCU sends to the device is the command byte and will be transferred to the outputs with rising edge of $\overline{CS}$.

OVERTEMPERATURE FAULT

Overtemperature detect and shutdown circuits are specifically incorporated for each individual output. The shutdown following an overtemperature condition is independent of the system clock or any other logic signal. Each independent output shuts down at 155°C to 185°C. When an output shuts down due to an overtemperature fault, no other outputs are affected. The MCU recognizes the fault by a one in the fault status register. After the 33880 device has cooled below the switch point temperature and 15°C hysteresis, the output will activate unless told otherwise by the MCU via SPI to shut down.

OVERVOLTAGE FAULT

An overvoltage condition on the VPWR pin will cause the device to shut down all outputs until the overvoltage condition is removed. When the overvoltage condition is removed, the outputs will resume their previous state. This device does not detect an overvoltage on the VDD pin. The overvoltage threshold on the VPWR pin is specified as 25 V to 30 V with 1.0 V typical hysteresis. A VPWR overvoltage detect is *global*, causing all outputs to be turned OFF.

OUTPUT OFF OPEN LOAD FAULT

An output OFF open load fault is the detection and reporting of an *open* load when the corresponding output is disabled (input bit programmed to a logic low state). The output OFF open load fault is detected by comparing the drain-to-source voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

An output off open load fault is indicated when the drain-to-source voltage is less than the output threshold voltage (V_{THRES}) of 1.0 V to 3.0 V. Hence, the 33880 will declare the load *open* in the OFF state when the V_{DS} is less than 1.0 V.

This device has an internal 650 μA current source connected from drain to source of the output MOSFET. This prevents either configuration of the driver from having a floating output. To achieve low sleep mode quiescent currents, the open load detect current source of each driver is switched off when V_{DD} is removed.

During output switching, especially with capacitive loads, a false output OFF open load fault may be triggered. To prevent this false fault from being reported, an internal fault filter of 100 μs to 300 μs is incorporated. A false fault reporting is a function of the load impedance, $R_{DS(ON)}$, C_{OUT} of the MOSFET, as well as the supply voltage, V_{PWR}. The rising edge of $\overline{CS}$ triggers the built-in fault delay timer. The timer will time out before the fault comparator is enabled and the fault is detected. Once the condition causing the open load fault is removed, the device will resume normal operation. The open load fault however, will be latched in the output DO register for the MCU to read.

SHORTED LOAD FAULT

A shorted load (overcurrent) fault can be caused by any output being shorted directly to supply or an output causing the device to current limit (linear short).

There are two safety circuits progressively in operation during load short conditions providing system protection:

1. The device's output current is monitored in an analog fashion using SENSEFET™ approach and current limited.
2. The device's output thermal limit is sensed and when attained causes only the specific faulted output to shut down. The output will remain off until cooled. The device will then reassert the output automatically. The cycle will continue until the fault is remove or the command bit instructs the output off.

UNDERVOLTAGE SHUTDOWN

An undervoltage V_{DD} condition will result in the global shutdown of all outputs. The undervoltage threshold is between 3.9 V and 4.6 V. When V_{DD} goes below the threshold, all outputs are turned OFF and the Fault Status (FS) register is cleared. As V_{DD} returns to normal levels, the FS register will resume normal operation.

An undervoltage condition at the VPWR pin will not cause output shutdown and reset. When V_{PWR} is between 5.5 V and 9.0 V, the output will operate per the command word. However, the status as reported by the serial data output (DO) pin may not be accurate below 9.0 V V_{PWR}. Proper operation at V_{PWR} voltages below 5.5 V cannot be guaranteed.

OUTPUT VOLTAGE CLAMP

Each output of the 33880 incorporates an internal voltage clamp to provide fast turn-off and transient protection of each output. Each clamp independently limits the drain-to-source voltage to 45 V for low-side drive configurations and -20 V for high-side drive configurations (see Figure 25). The total energy clamped (E_J) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}).

Characterization of the output clamps, using a single pulse non-repetitive method at 0.3 A, indicates the maximum energy to be 50 mJ at 150°C junction temperature per output.

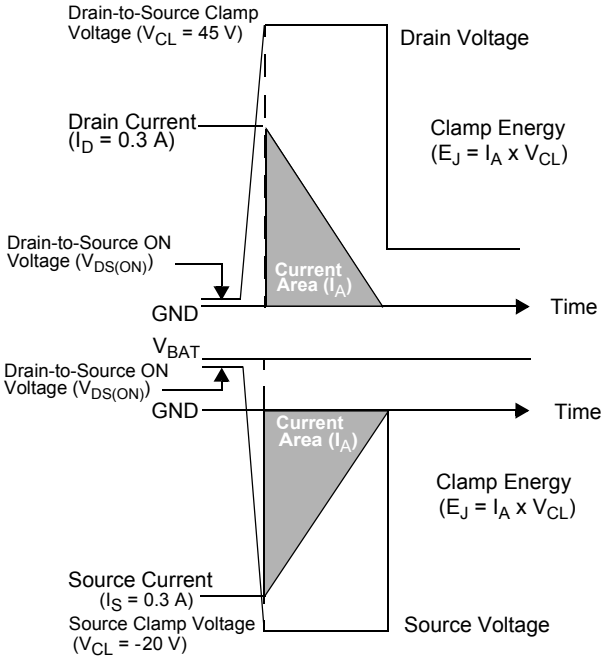


Figure 25. Output Voltage Clamping

SPI CONFIGURATIONS

The SPI configuration on the 33880 device is consistent with other devices in the OSS family. This device may be used in serial SPI or parallel SPI with the 33291 and 33298. Different SPI configurations may be provided. For more information, contact Analog Products Division.

REVERSE BATTERY

The 33880 has been designed with reverse battery protection on the VPWR pin. However, the device does not protect the load from reverse battery. During the reverse battery condition, current will flow through the load via the output MOSFET substrate diode. Under this circumstance relays may energize and lamps will turn on. If load reverse battery protection is desired, a diode must be placed in series with the load.

LOGIC COMMANDS AND REGISTERS

On each SPI communication, an 8-bit command word is sent to the 33880 and an 8-bit fault word is received from the 33880. The Most Significant Bit (MSB) is sent and received first (see below).

MSB							**LSB**
OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1

Command Register Definition:
0 = Output Command Off
1 = Output Command On

Fault Register Definition:
0 = No fault
1 = Fault.

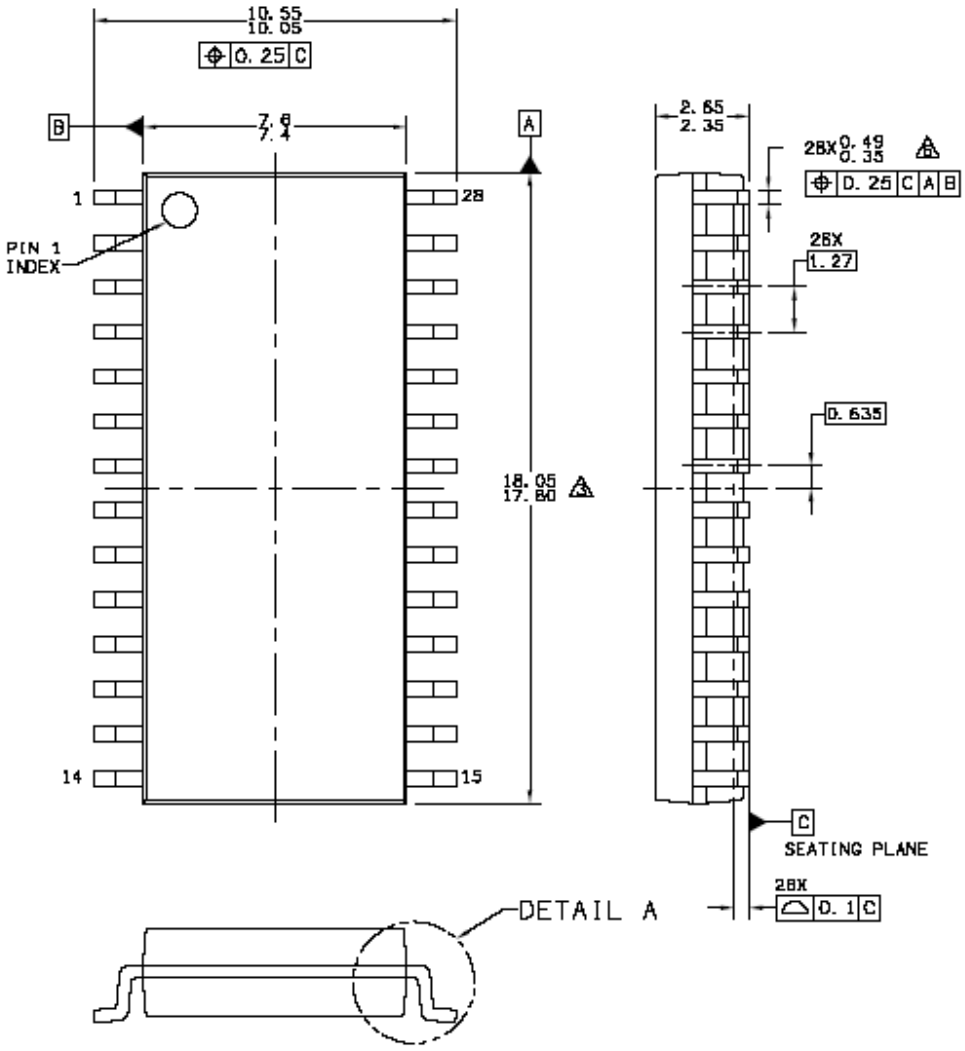
Table 6. Fault Operation

SERIAL OUTPUT (SO) PINS REPORTS	
Overtemperature	Fault reported by Serial Output (DO) pin.
Overcurrent	DO pin reports short to battery/supply or overcurrent condition.
Output ON Open Load Fault	Not reported.
Output OFF Open Load Fault	DO pin reports output OFF open load condition.
DEVICE SHUTDOWNS	
Overvoltage	Total device shutdown at V_{PWR} = 25 V to 30 V. Resumes normal operation with proper voltage. All outputs assuming the previous state upon recovery from overvoltage.
Overtemperature	Only the output experiencing an overtemperature fault shuts down. Output assumes previous state upon recovery from overtemperature.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using "**98ASB42345B**".

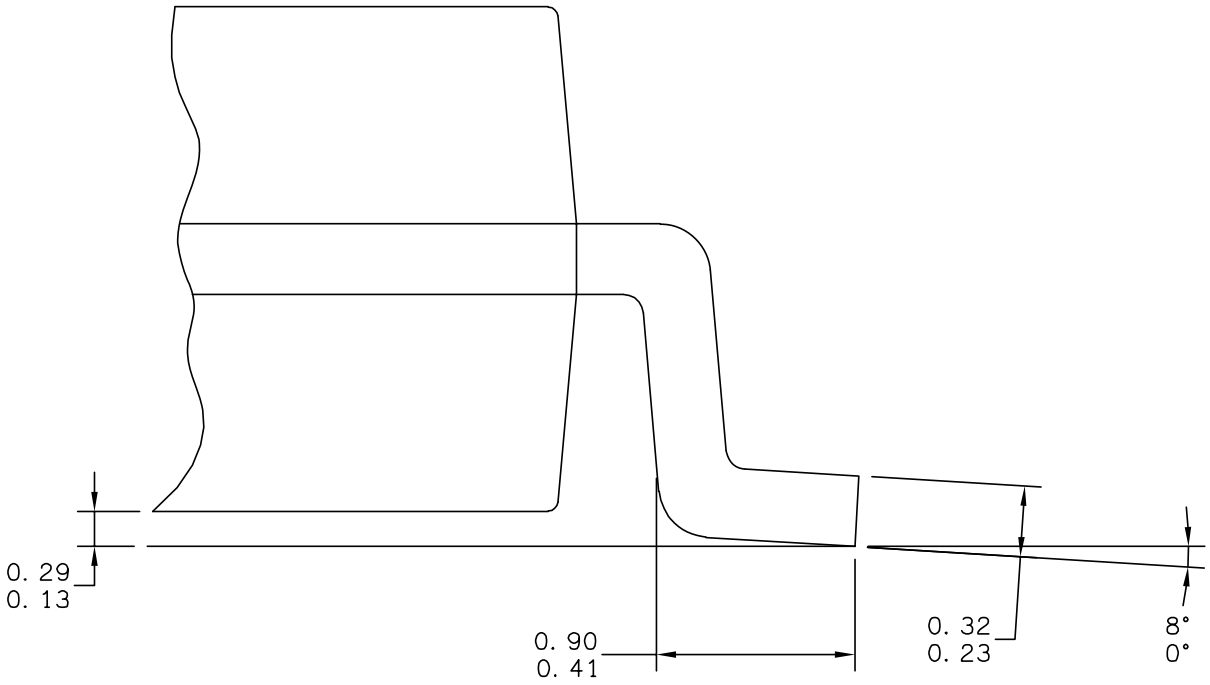


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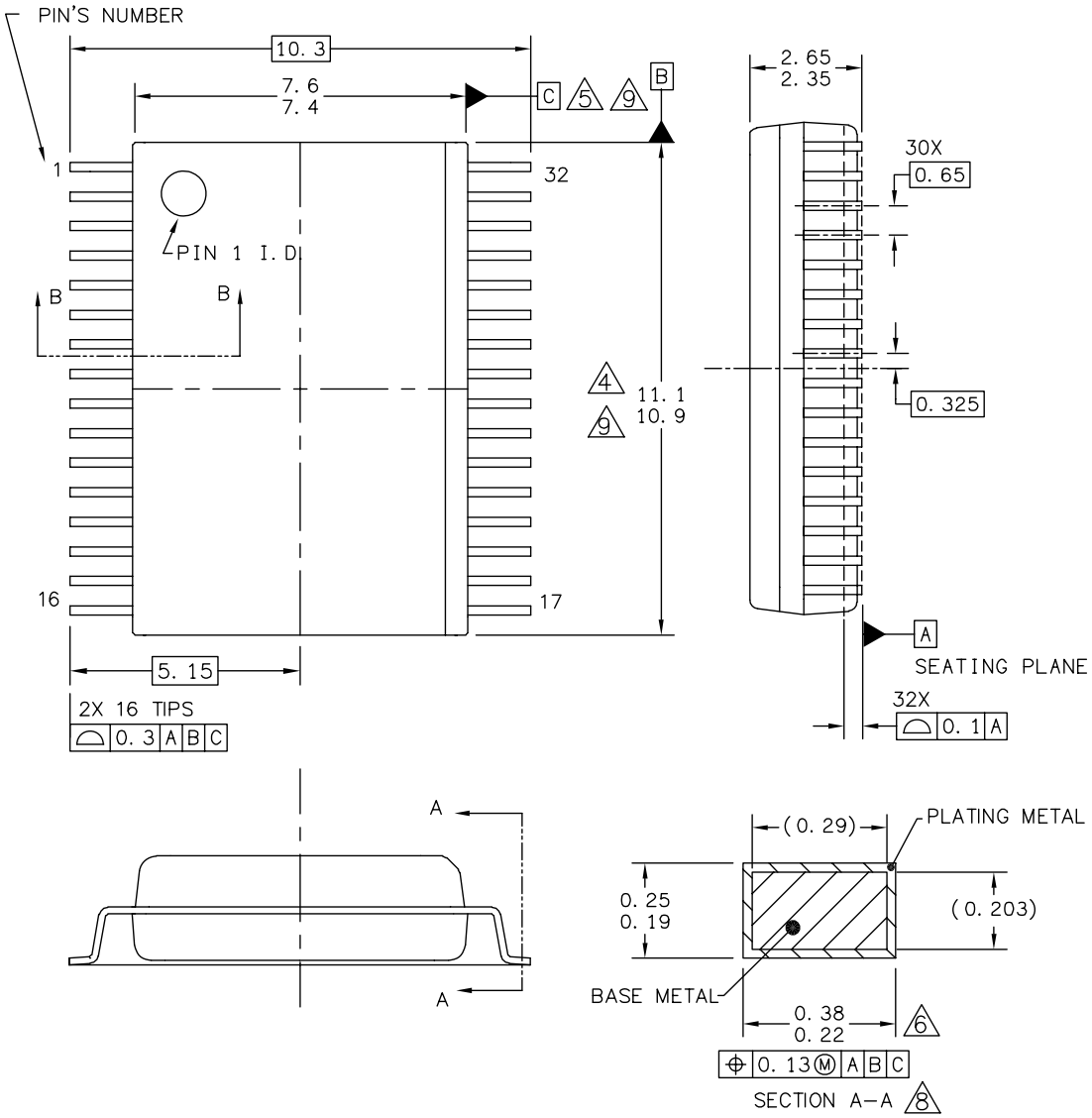
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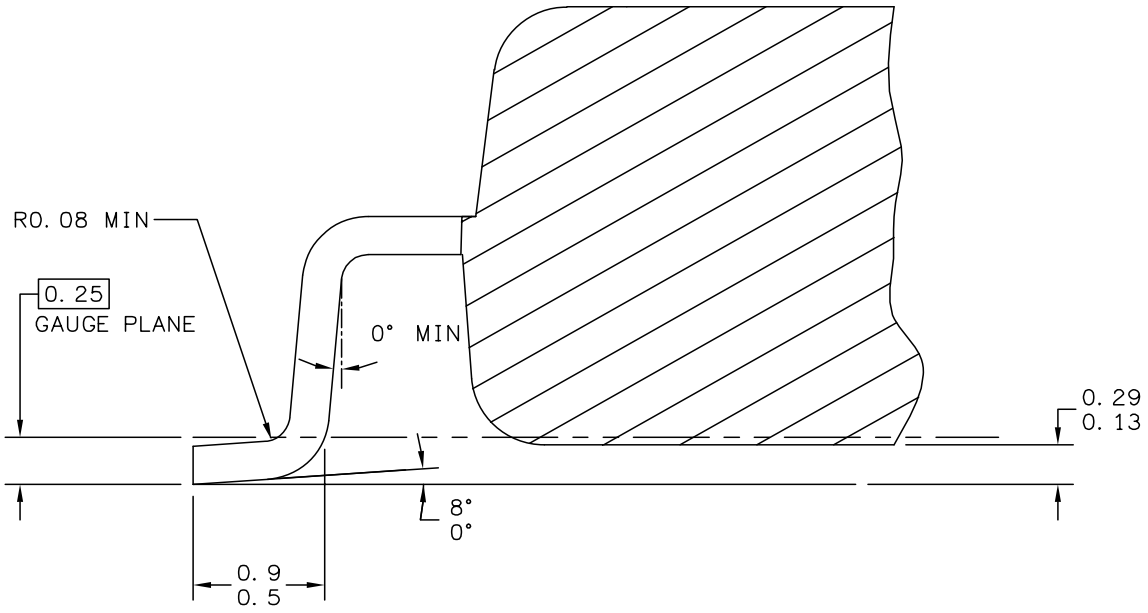
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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	6/2006	• Implemented Revision History page • Converted to Freescale format and adjusted content to prevailing form and style
5.0	6/2007	• Removed MC33880EG/R2 and MC33880EK/R2 from the ordering information and added MCZ33880EG/R2 and MCZ33880EW/R2. • Added Peak Package Reflow Temperature During Reflow (8), (9) • Updated data sheet to current format.
6	5/2008	• Changed 32 pin SOICW, pins 8, 9, 24, 25 from GND to TGND on page 4.
7.0	1/2009	• Corrected Notes for Peak Package Reflow in Maximum Rating Table.

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