DESCRIPTION

PT6520 is a dot matrix LCD driver IC. The bit addressable display data which is sent from a microcomputer is stored in a build-in display data RAM and generates the LCD signal.

The PT6520 incorporates innovative circuit design strategies to assure very low current dissipation and a wide range of operating voltages. The PT6520 permits the user to implement high-performance handy systems operating from a miniature battery.

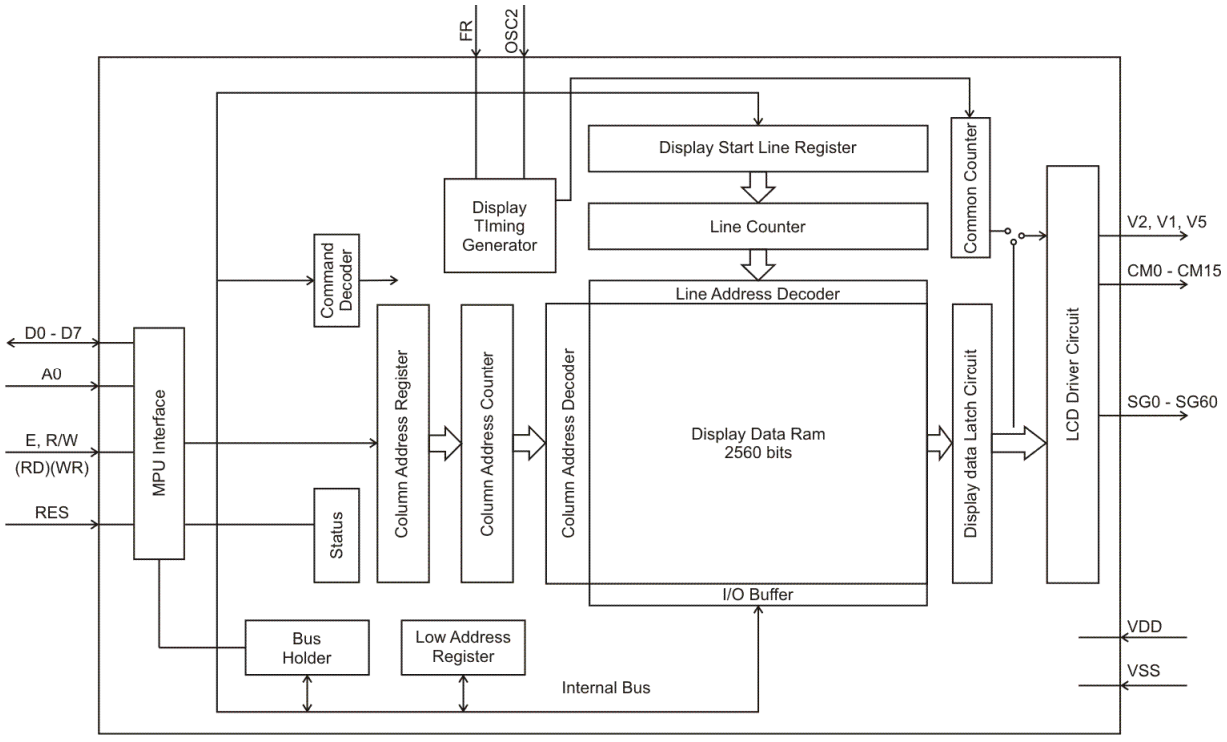
FEATURES

- CMOS technology
- 8-bit data interface
- 61 segment output
- 16 common output
- Duty cycle – PT6520 – 1/16 ~ 1/32
- 2560 bits built-in display data RAM
- Master/Slave operation
- Low power: 30μW
- LCD voltage: 3.5 ~ 13V
- Power supply: 2.4 ~ 7V
- Available in 100 pins, QFP & C.O.B.

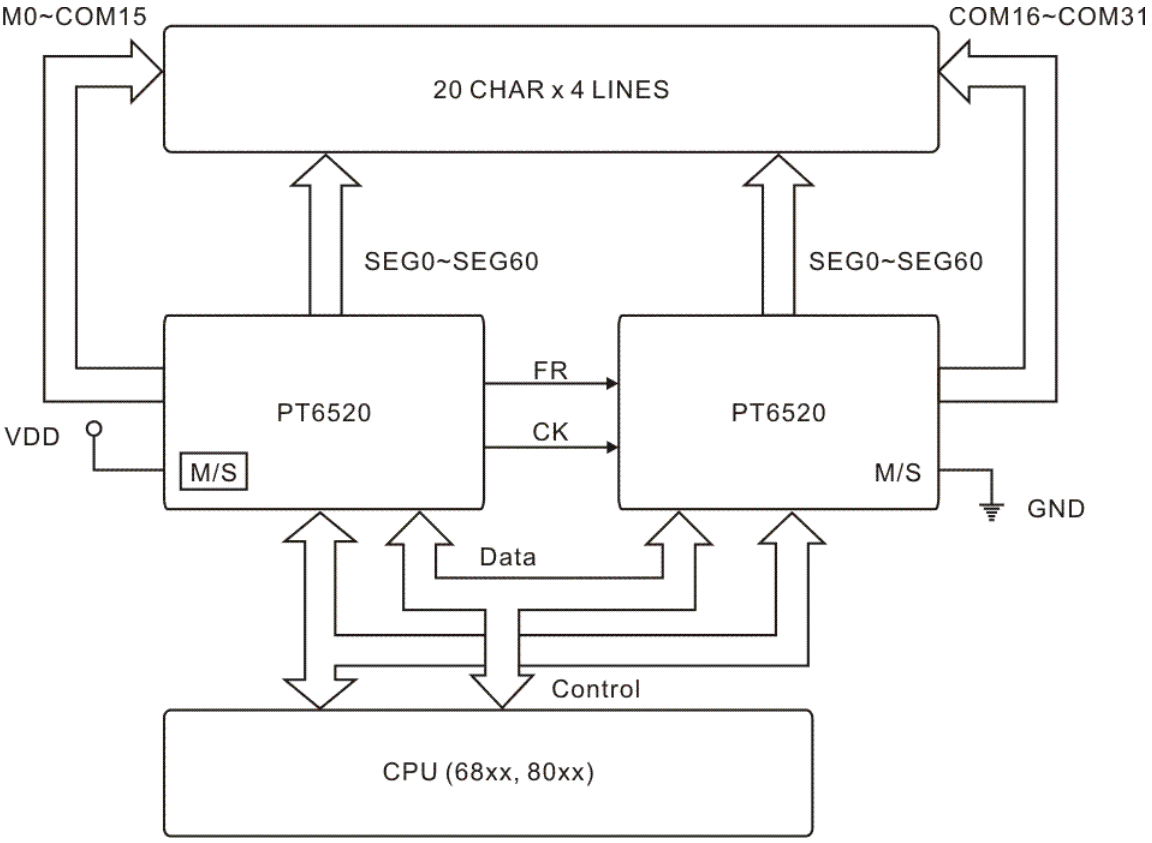
APPLICATIONS

- Peripheral devices
- LCD modules
- Electronic instruments

BLOCK DIAGRAM



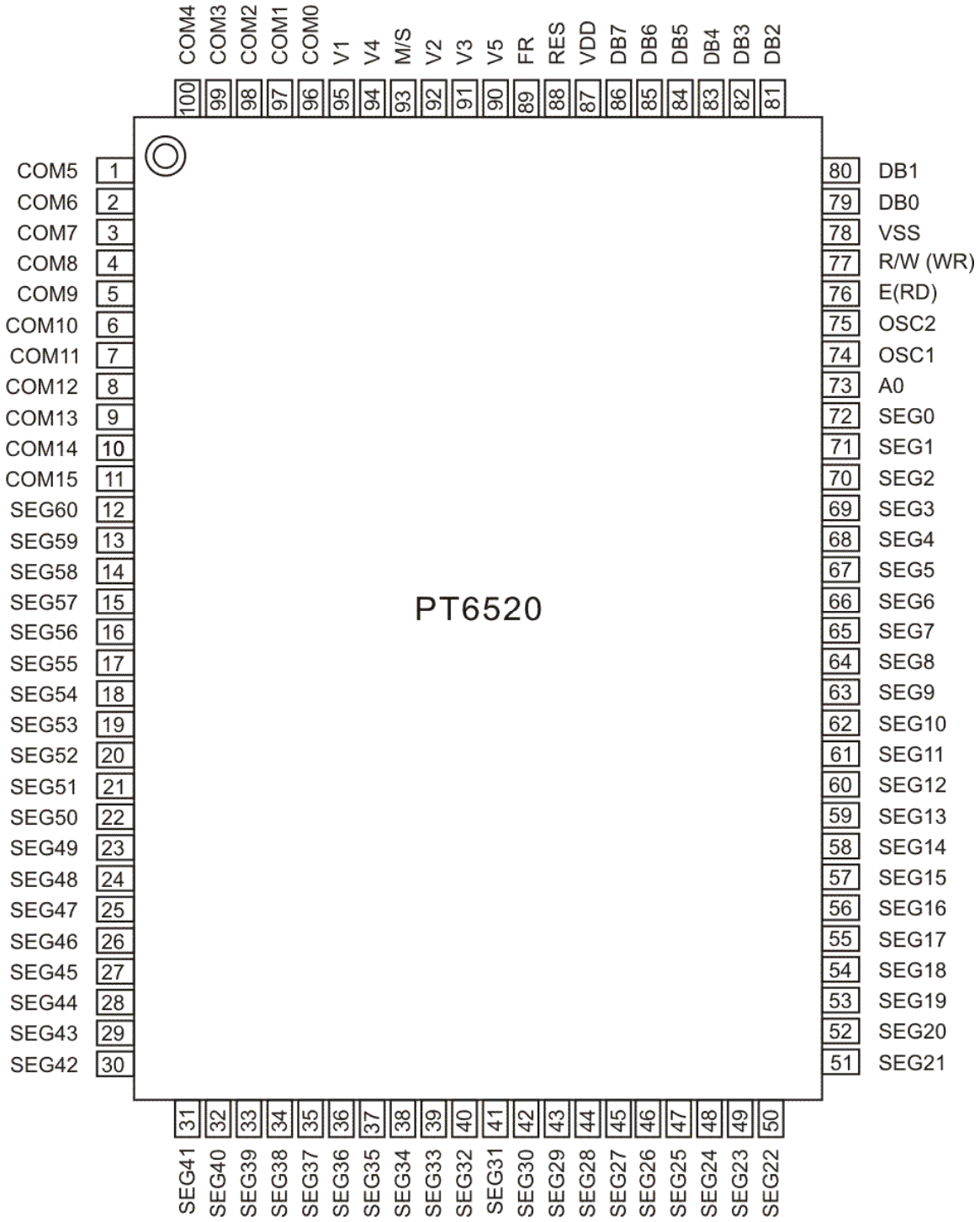
SYSTEM BLOCK DIAGRAM



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6520	100 Pin, QFP	PT6520/PT6520-Q
PT6520-H	C.O.B.	-

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Function
DB0 ~ DB7	Data input
A0	Selection display data or instructions. High: Display data. Low: Instruction.
RES	Reset the system and selects the interface type for a 68 port/80 port MPU. High: 68 port MPU interface. Low: 80 port MPU interface. (edge trigger)
OSC1	Oscillation input pin
E/RD	Read/Write Enable signal when a 68 port MPU is connected. (Active-Low read enable signal when an 80 port MPU is connected)
RW/WR	Read/Write select signal when a 68 port MPU is connected. High: read select. Low: write select. (Active-Low writes enable input when an 80 port MPU is connected. Rising edge sensing)
OSC2	Oscillation output pin
FR	LCD Frame (AC-conversion) signal input/output
SEG0 ~ SEG60	Segment output for driving the LCD
COM0 ~ COM15	Common output for driving the LCD
COM31 ~COM16	Common output for driving the LCD
M/S	Master/Slave select signal
VDD	5V power supply
VSS	0V power supply (GND level)
V1, V2, V3, V4, V5	Power supplies for driving the LCD, VDD>V1>V2>V3>V4>V5

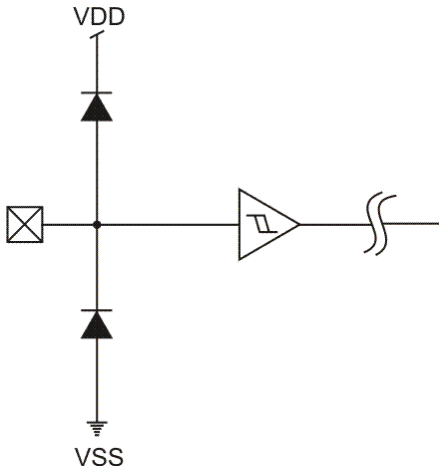
Note: This is an example of PT6520 family pin assignment. The modified pin names are given below.

Product Name	Pin/Pad Number					
	74	75	96 ~ 100, 1~ 11	93	94	95
PT6520	OSC1	OSC2	COM0 ~ COM15	M/S	V4	V1

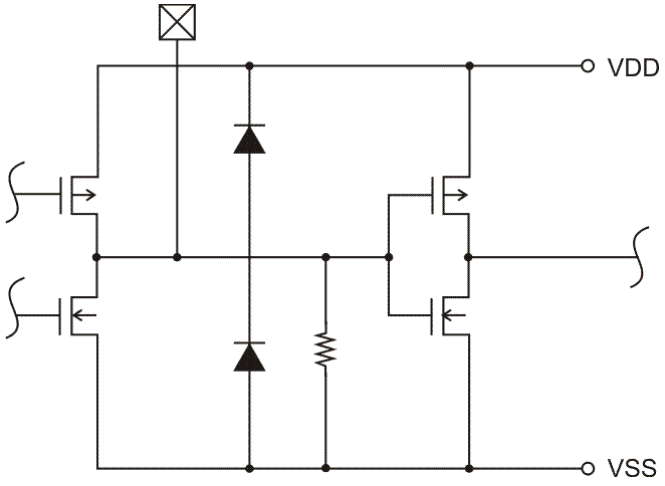
INPUT/OUPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

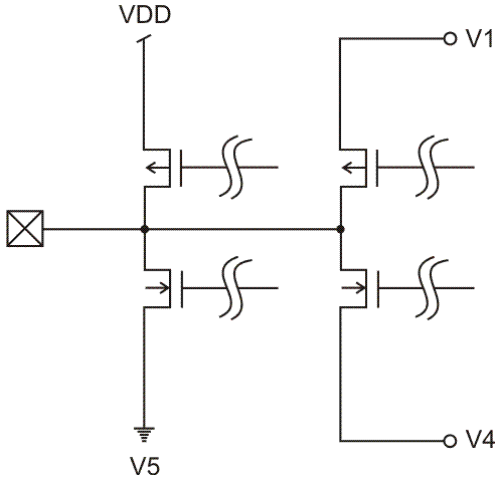
INPUT PIN: A0, E, R/W, DB0~DB7, M/S



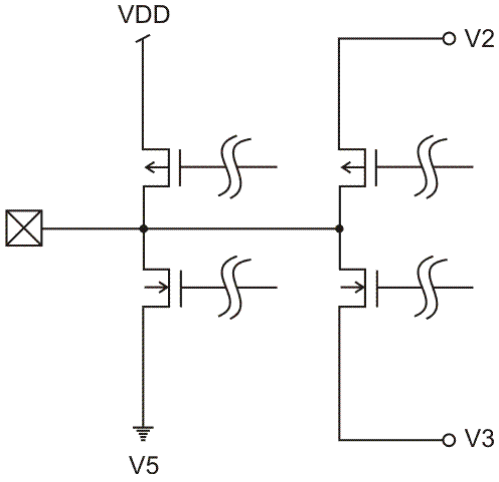
INPUT/OUTPUT PIN: FR



OUTPUT PIN: COM0 TO COM15



OUTPUT PIN: SG0~SG60



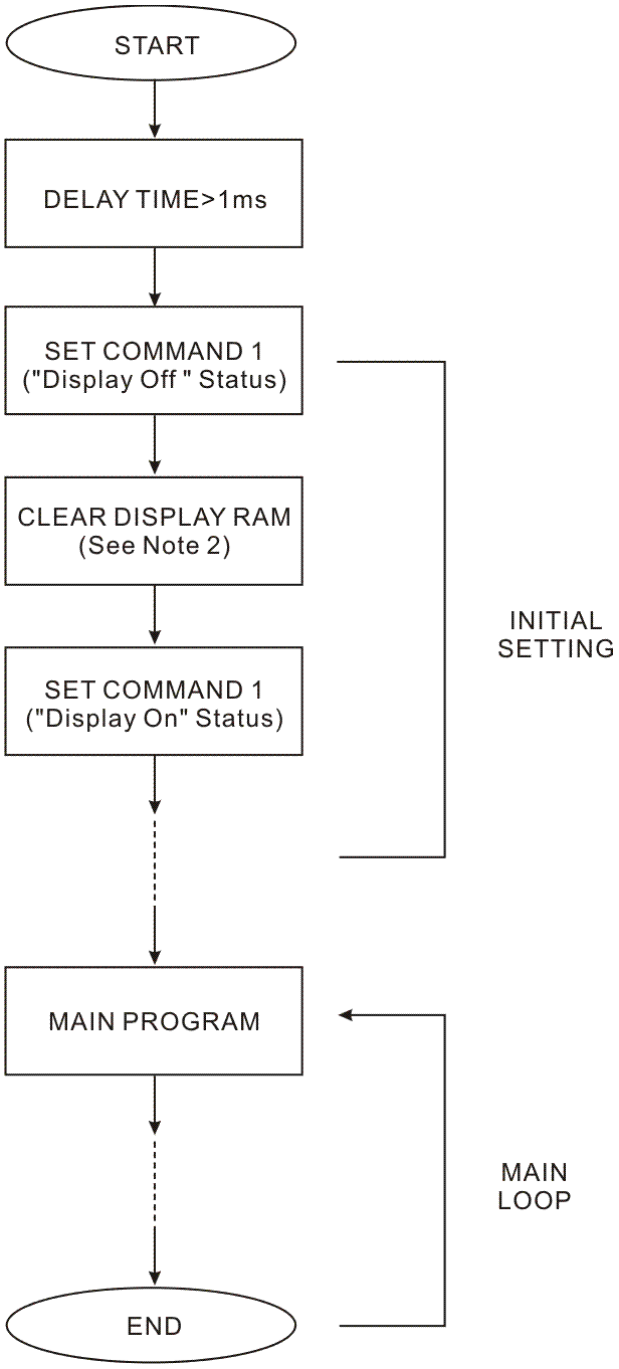
FUNCTION DESCRIPTION

DISPLAY COMMANDS

(Based on the 80 port MPU; the RD and WR commands differ for the 68 port MPU)

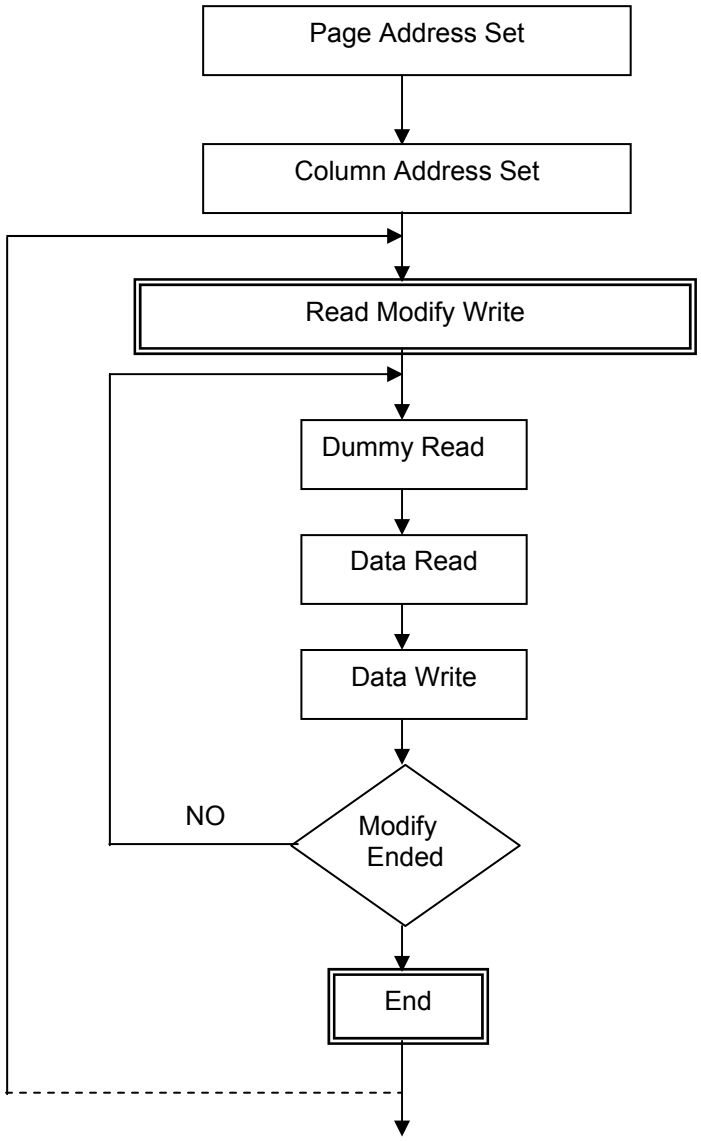
Command		RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	Function
1	Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status. *
2	Display START Line	1	0	0	1	1	0	Display START Address (0-31)					Determines the line of RAM data to be displayed at the display's top line (COM0)
3	Page Address Set	1	0	0	1	0	1	1	1	0	Page (0-3)		Sets the page of the Display RAM in the page address register.
4	Column (segment) Address Set	1	0	0	0	Column address(0-79)							Sets the column address of the Display RAM in the column address register.
5	Status Read	0	1	0	BUSY	ACC	ON/OFF	RESET	0	0	0	0	Read the status. Busy 1: Busy (internal processing) 0: Ready status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting. 0: Normal
6	Write Display Data	1	0	1	Write Data								Writes the data on the data bus to RAM
7	Read Display Data	0	1	1	Read Data								Reads data from the Display RAM onto the data bus.
													These commands access a previously-specified address of the Display RAM, after which the column address is incremented by one.
8	ADC Select	1	0	0	1	0	1	0	0	0	0	0/1	Used to reverse the correspondence between the Display RAM's column address and segment driver output ports 0: Rightward (forward)output 1: Leftward (reverse) output
9	Static Drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (power save)* 0: Normal display operation
10	Duty Select	1	0	0	1	0	1	0	1	0	0	0/1	Selects the duty factor for driving LCD cells. 1: 1/32 duty, 0: 1/16 duty
11	Read Modify Write	1	0	0	1	1	1	0	0	0	0	0	Increments column address counter by 1 when display is written. (This is not done when data is read)
12	End	1	0	0	1	1	1	0	1	1	1	0	Cancels the Ready Modify Write mode.
13	Reset	1	0	0	1	1	1	0	0	0	1	0	Resets the display START line to the 1st line in the register. Resets the column address counter to 0 and page address to 0.

RECOMMENDED SOFTWARE FLOWCHART

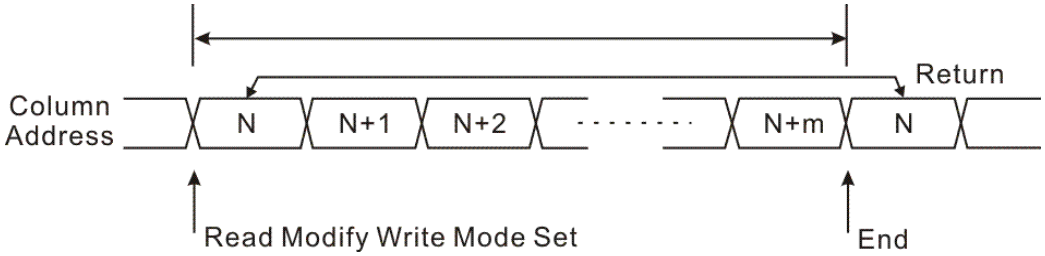


Notes:
1. Command 1: Display On/Off Commands
2. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

CURSOR BLINKING SEQUENCE

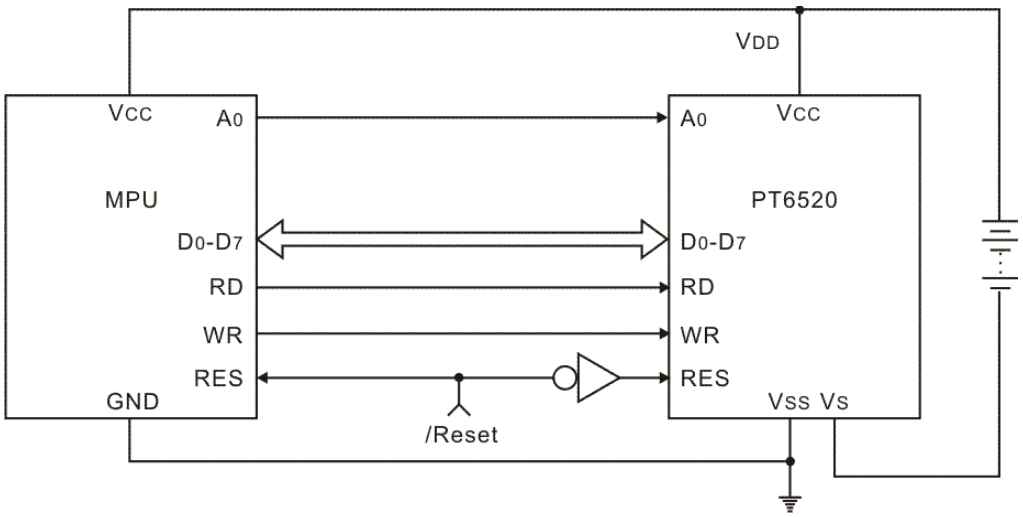


END TIMING

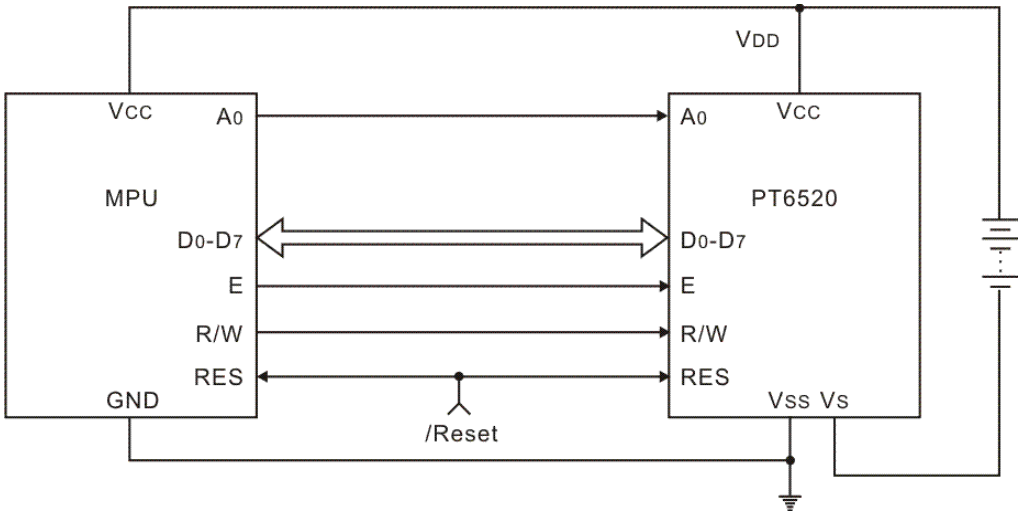


MPU INTERFACE

(1)80-FAMILY MPU

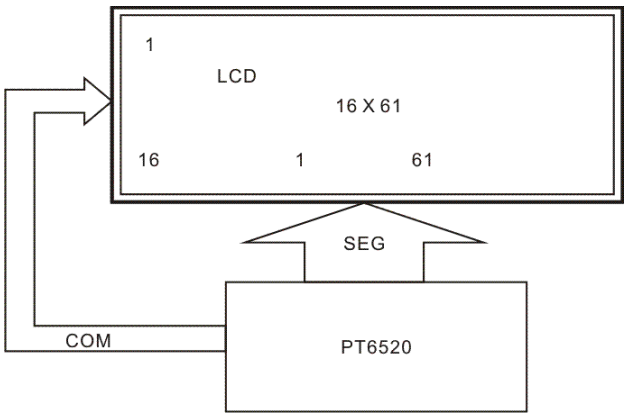


(2)68-FAMILY MPU

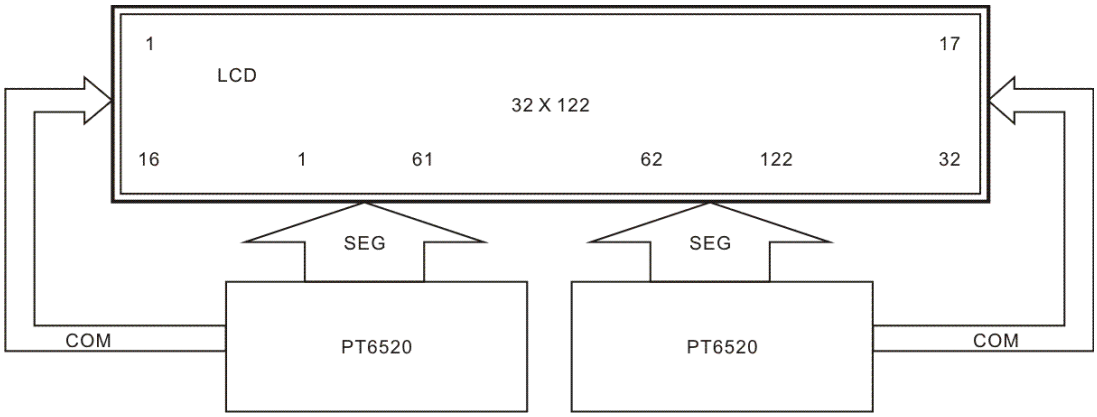


TYPICAL CONNECTIONS WITH LCD PANEL (FULL DOT LCD PANEL: 1 CHARACTER = 6 X 8 DOTS)

(1) DUTY 1/16, 10 CHARACTER X 2 LINES

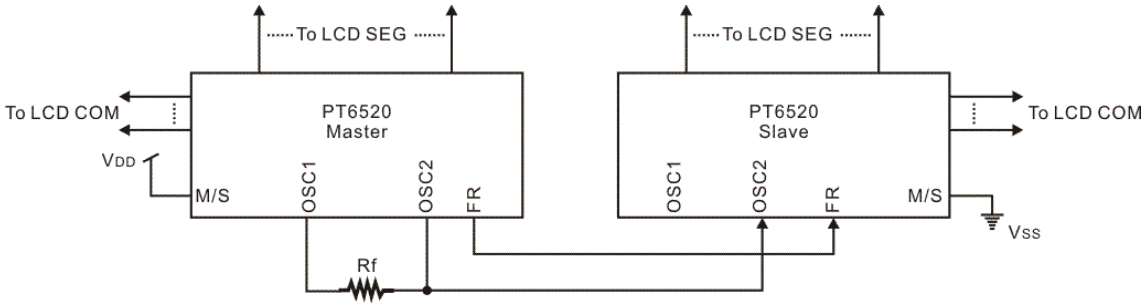


(2) DUTY 1/32, 20 CHARACTERS X 4 LINES



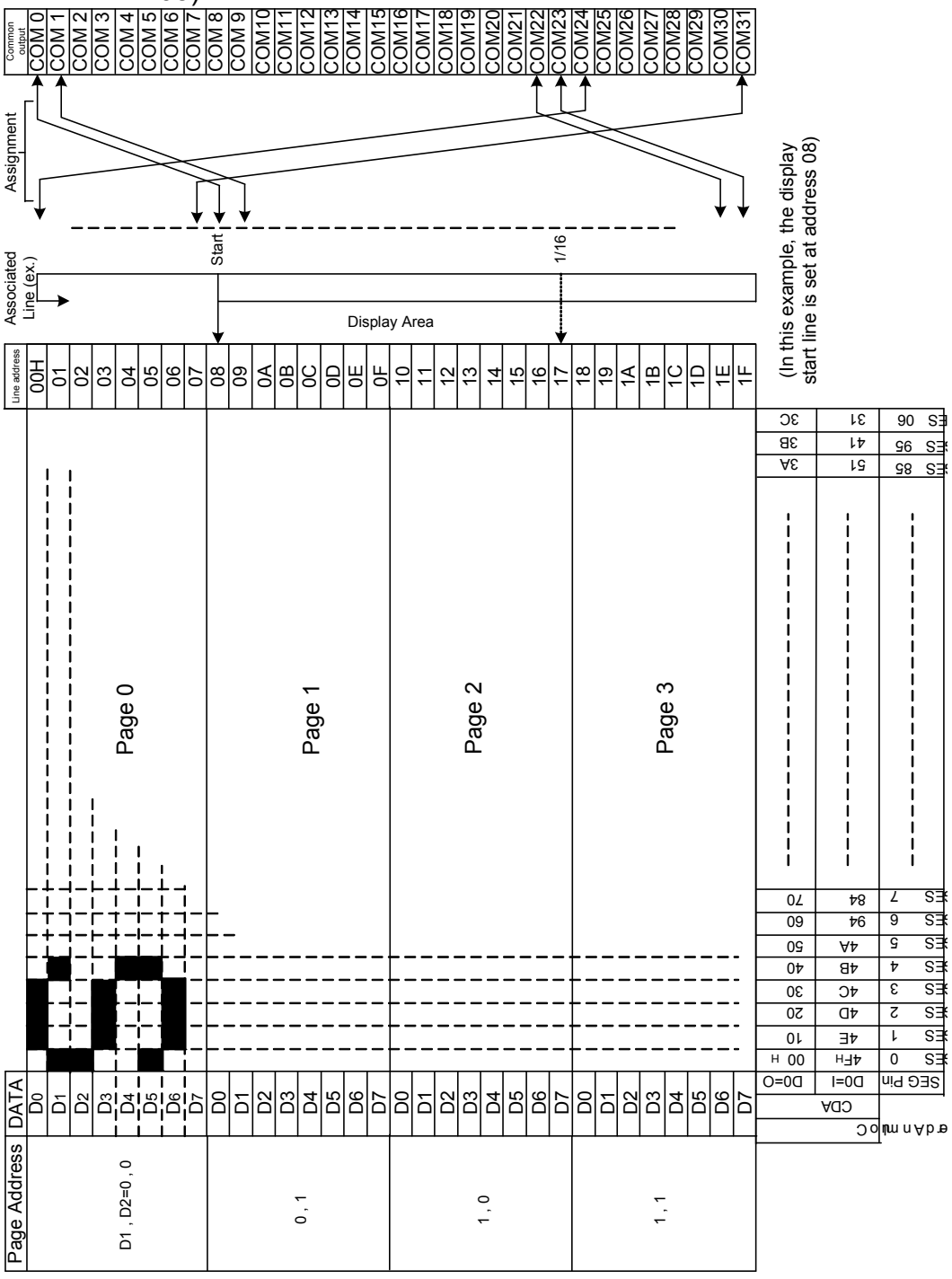
LCD DRIVER INTERCONNECTIONS

PT6520 – PT6520



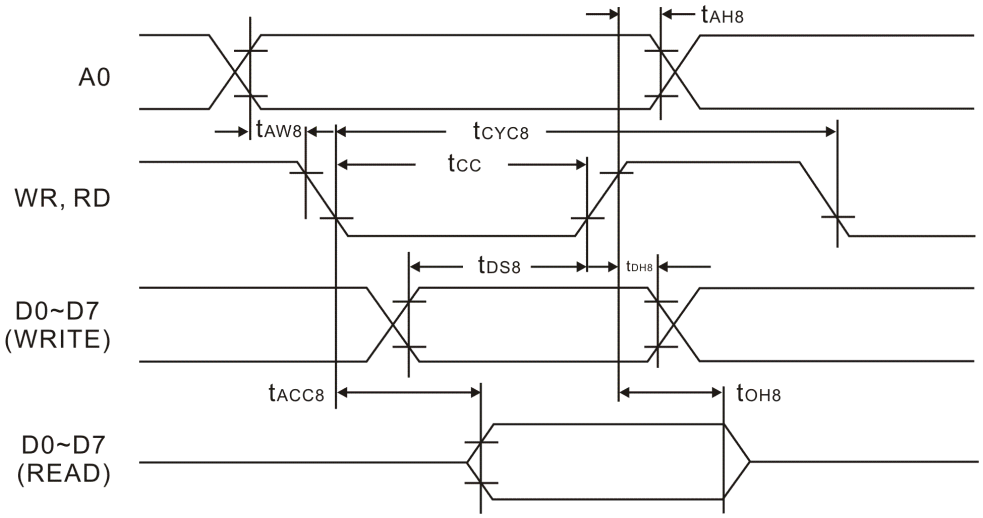
RELATIONSHIP BETWEEN DISPLAY DATA RAM LOCATIONS AND ADDRESSES

(DISPLAY START LINE: 08)

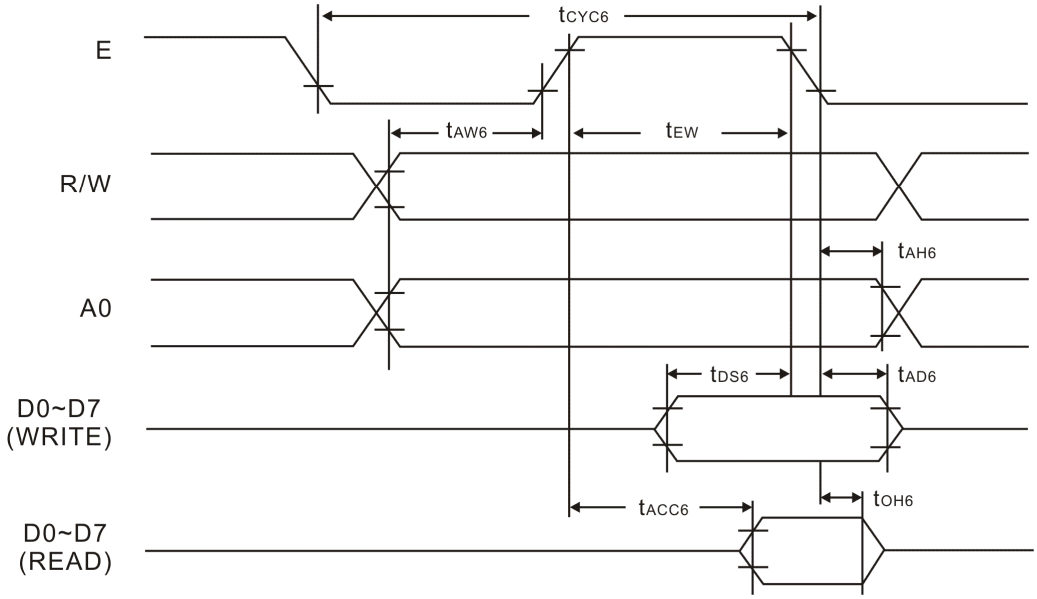


TIMING CHART

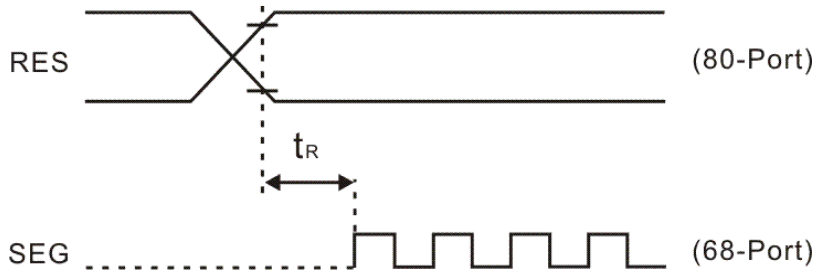
READ/WRITE TIMING FOR THE 80-PORT MPU



READ/WRITE TIMING FOR THE 68-PORT MPU



RESET TIMING FOR 80-PORT/68-PORT DISPLAY



ABSOLUTE MAXIMUM RATING

(Unless otherwise stated, Ta=25℃, VDD=0V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	VSS	-8.0 to 0.3	V
Supply voltage (2)	V5	-16.5 to 0.3	V
Supply voltage (3)	V1, V2, V3, V4	V5 to 0.3	V
Input voltage	VI	VSS –0.3 to 0.3	V
Output voltage	VO	VSS –0.3 to 0.3	V
Power dissipation	PD	250	mW
Operating temperature	Topr	-40 to 85	℃
Storage temperature	Tstg	-65 to 150	℃
Soldering temperature	Tsol	260°C for 10 s (at leads)	-

DC CHARACTERISTICS

(Unless otherwise stated, VDD=0V, VSS=-5/-3V, Ta=25℃)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Pin
Operating voltage (1) **(Note 1)**	Recommended	VSS			-5.5	-5.0	-4.5	V	VSS
	Potential				-7.0	-	-2.4	V	
Operating voltage (2)	Recommended	V5			-13	-	-3.5	V	V5
	Potential				-13	-	-	V	
	Potential	V1, V2			0.6xV5	-	VDD	V	V1, V2
	Potential	V3, V4			V5	-	0.4xV5	V	V3, V4
High input voltage		VIHT	VSS=-5V		VSS+2.0	-	VDD	V	**(Note 2, 3)**
		VIHC	VSS=-5V		0.2xVSS	-	VDD		
		VIHT	VSS=-3V		0.2xVSS	-	VDD		**(Note 2, 3)**
		VIHC	VSS=-3V		0.2xVSS	-	VDD		
Low input voltage		VILT	VSS=-5V		VSS	-	VSS+0.8		**(Note 2, 3)**
		VILC	VSS=-5V		VSS	-	0.8xVSS		
		VILT	VSS=-3V		VSS	-	0.85xVSS		**(Note 2, 3)**
		VILC	VSS=-3V		VSS	-	0.8xVSS		
High output voltage		VOHT	VSS=-5V	IOH=-3.0mA	VSS+2.4	-	-	V	OSC2 **(Note 4, 5)**
		VOHC1		IOH=-2.0mA	VSS+2.4	-	-		
		VOHC2		IOH=-120μA	0.2xVSS	-	-		
		VOHT	VSS=-3V	IOH=-2mA	0.2xVSS			V	OSC2 **(Note 4, 5)**
		VOHC1		IOH=-2mA	0.2xVSS				
		VOHC2		IOH=-50μA	0.2xVSS				
Low output voltage		VOLT	VSS=-5V	IOL=3.0mA	-	-	VSS+0.4	V	OSC2 **(Note 4, 5)**
		VOLT1		IOL=2.0mA	-	-	VSS+0.4		
		VOLT2		IOL=120μA	-	-	0.8xVSS		
		VOLT	VSS=-3V	IOL=2mA			0.8xVSS	V	OSC2 **(Note 4, 5)**
		VOLC1		IOL=2mA			0.8xVSS		
		VOLC2		IOL=50μA			0.8xVSS		
Input leak current		ILI			-1	-	1	μA	**(Note 6)**
Output leak current		ILO			-3	-	3	μA	**(Note 7)**
LCD driver ON resistance		RON	Ta=25°C	V5=-5.0V VSS=-5V	-	5	7.5	KΩ	SEG0~60 COM0~15 **(Note 9)**
				V5=-3.5V VSS=-5V	-	10	50		
Static current consumption		IDDQ	CS=CL=VDD		-	0.05	1	μA	VDD
Dynamic current dissipation		During IDD (1)	During display V5=-5.0V VSS=-5V	fCL=2KHz	-	2.0	5.0	μA	VDD**(Note 10)**
				Rf=1MΩ	-	9.5	15		
			During display V5=-5V VSS =-3V	fCL=2KHz	-	1.5	4.5	μA	
				Rf=1MΩ	-	6.0	12		
		IDD (2)	During access Tcyc=200KHz, VS5=-5V		-	300	500	μA	VDD**(Note 8)**
			VSS=-3V, During access Tcyc=200KHz, VSS=-3V			150	300		
Input terminal capacity		CIN	Ta=25°C, f=1MHz		-	5.0	8	pF	All input terminals

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Pin
Oscillation frequency	Fosc	Rf=1.2MΩ±5%	VSS=-5.0V	12	17	25	KHz	OSC2**(Note 5, 6)**
		Rf=1.2MΩ±5%	VSS=-3.0V	11	16	27		
Hysteresis	VH			0.05VSS	0.1VSS	-	V	**(Note 2, 3, 4, 5)**

Notes:
1. A wide range of operating voltages is guaranteed, except in case of abrupt voltage fluctuations during MPU access.
2. A0, D0~D7, E, R/W pins
3. CL, FR, M/S and RES pins
4. D0~D7
5. FR
6. A0, E (or RD), R/W (or WR), M/S and RES.
7. When D0 to D7 and FR are high impedance.
8. During continual writer access at a frequency of tcyc. Current consumption during access is effectively proportional to the access frequency.
9. For a voltage differential of 0.1V between input (V1,…, V4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
10. PT6520 only. Does not include transient currents due to stray and panel capacitances.

AC CHARACTERISTICS

READ/WRITE TIMING FOR THE 80-PORT MPU

(Ta=25℃, VDD=0V, VSS=-5V)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max	Unit
Address hold time	A0, CS	tAH8	VSS=-5V	10	-	-	ns
			VSS=-3V	20	-	-	ns
Address set-up time		tAW8	VSS=-5V	20	-	-	ns
			VSS=-3V	40	-	-	ns
System cycle time	WR, RD	tCYC8	VSS=-5V	1000	-	-	ns
			VSS=-3V	2000	-	-	ns
Control pulse width		tCC	VSS=-5V	250	-	-	ns
			VSS=-3V	500	-	-	ns
Data set-up time	D0~D7	tDS8	VSS=-5V	100	-	-	ns
			VSS=-3V	200	-	-	ns
Data hold time		tDH8	VSS=-5V	40	-	-	ns
			VSS=-3V	80	-	-	ns
RD access time		tACC8	VSS=-5V	-	-	120	ns
			VSS=-3V	-	-	250	ns
Output disable time		tOH8	CL=100pF	10	-	60	ns
			CL=100pF, VSS=-3V	20	-	120	ns

READ/WRITE TIMING FOR THE 68-PORT MPU

(Ta=25℃, VDD=0V, VSS=-5V)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max	Unit
System cycle time	A0, CS, R/W	tCYC6	VSS=-5V	1000	-	-	ns
			VSS=-3V	2000	-	-	ns
Address set-up time		tAW6	VSS=-5V	20	-	-	ns
			VSS=-3V	40	-	-	ns
Address hold time		tAH6	VSS=-5V	10	-	-	ns
			VSS=-3V	30	-	-	ns
Control pulse width	D0~D7	tDS6	VSS=-5V	80	-	-	ns
			VSS=-3V	160	-	-	ns
Data set-up time		tDH6	VSS=-5V	10	-	-	ns
			VSS=-3V	20	-	-	ns
Data hold time		tOH6	CL=100pF VSS=-5V	10	-	60	ns
			CL=100pF VSS=-3V	20	-	120	ns
RD access time		tACC6	CL=100pF VSS=-5V	-	-	200	ns
			CL=100pF VSS=-3V	-	-	400	ns
Enable disable time	READ	E	tew VSS=-5V	250	-	-	ns
			tew VSS=-3V	400	-	-	ns
	WRITE		tew VSS=-5V	150	-	-	ns
			tew VSS=-3V	250	-	-	ns

Note: tCYC6 indicates the cycle during which CS/E are high; it does not indicate are cycle of the E signal.

CONTROL TIMING FOR 80-PORT/68-PORT MPU

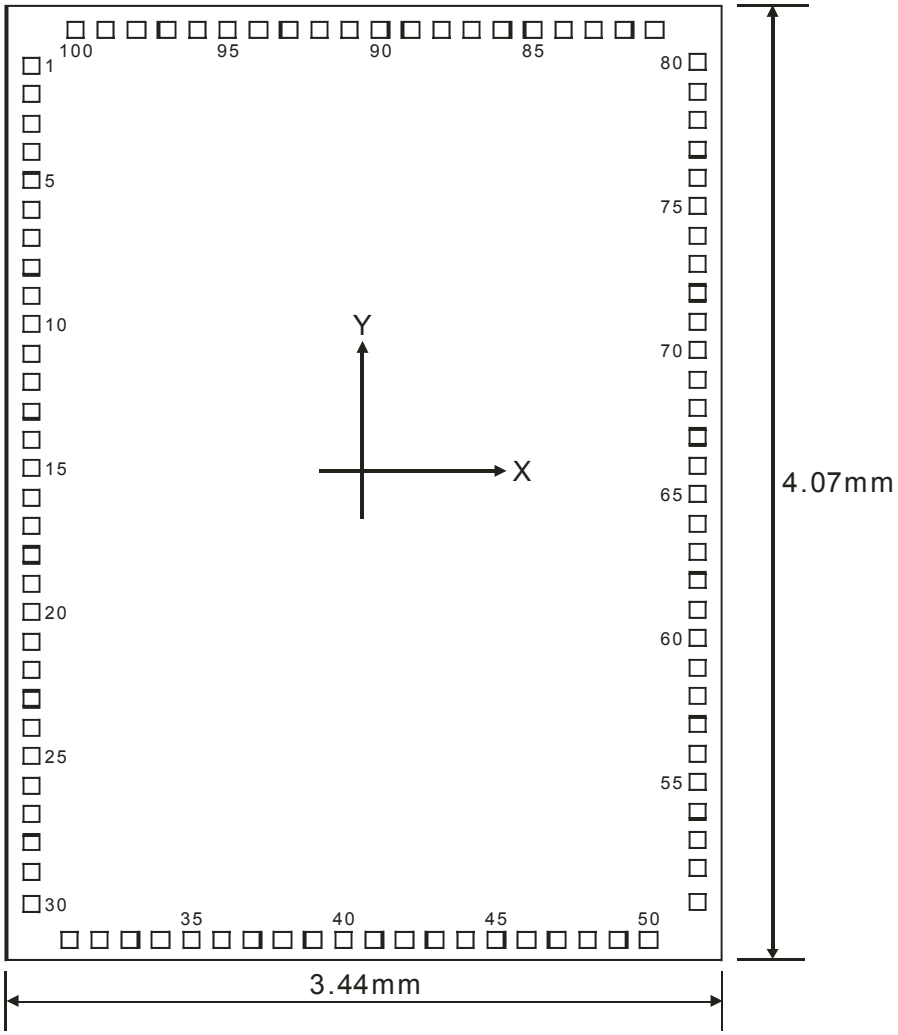
(Ta=25℃, VDD=0V, VSS=-5V)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max	Unit
Reset time	RES	tR	VSS=-5V	1	-	750	µs
			VSS=-3V	1.5	-	1000	µs
Reset time (68-Port)	RES	tR1	VSS=-5V	1	-	-	µs
			VSS=-3V	1.5	-	-	µs
Reset time (80-Port)	RES	tR2	VSS=-5V	1	-	-	µs
			VSS=-3V	1.5	-	-	µs

Notes:
1. The input timing of the FR delay time is determined by the PT6520 (Slave)
2. The output timing of the FR delay time is determined by the PT6520 (Master)

PAD LAYOUT

(PT6520D*A)



Al PAD

Chip Specification	Dimension (mm)
Chip size	3.44 x 4.07
Chip thickness	0.400+0.025
Pad size	0.095 x 0.095

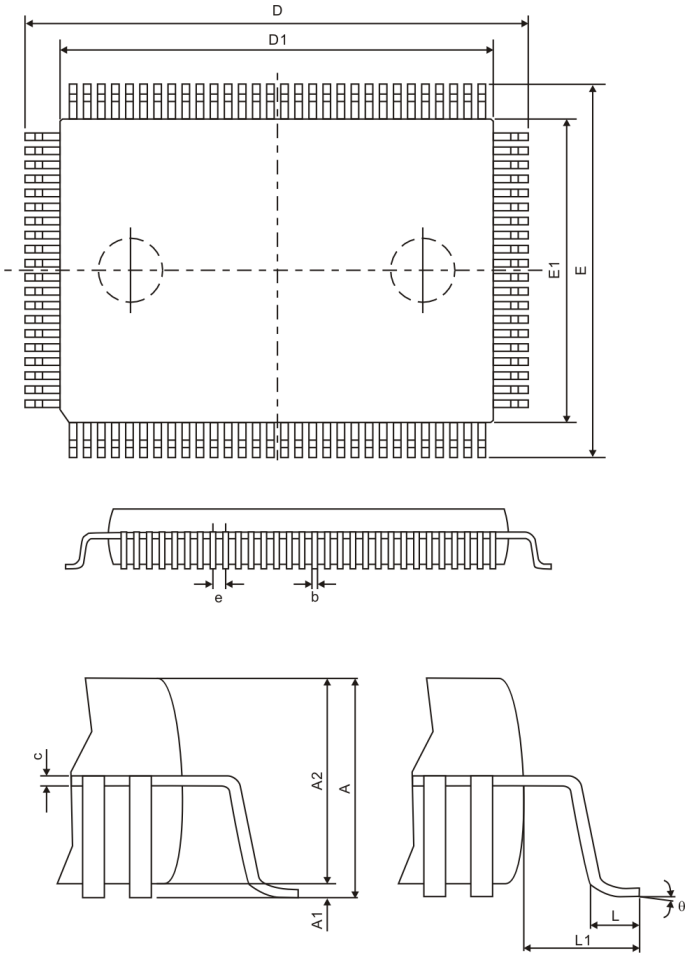
PAD COORDINATES OF PT6520D*A

(Coordinate unit: um)

Pin no.	Name	X	Y	Pin no.	Name	X	Y	Pin no.	Name	X	Y
1	COM5	76.4	3535.2	35	SEG37	875.4	76.4	69	SEG3	3365.4	2270.2
2	COM6	76.4	3420.2	36	SEG36	1025.4	76.4	70	SEG2	3365.4	2385.2
3	COM7	76.4	3305.2	37	SEG35	1175.4	76.4	71	SEG1	3365.4	2500.2
4	COM8	76.4	3190.2	38	SEG34	1325.4	76.4	72	SEG0	3365.4	2615.2
5	COM9	76.4	3075.2	39	SEG33	1475.4	76.4	73	A0	3365.4	2781.9
6	COM10	76.4	2960.2	40	SEG32	1625.4	76.4	74	OSC1	3365.4	2896.9
7	COM11	76.4	2845.2	41	SEG31	1775.4	76.4	75	OSC2	3365.4	3011.9
8	COM12	76.4	2730.2	42	SEG30	1925.4	76.4	76	E(RD#)	3365.4	3126.9
9	COM13	76.4	2615.2	43	SEG29	2075.4	76.4	77	R/W(WR#)	3365.4	3241.9
10	COM14	76.4	2500.2	44	SEG28	2225.4	76.4	78	Vss	3365.4	3356.9
11	COM15	76.4	2385.2	45	SEG27	2375.4	76.4	79	DB0	3365.4	3471.9
12	SEG60	76.4	2270.2	46	SEG26	2525.4	76.4	80	DB1	3365.4	3586.9
13	SEG59	76.4	2155.2	47	SEG25	2675.4	76.4	81	DB2	3013.8	3996.9
14	SEG58	76.4	2040.2	48	SEG24	2825.4	76.4	82	DB3	2833.8	3996.9
15	SEG57	76.4	1925.2	49	SEG23	2975.4	76.4	83	DB4	2653.8	3996.9
16	SEG56	76.4	1810.2	50	SEG22	3125.4	76.4	84	DB5	2473.8	3996.9
17	SEG55	76.4	1695.2	51	SEG21	3365.4	200.2	85	DB6	2293.8	3996.9
18	SEG54	76.4	1580.2	52	SEG20	3365.4	315.2	86	DB7	2113.8	3996.9
19	SEG53	76.4	1465.2	53	SEG19	3365.4	430.2	87	Vdd	1933.8	3996.9
20	SEG52	76.4	1350.2	54	SEG18	3365.4	545.2	88	RES#	1753.8	3996.9
21	SEG51	76.4	1235.2	55	SEG17	3365.4	660.2	89	FR	1573.8	3996.9
22	SEG50	76.4	1120.2	56	SEG16	3365.4	775.2	90	V5	1282.7	3996.9
23	SEG49	76.4	1005.2	57	SEG15	3365.4	890.2	91	V3	1167.7	3996.9
24	SEG48	76.4	890.2	58	SEG14	3365.4	1005.2	92	V2	1052.7	3996.9
25	SEG47	76.4	775.2	59	SEG13	3365.4	1120.2	93	M/S	937.7	3996.9
26	SEG46	76.4	660.2	60	SEG12	3365.4	1235.2	94	V4	822.7	3996.9
27	SEG45	76.4	545.2	61	SEG11	3365.4	1350.2	95	V1	707.7	3996.9
28	SEG44	76.4	430.2	62	SEG10	3365.4	1465.2	96	COM0	592.7	3996.9
29	SEG43	76.4	315.2	63	SEG9	3365.4	1580.2	97	COM1	477.7	3996.9
30	SEG42	76.4	200.2	64	SEG8	3365.4	1695.2	98	COM2	362.7	3996.9
31	SEG41	275.4	76.4	65	SEG7	3365.4	1810.2	99	COM3	247.7	3996.9
32	SEG40	425.4	76.4	66	SEG6	3365.4	1925.2	100	COM4	132.7	3996.9
33	SEG39	575.4	76.4	67	SEG5	3365.4	2040.2				
34	SEG38	725.4	76.4	68	SEG4	3365.4	2155.2				

PACKAGE INFORMATION

100 PINS, QFP



Symbol	Min.	Nom.	Max.
A	-	-	3.40
A1	0.25	-	0.50
A2	2.55	2.70	2.90
b	0.22	0.30	0.33
c	0.11	-	0.23
D	23.20 BSC		
D1	20.00 BSC		
E	17.20 BSC		
E1	14.00 BSC		
e	0.65 BSC		
L1	1.60 REF		
θ	0°	3.5°	7°

Notes:
1. Refer to JEDEC MO-112 GC-1
2. All dimensions are in millimeter.

IMPORTANT NOTICE

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