HARRIS SEMICONDUCTOR

RLD03N06CLE, RLD03N06CLESM, RLP03N06CLE

0.3A, 60V, ESD Rated, Current Limited, Voltage Clamped Logic Level N-Channel Enhancement-Mode Power MOSFETs

July 1996

Features

- **0.30A, 60V**
- **$r_{DS(ON)}$ = 6.0Ω**
- **Built in Current Limit I_{LIMIT} 0.140 to 0.210A at 150°C**
- **Built in Voltage Clamp**
- ***Temperature Compensating* PSPICE Model**
- **2kV ESD Protected**
- **Controlled Switching Limits EMI and RFI**

Description

The RLD03N06CLE, RLD03N06CLESM and RLP03N06CLE are intelligent monolithic power circuits which incorporate a lateral bipolar transistor, resistors, zener diodes and a power MOS transistor. The current limiting of these devices allow it to be used safely in circuits where a shorted load condition may be encountered. The drain-source voltage clamping offers precision control of the circuit voltage when switching inductive loads. The "Logic Level" gate allows this device to be fully biased on with only 5.0V from gate to source, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

The RLD03N06CLE, RLD03N06CLESM and RLP03N06CLE incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

PACKAGING AVAILABILITY

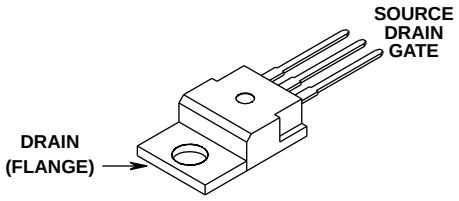
PART NUMBER	PACKAGE	BRAND
RLD03N06CLE	TO-251AA	03N06C
RLD03N06CLESM	TO-252AA	03N06C
RLP03N06CLE	TO-220AB	03N06CLE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. RLD03N06CLESM9A.

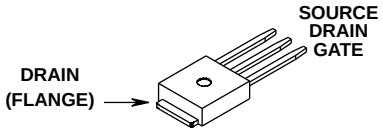
Formerly developmental type TA49026.

Packages

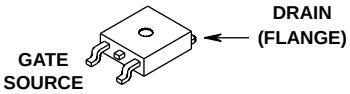
JEDEC TO-220AB



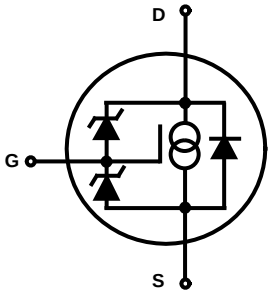
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings T_C = +25°C

		RLD03N06CLE, RLD03N06CLESM, RLP03N06CLE	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage (Note) Reverse Voltage Gate Bias Not Allowed	V_{GS}	+5.5	V
Drain Current RMS Continuous	I_D	Self Limited	
Power Dissipation T_C = +25°C	P_D	30	W
Derate above +25°C	P_T	0.2	W/°C
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	KV
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

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File Number **3948.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	85	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 45V$, $V_{GS} = 0V$	$T_J = +25^oC$	-	-	50	µA
			$T_J = +150^oC$	-	-	200	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 5V$	$T_J = +25^oC$	-	-	5	µA
			$T_J = +150^oC$	-	-	20	µA
On Resistance	$r_{DS(ON)}$	$I_D = 0.100A$, $V_{GS} = 5V$	$T_J = +25^oC$	-	-	6.0	Ω
			$T_J = +150^oC$	-	-	12.0	Ω
Limiting Current	$I_{DS(LIMIT)}$	$V_{DS} = 15V$, $V_{GS} = 5V$	$T_J = +25^oC$	280	-	420	mA
			$T_J = +150^oC$	140	-	210	mA
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 0.10A$, $R_L = 300\Omega$, $V_{GS} = 5V$, $R_{GS} = 25\Omega$		-	-	7.5	µs
Turn-On Delay Time	$t_{D(ON)}$			-	-	2.5	µs
Rise Time	t_R			-	-	5.0	µs
Turn-Off Delay Time	$t_{D(OFF)}$			-	-	7.5	µs
Fall Time	t_F			-	-	5.0	µs
Turn-Off Time	t_{OFF}			-	-	12.5	µs
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	100	-	pF
Output Capacitance	C_{OSS}			-	65	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	3.0	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	5.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220 Package		-	-	80	$^oC/W$
		TO-251 and TO-252 Packages		-	-	100	$^oC/W$

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 0.1A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 0.1A$, $dI_{SD}/dt = 100A/\mu s$	-	-	1.0	ms

Typical Performance Curves

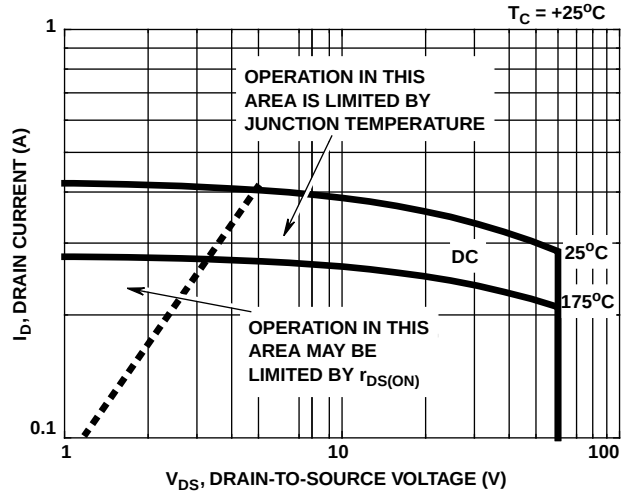


FIGURE 1. SAFE OPERATING AREA CURVE

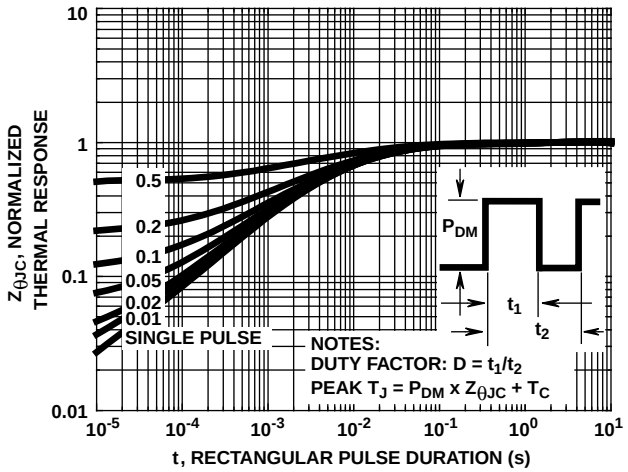


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

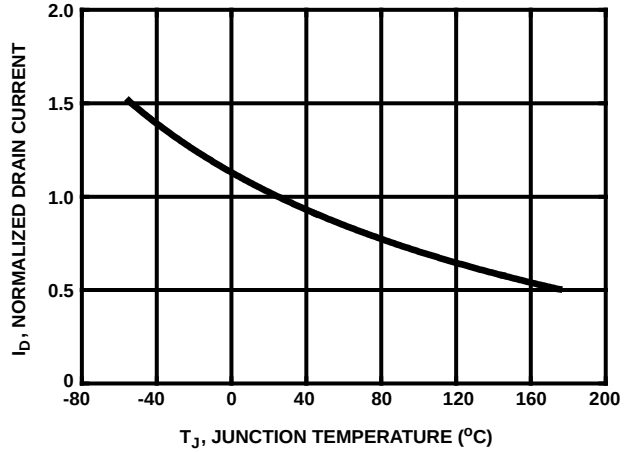


FIGURE 3. TYPICAL NORMALIZED DRAIN CURRENT vs JUNCTION TEMPERATURE

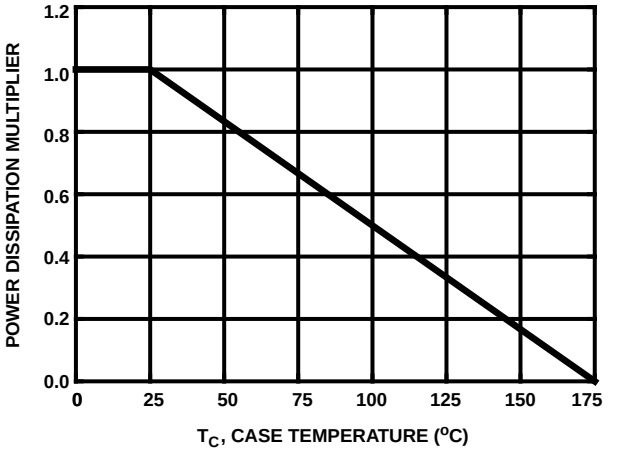


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

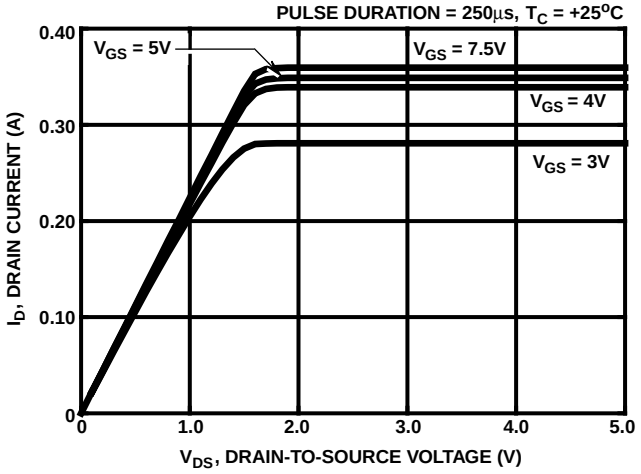


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

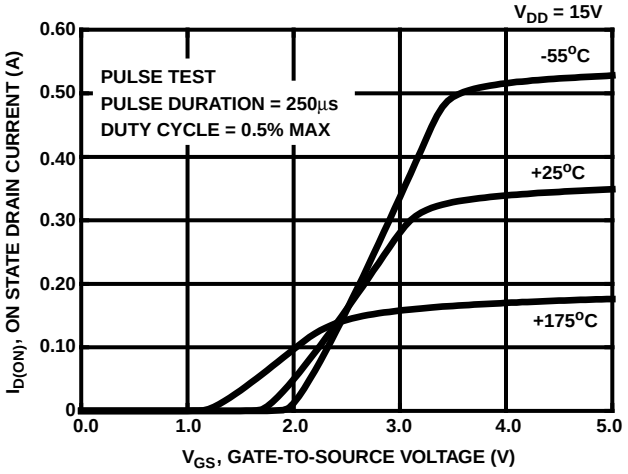


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

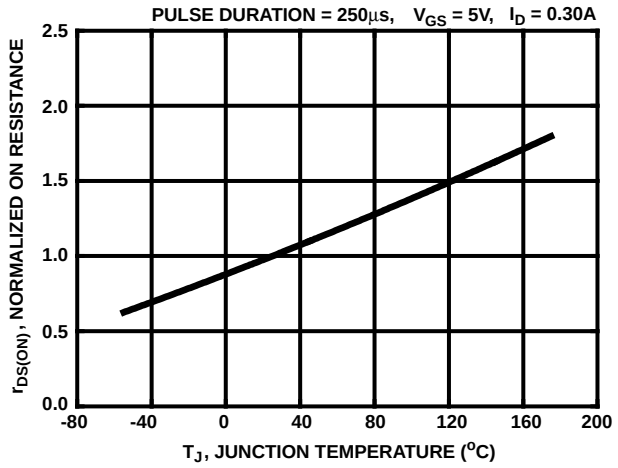


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

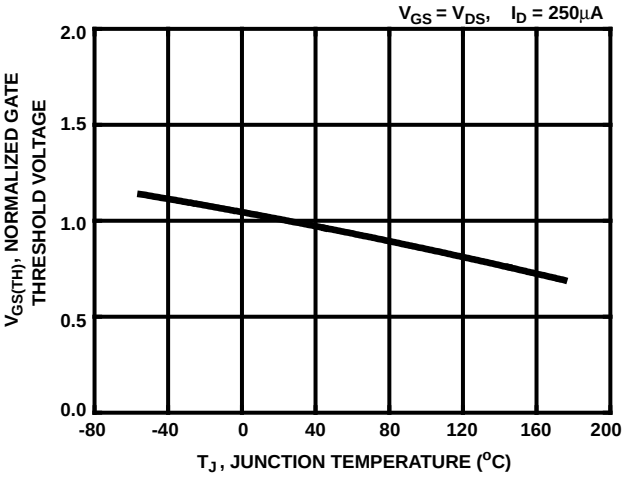


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

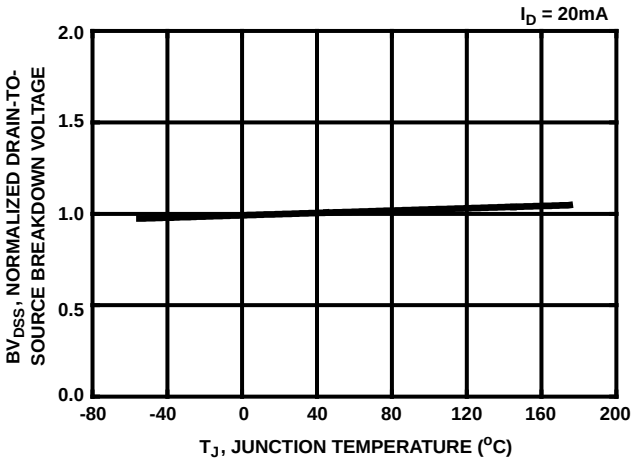


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

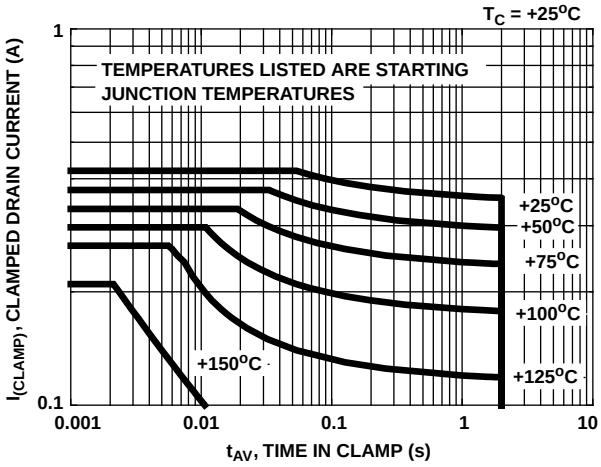


FIGURE 10. SELF-CLAMPED INDUCTIVE SWITCHING

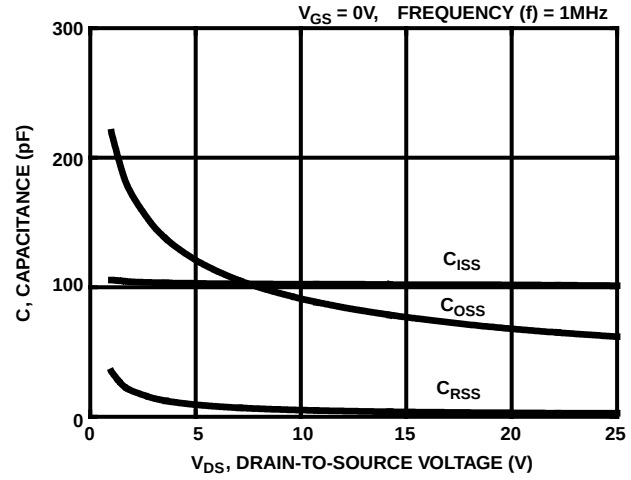


FIGURE 11. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

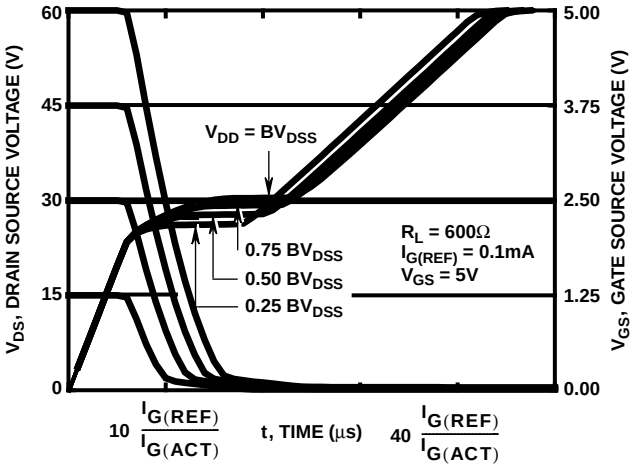


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Test Circuit and Waveform

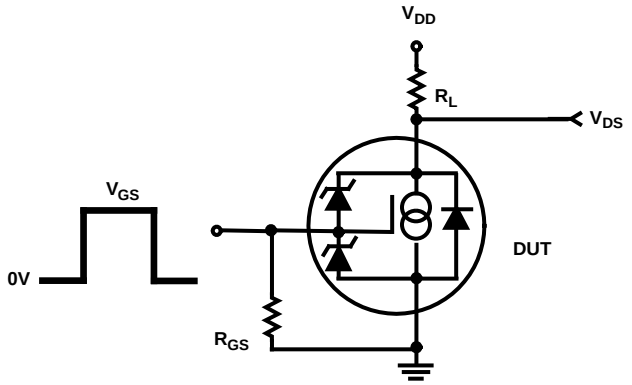


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUIT

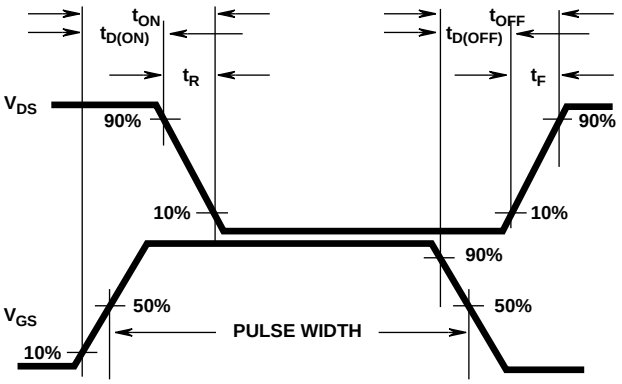


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

Detailed Description

Temperature Dependence of Current Limiting and Switching Speed Performance

The RLD03N06CLE, RLD03N06CLESM and RLP03N06CLE are a monolithic power device which incorporates a Logic Level power MOSFET transistor with a current sensing scheme and control circuitry to enable the device to self limit the drain source current flow. The current sensing scheme supplies current to a resistor that is connected across the base to emitter of a bipolar transistor in the control section. The collector of this bipolar transistor is connected to the gate of the power MOSFET transistor. When the ratiometric current from the current sensing reaches the value required to forward bias the base emitter junction of this bipolar transistor, the bipolar "turns on". A resistor is incorporated in series with the gate of the power MOSFET transistor allowing the bipolar transistor to adjust the drive on the gate of the power MOSFET transistor to a voltage which then maintains a constant current in the power MOSFET transistor. Since both the ratiometric current sensing scheme and the base emitter unction voltage of the bipolar transistor vary with temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 3.

The resistor in series with the gate of the power MOSFET transistor also results in much slower switching performance than in standard power MOSFET transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable.

DC Operation

The limit on the drain to source voltage for operation in current limiting on a steady state (DC) basis is shown in the equation below. The dissipation in the device is simply the applied drain to source voltage multiplied by the limiting current. This device, like most power MOSFET devices today, is limited to 175^{o}C. The maximum voltage allowable can, therefore, be expressed as shown in Equation 1:

$$V_{DS} = \frac{(150°C - T_{AMBIENT})}{I_{LM} \bullet (R_{\theta JC} + R_{\theta JA})} \quad \text{(EQ. 1)}$$

The results of this equation are plotted in Figure 15 for various heatsinks.

Duty Cycle Operation

In many applications either the drain to source voltage or the gate drive is not available 100% of the time. The copper header on which the RLD03N06CLE, RLD03N06CLESM and RLP03N06CLE is mounted has a very large thermal storage capability, so for pulse widths of less then 1ms, the temperature of the header can be considered a constant, thereby the junction temperature can be calculated simply as shown in Equation 2:

$$T_C = (V_{DS} \bullet I_D \bullet D \bullet R_{\theta CA}) + T_{AMBIENT} \quad \text{(EQ. 2)}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to 175^{o}C and using the T_C calculated in Equation 2, the expression for maximum V_{DS} under duty cycle operation is shown in Equation 3:

$$V_{DS} = \frac{150^{o}C - T_C}{I_{LM} \bullet D \bullet R_{\theta JC}} \quad \text{(EQ. 3)}$$

These values are plotted as Figures 16 through 21 for various heatsink thermal resistances.

Limited Time Operations

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 ms, thereby the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures 22 through 25 (RLP03N06CLE) and Figure 26 through 29 (RLD03N06CLE and RLD03N06CLESM) give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 175^{o}C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

Performance Curves

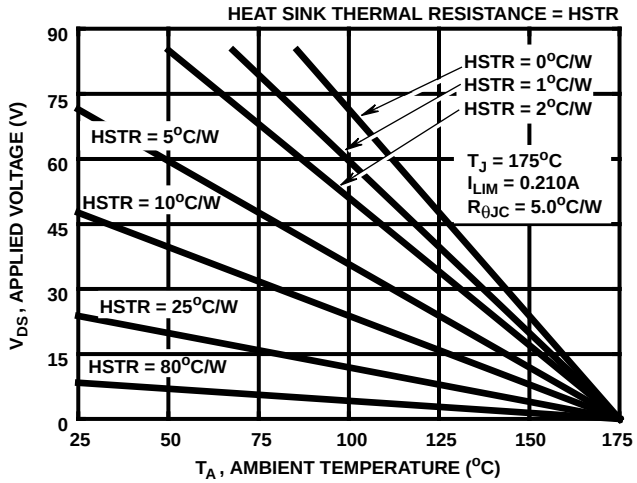


FIGURE 15. DC OPERATION IN CURRENT LIMITING

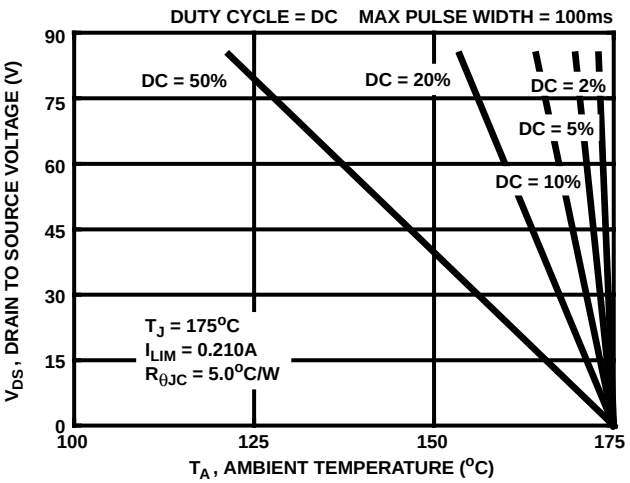


FIGURE 16. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 1°C/W)

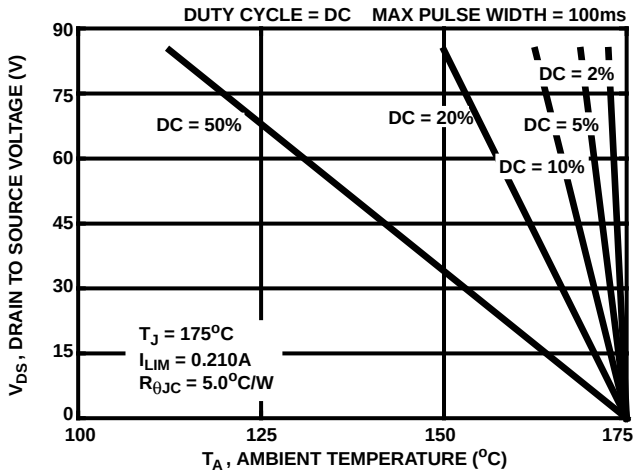


FIGURE 17. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 2°C/W)

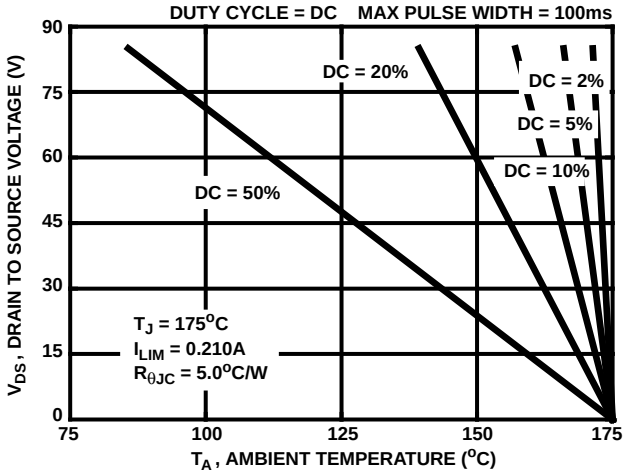


FIGURE 18. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 5°C/W)

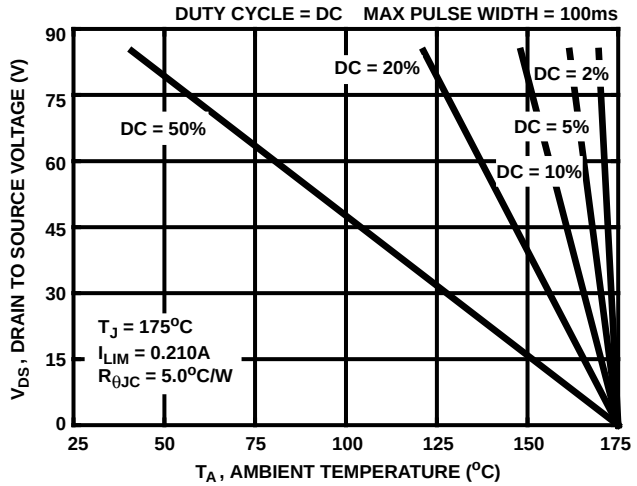


FIGURE 19. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 10°C/W)

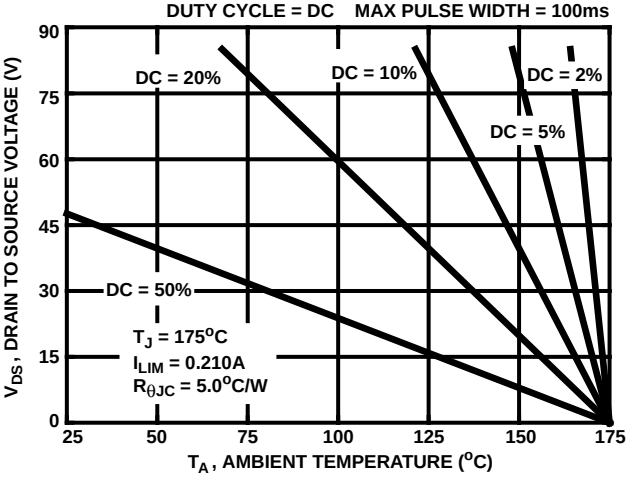


FIGURE 20. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 25°C/W)

Performance Curves (Continued)

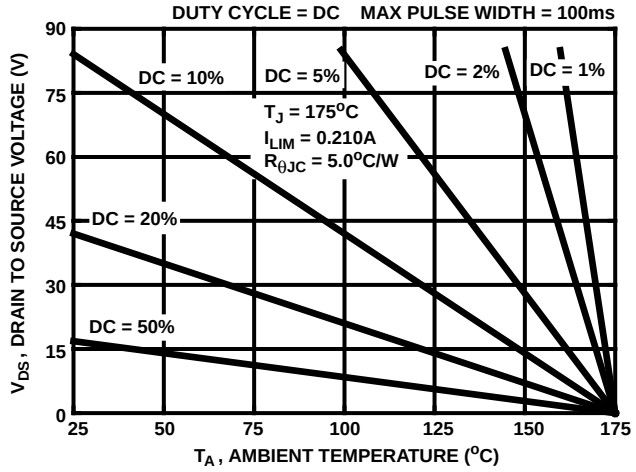


FIGURE 21. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 80°C/W)

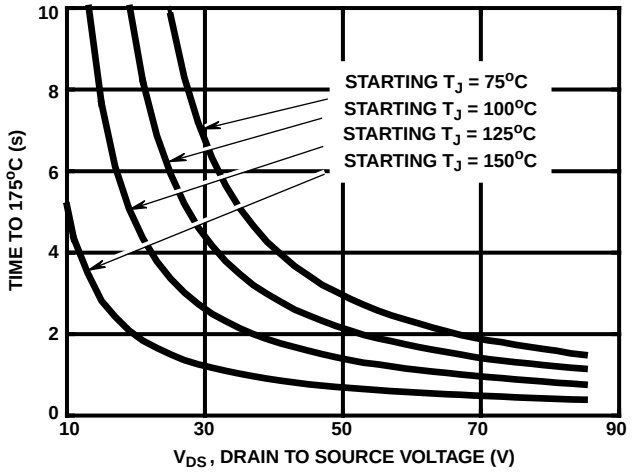


FIGURE 22. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W) (HEATSINK THERMAL CAPACITANCE = 0.5J/°C)

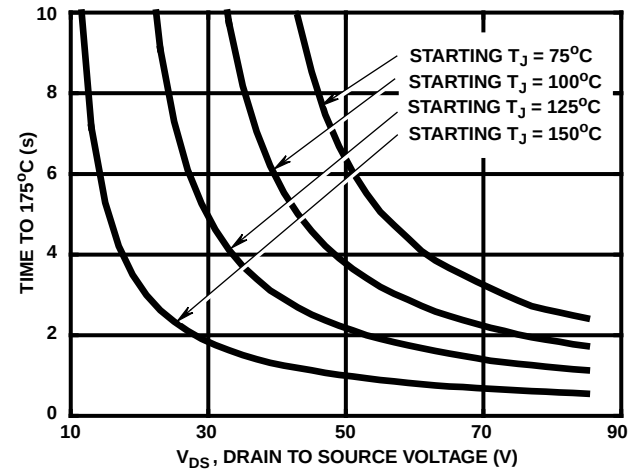


FIGURE 23. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W) (HEATSINK THERMAL CAPACITANCE = 1.0J/°C)

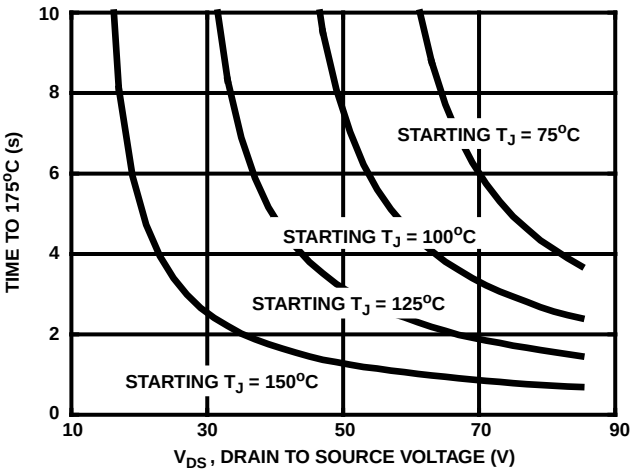


FIGURE 24. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W) (HEATSINK THERMAL CAPACITANCE = 2.0J/°C)

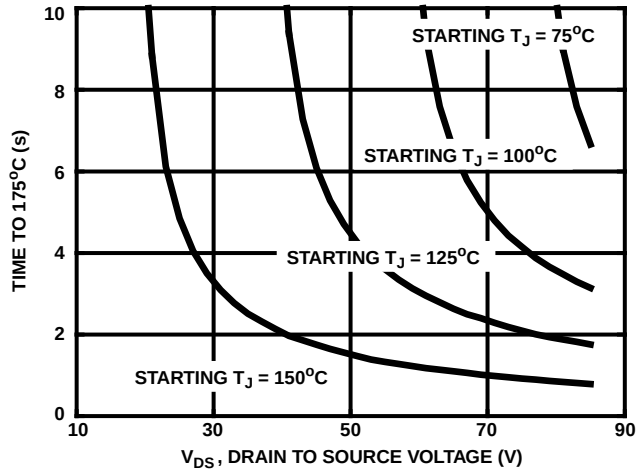


FIGURE 25. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 2°C/W) (HEATSINK THERMAL CAPACITANCE = 4J/°C)

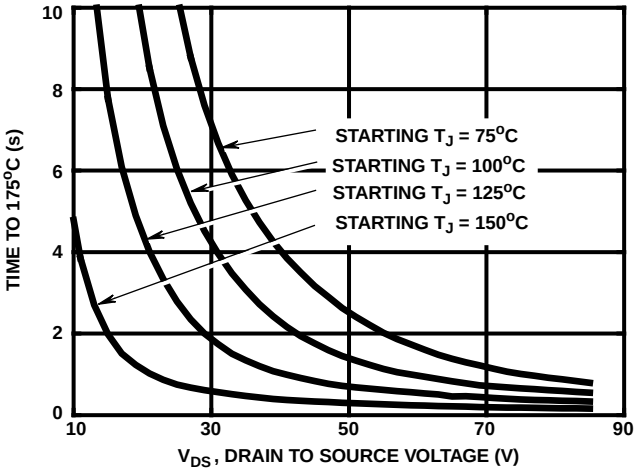


FIGURE 26. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W) (HEATSINK THERMAL CAPACITANCE = 0.5J/°C)

Performance Curves (Continued)

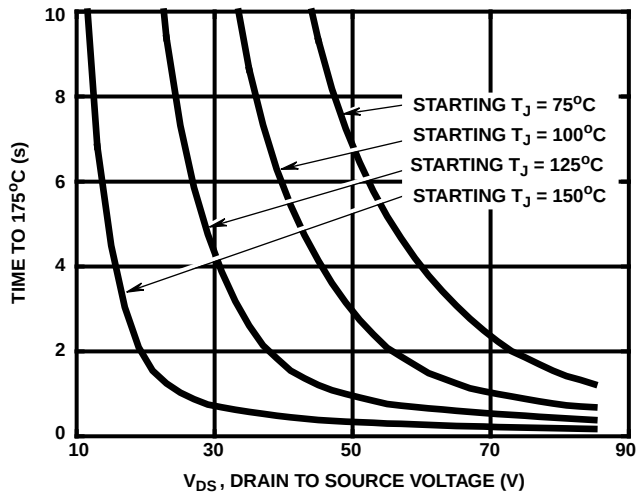


FIGURE 27. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W) (HEATSINK THERMAL CAPACITANCE = 1.0J/°C)

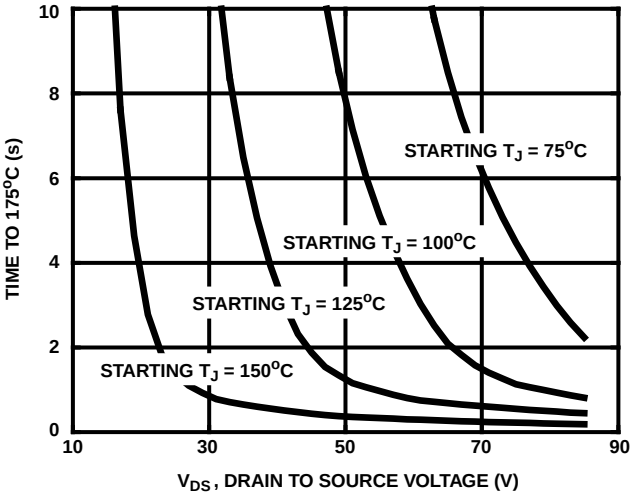


FIGURE 28. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W) (HEATSINK THERMAL CAPACITANCE = 2.0J/°C)

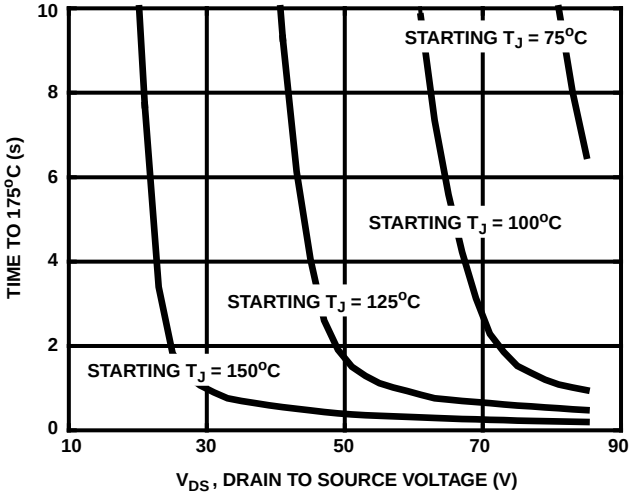


FIGURE 29. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 2°C/W) (HEATSINK THERMAL CAPACITANCE = 4J/°C)

Temperature Compensated PSPICE Model for the RLD03N06CLE, RLD03N06CLESM, RLP03N06CLE

```
SUBCKT RLD03N06CLE 2 1 3;       rev 4/18/94
CA 12 8 0.547e-9
CB 15 14 0.547e-9
CIN 6 8 0.301e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 20 17 18 66.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.96e-9
LSOURCE 3 7 2.96e-9

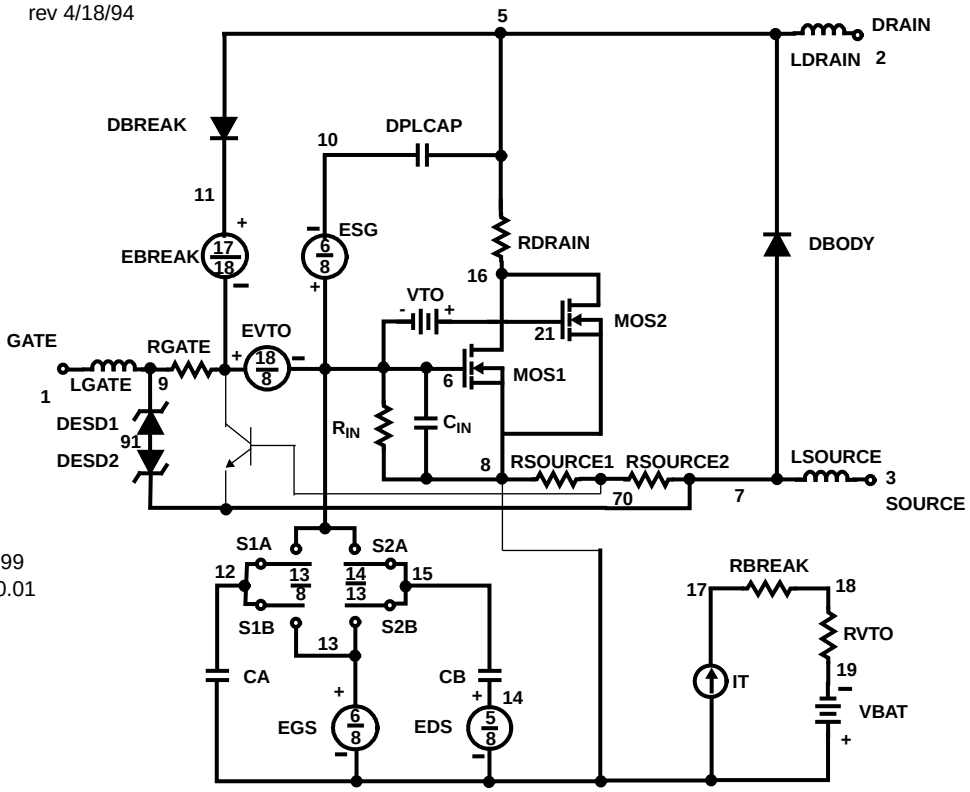
MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

QCONTROL 20 70 7 QMOD 1

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1.123
RGATE 9 20 3200
RIN 6 8 1e9
RSOURCE1 8 70 RDSMOD 1.12
RSOURCE2 70 7 RSMOD 2.16
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.22
```



.MODEL DBDMOD D (IS = 7.97e-17 RS = 1.82 TRS1 = 3.91e-3 TRS2 = 1.24e-5 CJO = 3.00e-10 TT = 1.83e-7)
.MODEL DBKMOD D (RS = 3150 TRS1 =0 TRS2 = 0)
.MODEL DESD1MOD D (BV = 13.54 TBV1 = 0 TBV2 = 0 RS = 45.5 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 11.46 TBV1 = -7.576e-4 TBV2 = -3.0e-6 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 74.2e-12 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.67 KP = 3.40 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL QMOD NPN (BF =5)
.MODEL RBKMOD RES (TC1 = 4e-4 TC2 = 1.13e-8)
.MODEL RDSMOD RES (TC1 = 6.80e-3 TC2 = 6.5e-6)
.MODEL RSMOD RES (TC1 = 2.95e-3 TC2 = -1e-6)
.MODEL RVTOMOD RES (TC1 = -2.22e-3 TC2 = -1.95e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3 VOFF = -1)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1 VOFF = -3)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.85 VOFF = 2.15)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.15 VOFF = -2.85)

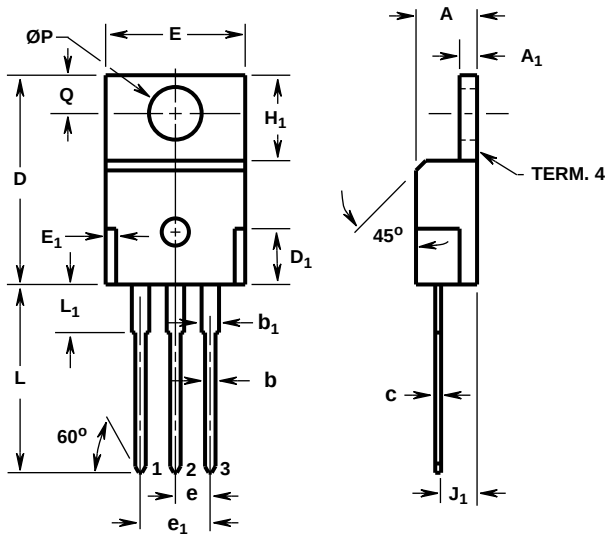
.ENDS

NOTE:

1. For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records 1991.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



LEAD NO. 1 - GATE
LEAD NO. 2 - DRAIN
LEAD NO. 3 - SOURCE
TERM. 4 - DRAIN

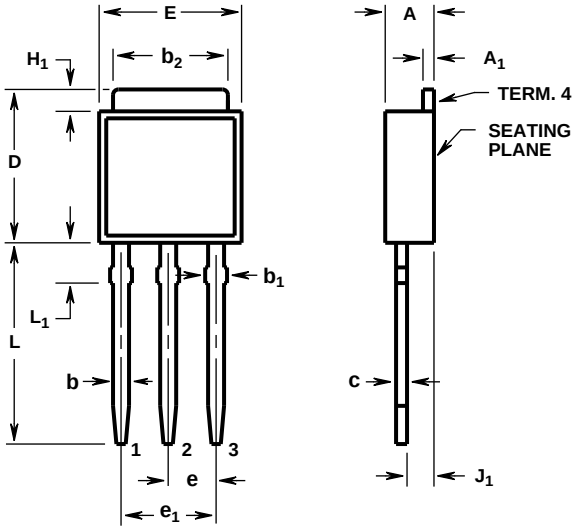
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

TO-251AA

3 LEAD JEDEC TO-251AA PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

LEAD NO. 1 - GATE

LEAD NO. 2 - DRAIN

LEAD NO. 3 - SOURCE

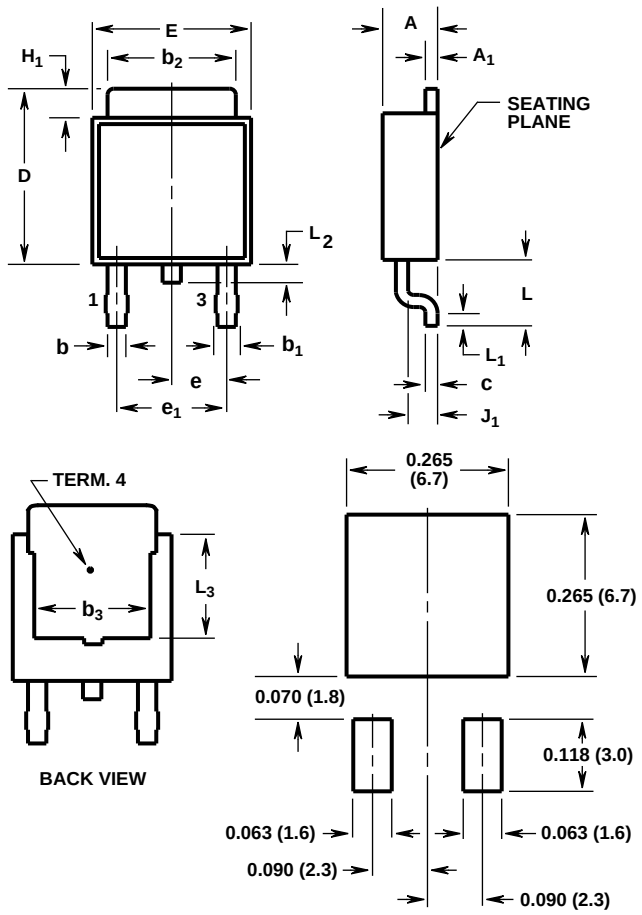
TERM. 4 - DRAIN

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

LEAD NO. 1 - GATE

LEAD NO. 3 - SOURCE

TERM. 4 - DRAIN

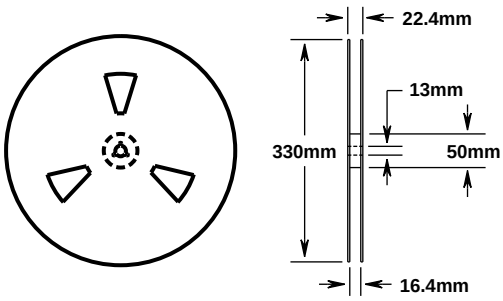
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.020	-	0.51	-	4, 6
L_2	0.025	0.040	0.64	1.01	3
L_3	0.170	-	4.32	-	2

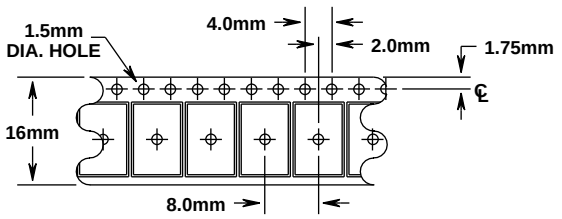
NOTES:

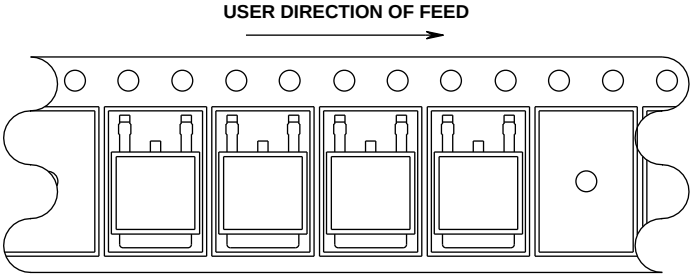
1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_3 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 5 dated 10-95.

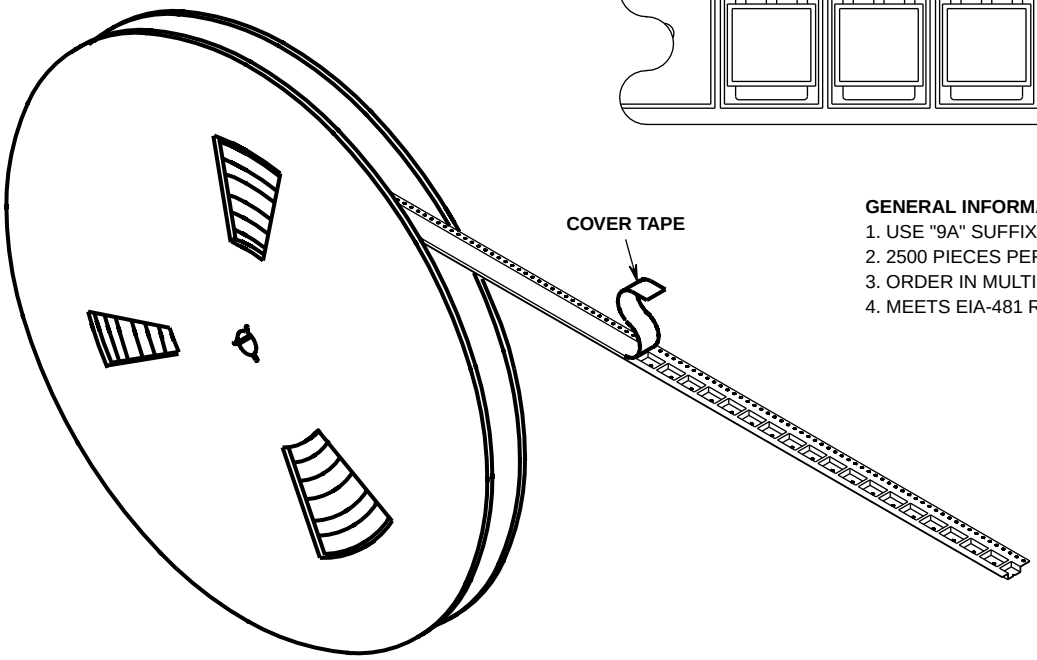
TO-252AA

16mm TAPE AND REEL









GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 5 dated 10-95

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