2.8W Stereo Class-D Audio Power Amplifier and Class AB Headphone Driver (DC Volume Control, UVP, AGC Function)

Features

- Operating Voltage: 3.3V-5.5V
- High Efficiency 85% at P_O=2.8W, 4Ω Speaker, V_{DD}=5V
- Filter-Free Class-D Amplifier
- Low Shutdown Current
  - I_{DD}=1μA at V_{DD}=5V
- 64 Steps Volume Adjustable from -80dB to +20dB by DC Voltage with Hysteresis
- AGC (Non-Clip) Function
  - Disable : 0.45VDD~VDD, Floating
  - Max, Power : GND
- UVP Function
  - Disable : Floating
- Output Power at THD+N=1%
  BTL Mode
  - 2.25W at V_{DD}=5V, R_L=4Ω
  - 1.3W at V_{DD}=5V, R_L=8Ω
  SE Mode
  - 68mW at V_{DD}=5V, R_L=32Ω
  Output Power at THD+N=10%
  - 2.8W at V_{DD}=5V, R_L=4Ω
  - 1.6W at V_{DD}=5V, R_L=8Ω
- Less External Components Required
- Two Output Modes Allowable with BTL and SE Modes Selected by SE/BTL Pin
- Input Signal and Headphone Output Signal in Phase
- Thermal and Over-Current Protections with Auto-Recovery
- Power Enhanced Packages SOP-24(300mil), Dip-24(300mil)
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- LCD TVs
- DVD Player
- Active Speakers

General Description

The APA2603A is a stereo, high efficiency, filter-free Class-D audio amplifier available in a SOP-24 package.

The APA2603A provide the precise DC volume control, the gain range is from +20dB (V_{VOLUME}=0V) to -80dB (V_{VOLUME}=5V) with 64 steps precise control. It's easy to get the suitable amplifier's gain with the 64 steps gain setting.

The filter-free architecture eliminates the output filters compared to the traditional Class-D audio amplifier, and reduces the external component counts and the components high, it could save the PCB space, system cost, simplifies the design and the power loss at filter.

APA2603A provides an AGC (Non-Clip) function, and this function can low down the dynamic range for large input signal. APA2603A can provide from 20dB to -80dB with 64 steps gain decrease for non-clipping function, and this function can avoid output signal clipping.

The APA2603A also integrates the de-pop circuitry that reduces the pops and click noises during power on/off or shutdown enable process.

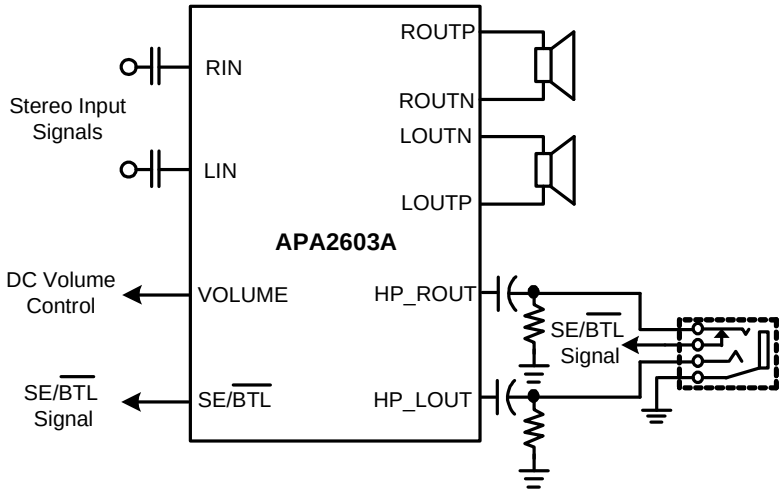
The APA2603A has build-in over-current and thermal protection that prevent the chip being destroyed by short circuit or over temperature situation.

APA2603A combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/BTL input control pin signal.

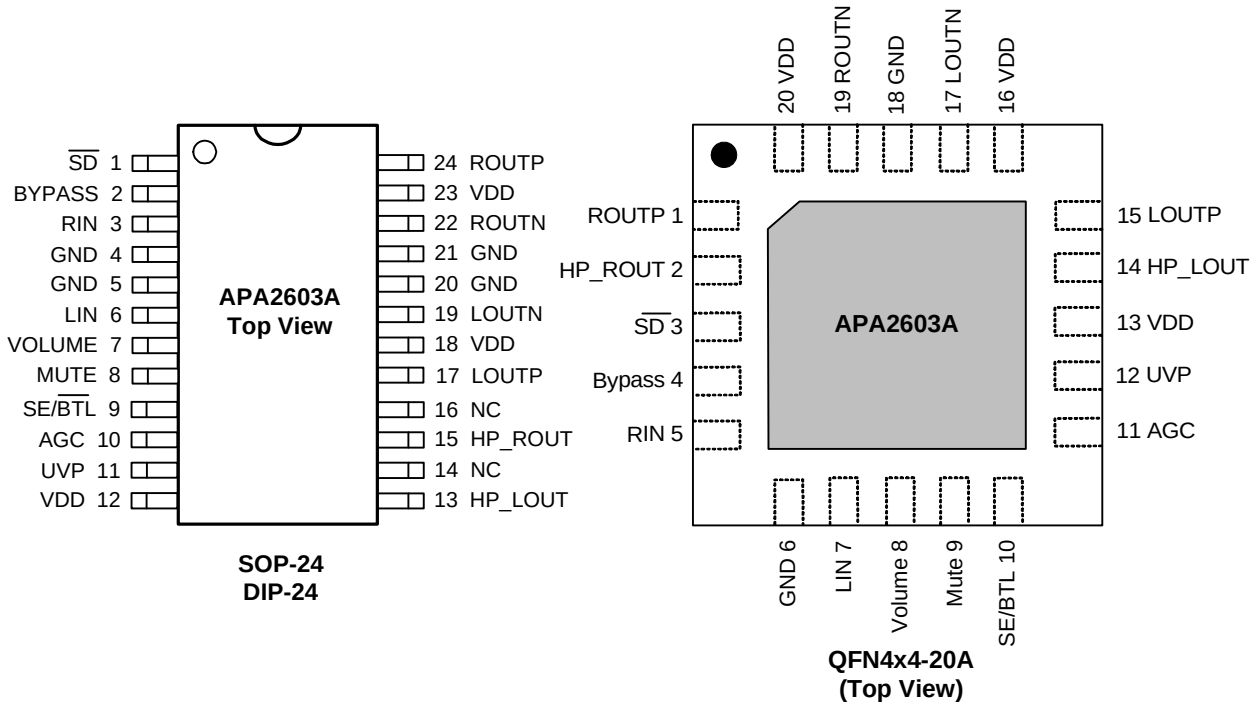
APA2603A is capable of driving 2.8W at 5V into 4Ω speaker. The efficiency can archived 85% at R_L=4Ω when P_O=2.8W at V_{DD}=5V.

APA2603A is capable of driving 60mW at 5V into 32Ω Headphone

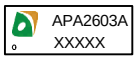
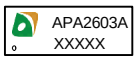
Simplified Application Circuit



Pin Configuration



Ordering and Marking Information

APA2603A □□□-□□□ Lead Free Code Handling Code Temperature Range Package Code	Package Code K : SOP-24 J : DIP-24 QA : QFN4x4-20A Operating Ambient Temperature Range I : -40 to 85°C Handling Code TU : Tube TR : Tape & Reel Lead Free Code G : Halogen and Lead Free Device
APA2603A K : 	XXXXX - Date Code
APA2603A J : 	XXXXX - Date Code
APA2603A QA : 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (VDD, PVDD to GND)	-0.3 to 6	V
	Input Voltage (LIN, RIN to GND)	-0.3 to V_{DD}+0.3	
	Input Voltage ($\overline{SD}$, MUTE, AGC, UVP, VOLUME and SE/$\overline{BTL}$, BYPASS to GND)	-0.3 to V_{DD}+0.3	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	
T_{SDR}	Maximum Soldering Temperature Range, 10 Seconds	260	
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under"recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) SOP-24 DIP-24 QFN4x4-20A	 96 50 45	°C/W
θ_{JC}	Thermal Resistance -Junction to Case (Note 3) SOP-24 DIP-24 QFN4x4-20A	 18 50 7	°C/W

Note 2: Please refer to " Layout Recommendation", the GND PIN on the central of the IC should connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Note 3: The case temperature is measured at the center of the GND PIN on the underside of the SOP-24 package.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		3.3 ~ 5.5	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$, MUTE	2 ~ V_{DD}	
		SE/ $\overline{BTL}$	0.8 V_{DD} ~ V_{DD}	
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$, MUTE	0~0.8	
		SE/$\overline{BTL}$	0~1.0	
V_{ICM}	Common Mode Input Voltage		1 ~ V_{DD}-1	V
T_A	Ambient Temperature Range		-40 ~ 85	°C
T_J	Junction Temperature Range		-40 ~ 125	
R_L	Speaker Resistance		3.5 ~	Ω

Electrical Characteristics

V_{DD}=5V, V_{GND}=0V, T_A= 25°C, Gain=20dB (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA2603A			Unit
				Min.	Typ.	Max.	
I_{DD}	Supply Current (BTL)	V_{MUTE}=0V, $V_{/SD}$=5V, No Load		-	6.5	15	mA
I_{DD}	Supply Current (SE)	V_{MUTE}=0V, $V_{/SD}$=5V, No Load		-	2.5	5	mA
I_{MUTE}	Supply Current (BTL)(MUTE)	V_{MUTE}=5V, $V_{/SD}$=5V, No Load		-	**6.5**	15	mA
I_{MUTE}	Supply Current (SE)(MUTE)	V_{MUTE}=5V, $V_{/SD}$=5V, No Load		-	**2.5**	5	mA
I_{SD}	Supply Current	V_{MUTE}=0V, $V_{/SD}$=0V, No Load		-	-	1	μA
I_i	Input Current	$\overline{SD}$, MUTE, VOLUME		-	-	1	
F_{OSC}	Oscillator Frequency			400	500	600	kHz
R_i	Input Resistance (BTL)	Gain=20dB		31	36	42	kΩ
R_i	Input Resistance (SE)	Gain=3.5dB		51	59	68	kΩ
R_{DSON}	Static Drain-Source On-State Resistance	V_{DD}=5.5V, I_L=0.8A	P-channel Power MOSFET	-	270	-	mΩ
			N-channel Power MOSFET	-	260	-	
		V_{DD}=4.5V, I_L=0.6A	P-channel Power MOSFET	-	285	-	
			N-channel Power MOSFET	-	270	-	
		V_{DD}=3.6V, I_L=0.4A	P-channel Power MOSFET	-	300	-	
			N-channel Power MOSFET	-	280	-	
$T_{START-UP}$	Start-Up Time from Shutdown	Bypass Capacitor, C_B=2.2μF.		-	1.2	2	s

Electrical Characteristics (Cont.)

V_{DD}=5V, V_{GND}=0V, T_A= 25°C, Gain=20dB (unless otherwise noted)

Operating Characteristics, BTL Mode

Symbol	Parameter	Test Conditions		APA2603A			Unit
				Min.	Typ.	Max.	
V_{DD}=5V, T_A=25°C, GAIN=6dB							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=4Ω	2.1	2.2	-	W
			R_L=8Ω	1.0	1.3	-	
		THD+N=10% f_{in}=1kHz	R_L=4Ω	-	2.8	-	
			R_L=8Ω	-	1.7	-	
η	Efficiency	R_L=4Ω, P_O=2.8W		80	85	-	%
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=4Ω, P_O=1.6W	-	0.1	0.3	
			R_L=8Ω, P_O=0.8W	-	0.08	0.2	
Crosstalk	Channel Separation	P_O=0.2W, R_L=4Ω, f_{in}=1kHz		-	-100	-60	dB
PSRR	Power Supply Rejection Ratio	R_L=4Ω, Input AC-Ground	f_{in}=100Hz	-	-60	-50	
			f_{in}=1kHz	-	-70	-60	
SNR (Note 5)	Signal to Noise Ratio	With A-weighting Filter V_O=1V_{rms}, R_L=8Ω		-	-82.5	-	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{rms}		-	-90	-80	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{rms}		-	-120	-90	
V_n	Output Noise	With A-weighting Filter (Gain=20dB)		-	75	100	μVrms
V_{OS}	Output Offset Voltage	R_L=4Ω (Gain=20dB)		-	5	30	mV
V_{DD}=3.6V, T_A=25°C, GAIN=6dB							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=4Ω	1.0	1.3	-	W
			R_L=8Ω	0.6	0.65	-	
		THD+N=10% f_{in}=1kHz	R_L=4Ω	-	1.7	-	
			R_L=8Ω	-	0.85	-	
η	Efficiency	R_L=4Ω, P_O=1.4W		78	83	-	%
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=4Ω, P_O=0.8W	-	0.2	0.4	
			R_L=8Ω, P_O=0.5W	-	0.1	0.3	
Crosstalk	Channel Separation	P_O=0.1W, R_L=4Ω, f_{in}=1kHz		-	-100	-60	dB
PSRR	Power Supply Rejection Ratio	R_L=4Ω, Input AC-Ground	f_{in}=100Hz	-	-60	-50	
			f_{in}=1kHz	-	-70	-60	
SNR	Signal to Noise Ratio	With A-weighting Filter V_O=1V_{rms}, R_L=8Ω		-	-82.5	-	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{rms}		-	-85	-70	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1V_{rms}		-	-110	-90	
V_n	Output Noise	With A-weighting Filter (Gain=20dB)		-	75	100	μVrms
V_{OS}	Output Offset Voltage	R_L=4Ω, (Gain=20dB)		-	5	30	mV

Electrical Characteristics (Cont.)

V_{DD}=5V, V_{GND}=0V, T_A= 25°C, Gain=20dB (unless otherwise noted)

Operating Characteristics, SE mode

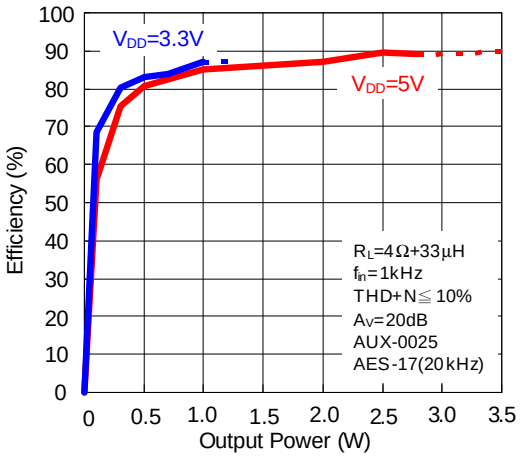
Symbol	Parameter	Test Conditions		APA2603A			Unit
				Min.	Typ.	Max.	
V_{DD}=5V, T_A=25°C, GAIN=3.5dB							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=32Ω	50	60	-	mW
		THD+N=10% f_{in}=1kHz	R_L=32Ω	-	75	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=32Ω P_O=42.5mW	-	0.02	-	%
Crosstalk	Channel separation	P_O=6mW, R_L=32Ω, f_{in}=1kHz		-	-100	-80	dB
PSRR	Power Supply Rejection Ratio	R_L=32Ω, Input AC-Ground	f_{in}=100Hz	-	-60	-50	
			f_{in}=1kHz	-	-75	-60	
SNR	Signal to Noise Ratio	With A-weighting Filter V_O=1V_{rms}, R_L=32Ω.		-	-94	-	
V_n	Output Noise	With A-weighting Filter (Gain=3.5dB)		-	20	40	μVrms
V_{OS}	Output Offset Voltage	R_L=32Ω, (Gain=3.5dB)		-	5	12	mV

Pin Description

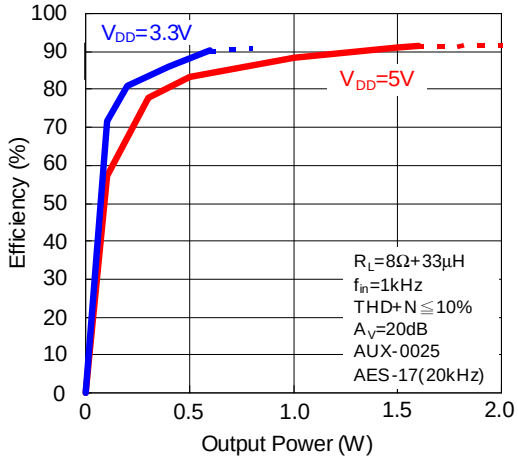
PIN		NAME	FUNCTION
NO.			
SOP-24	QFN-20		
1	3	$\overline{SD}$	Shutdown mode control input. Pulling low the voltage on this pin shuts off the IC.
2	4	BYPASS	Bias voltage for power amplifiers.
3	5	RIN	Input of right channel power amplifier.
4,5	6	AGND	Analog signal ground.
6	7	LIN	Input of left channel power amplifier.
7	8	VOLUME	Internal gain setting input. Connect to GND to set max gain=20dB
8	9	MUTE	Mute control signal input, hold low for normal operation, hold high to mute.
9	10	SE/$\overline{BTL}$	Output mode control input, high for SE output mode and low for BTL mode.
14,16	-	NC	No connection.
10	11	AGC	VDD~0.45VDD or AGC Floating, disable this function.
11	12	UVP	Under voltage protection input. Floating or pull “H” disable this function.
12,18,23	13,16,20	VDD	Power
13	14	HP_LOUT	Headphone output of left channel power amplifier.
15	2	HP_ROUT	Headphone output of right channel power amplifier.
17	15	LOUTP	Positive output of left channel power amplifier.
19	17	LOUTN	Negative output of left channel power amplifier.
20,21	18	PGND	Power ground for the H-bridges.
22	19	ROUTN	Negative output of right channel power amplifier.
24	1	ROUTP	Positive output of right channel power amplifier.

Typical Operating Characteristics

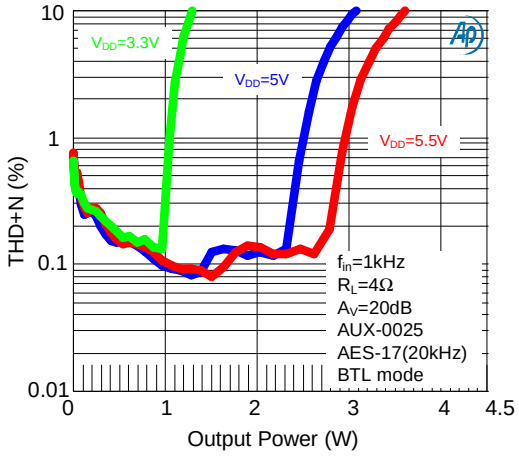
Efficiency vs. Output Power (4W)



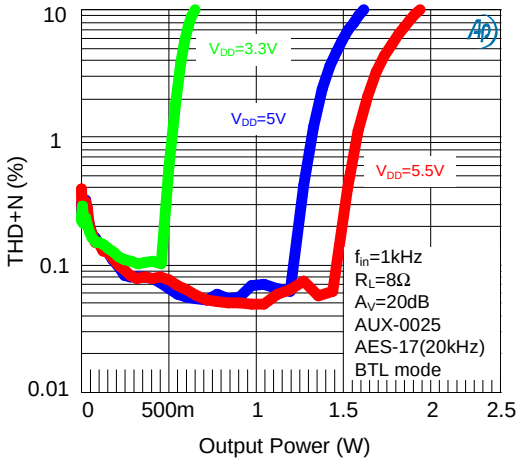
Efficiency vs. Output Power (8W)



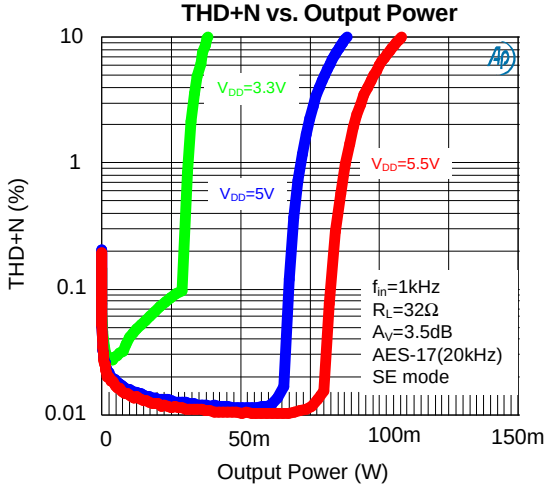
THD+N vs. Output Power



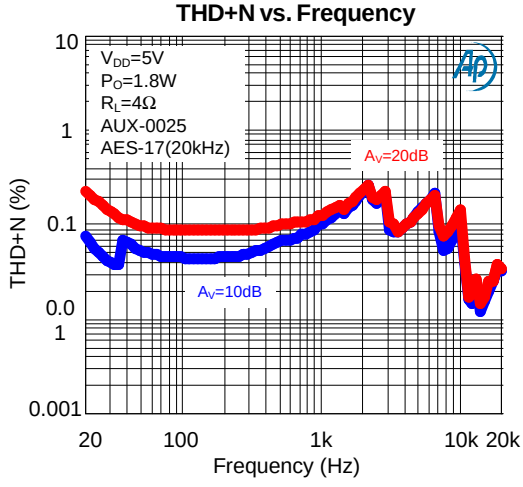
THD+N vs. Output Powe



THD+N vs. Output Power

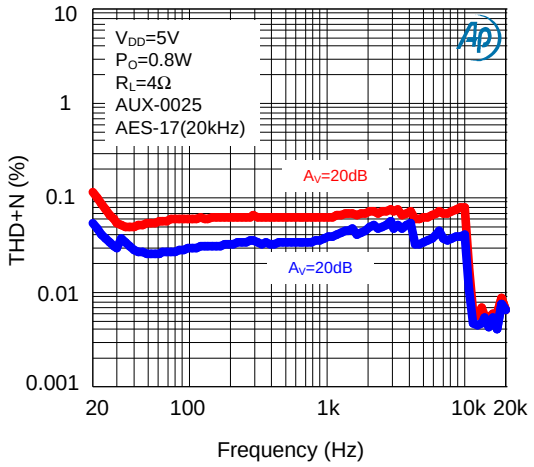


THD+N vs. Frequency

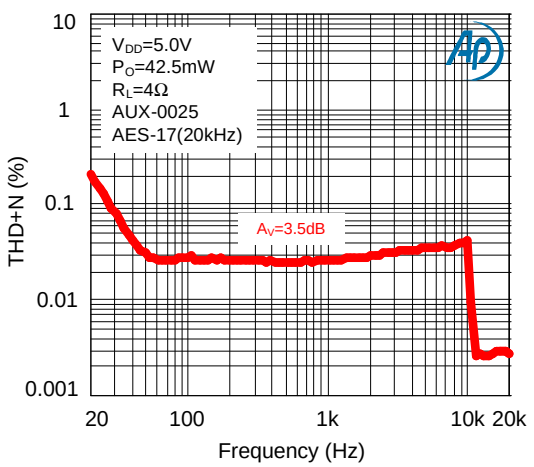


Typical Operating Characteristics

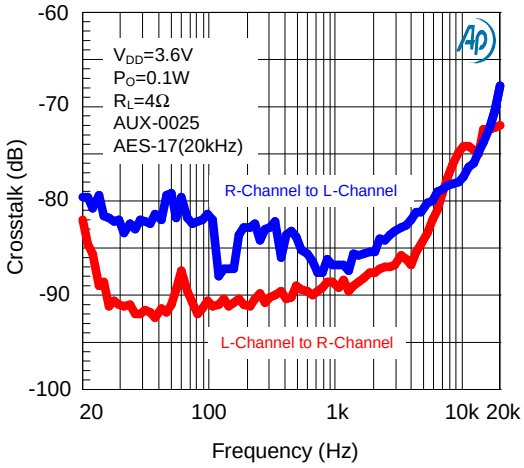
THD+N vs. Frequency



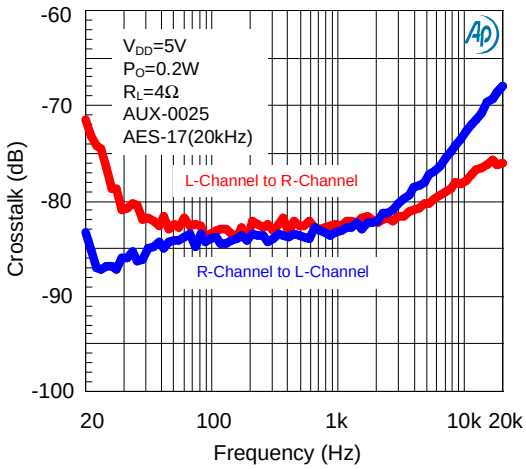
THD+N vs. Frequency



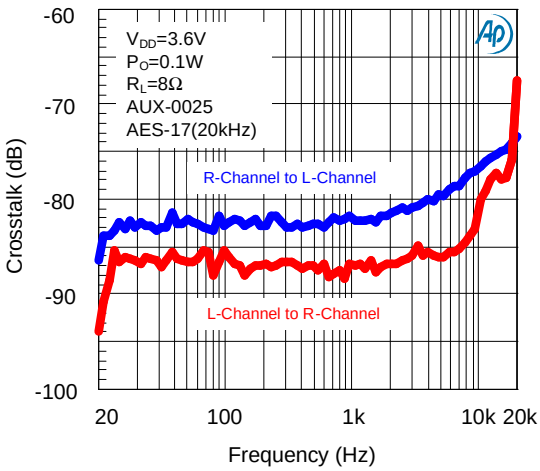
Crosstalk vs. Frequency



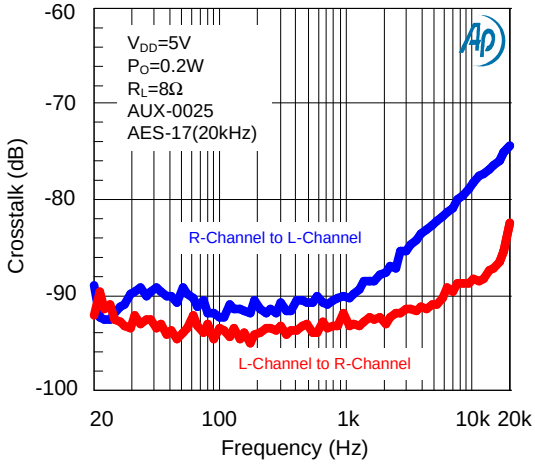
Crosstalk vs. Frequency



Crosstalk vs. Frequency

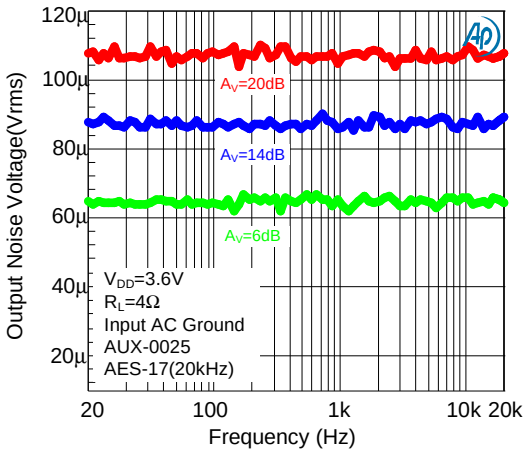


Crosstalk vs. Frequency

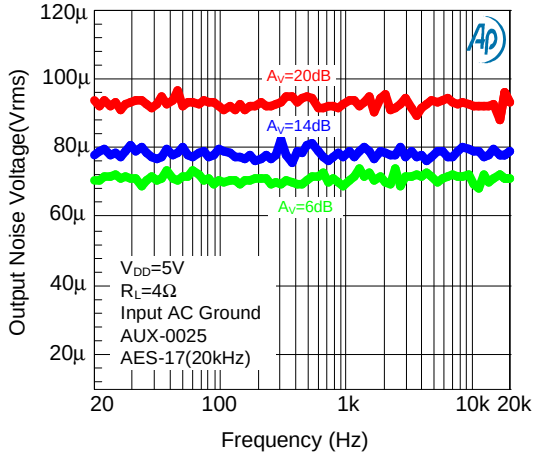


Typical Operating Characteristics

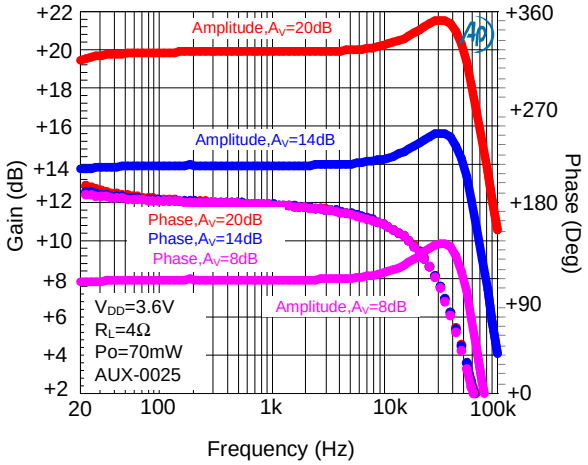
Output Noise Voltage vs. Frequency



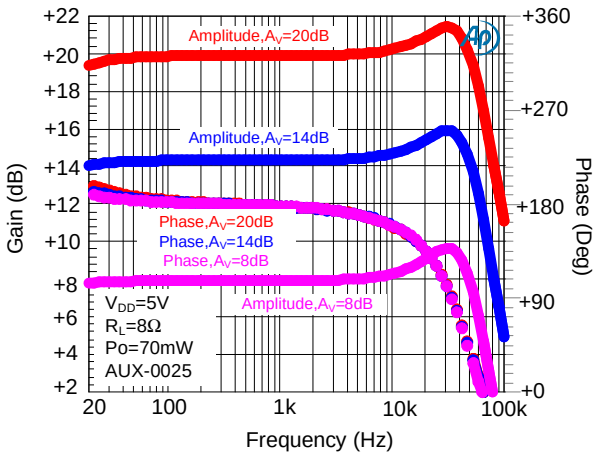
Output Noise Voltage vs. Frequency



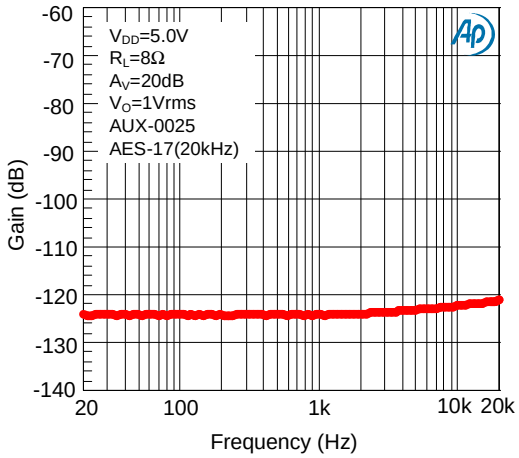
Frequency Response



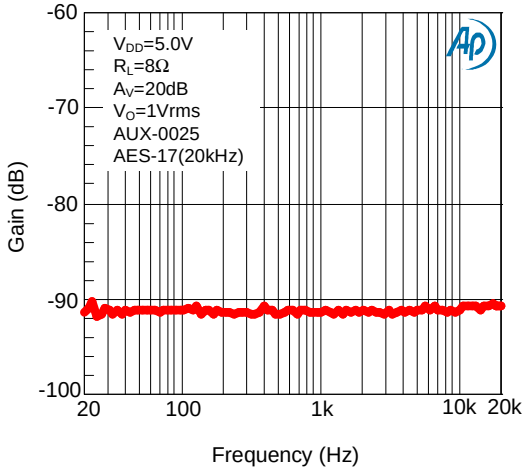
Frequency Response



Shutdown Attenuation vs. Frequency

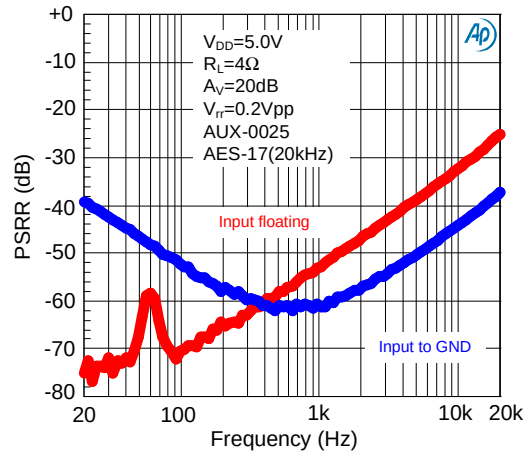


Mute Attenuation vs. Frequency

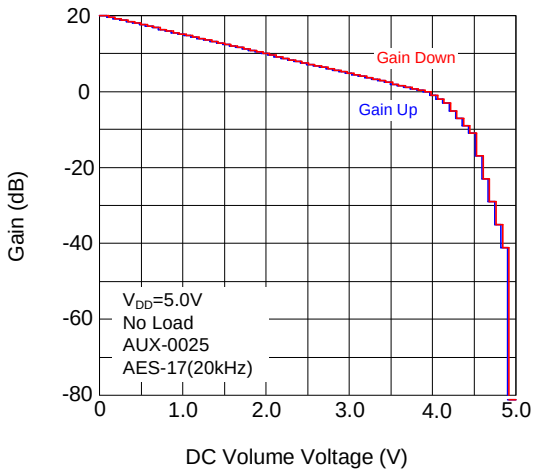


Typical Operating Characteristics

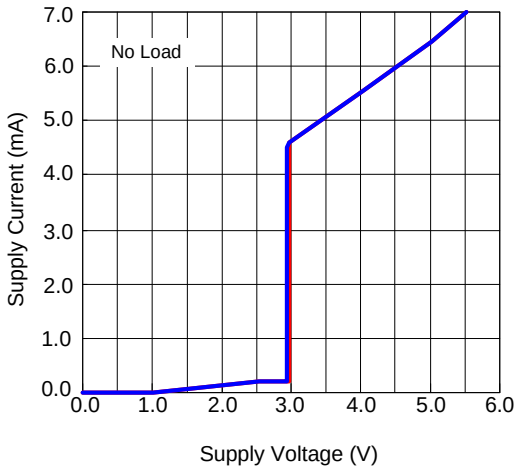
PSRR vs. Frequency



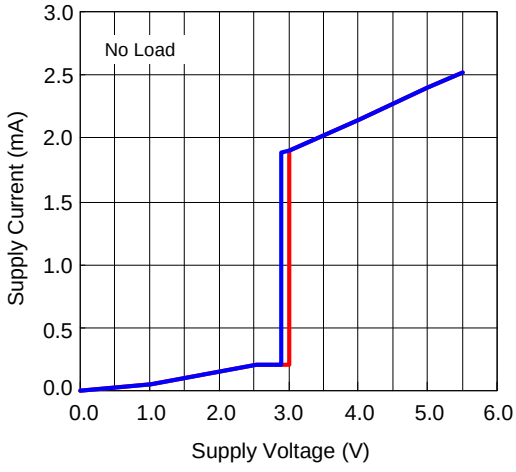
Gain vs. Volume Voltage



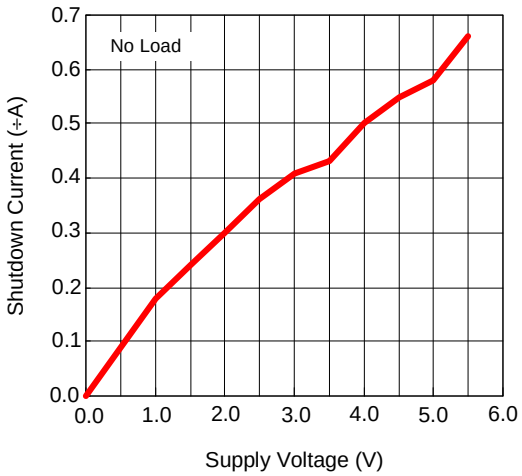
Supply Current vs. Supply Voltage (BTL)



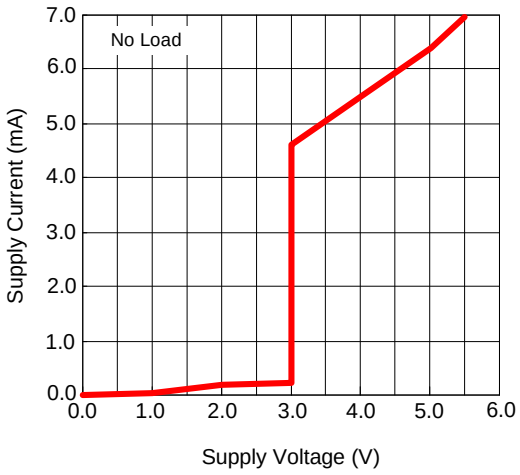
Supply Current vs. Supply Voltage (SE)



Shutdown Current vs. Supply Voltage

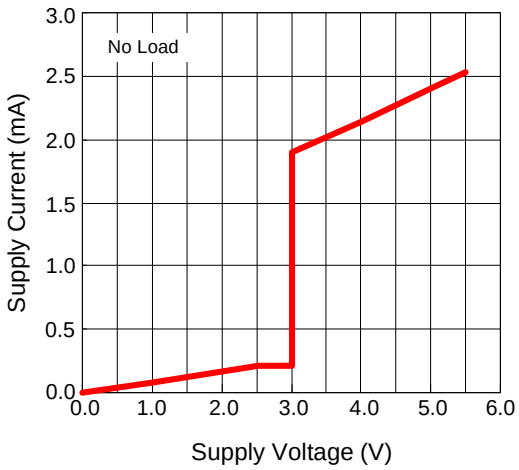


Mute Current vs. Supply Voltage(BTL)

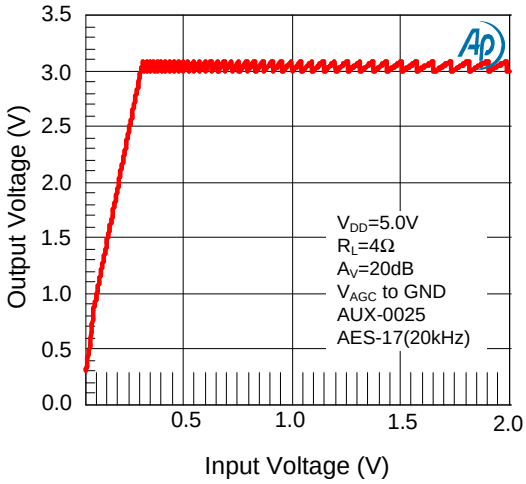


Typical Operating Characteristics

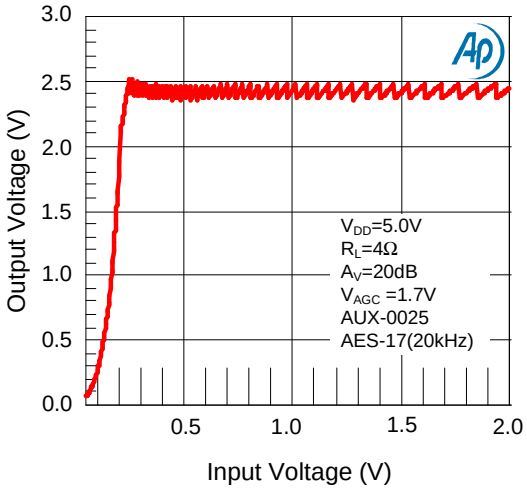
Mute Current vs. Supply Voltage(SE)



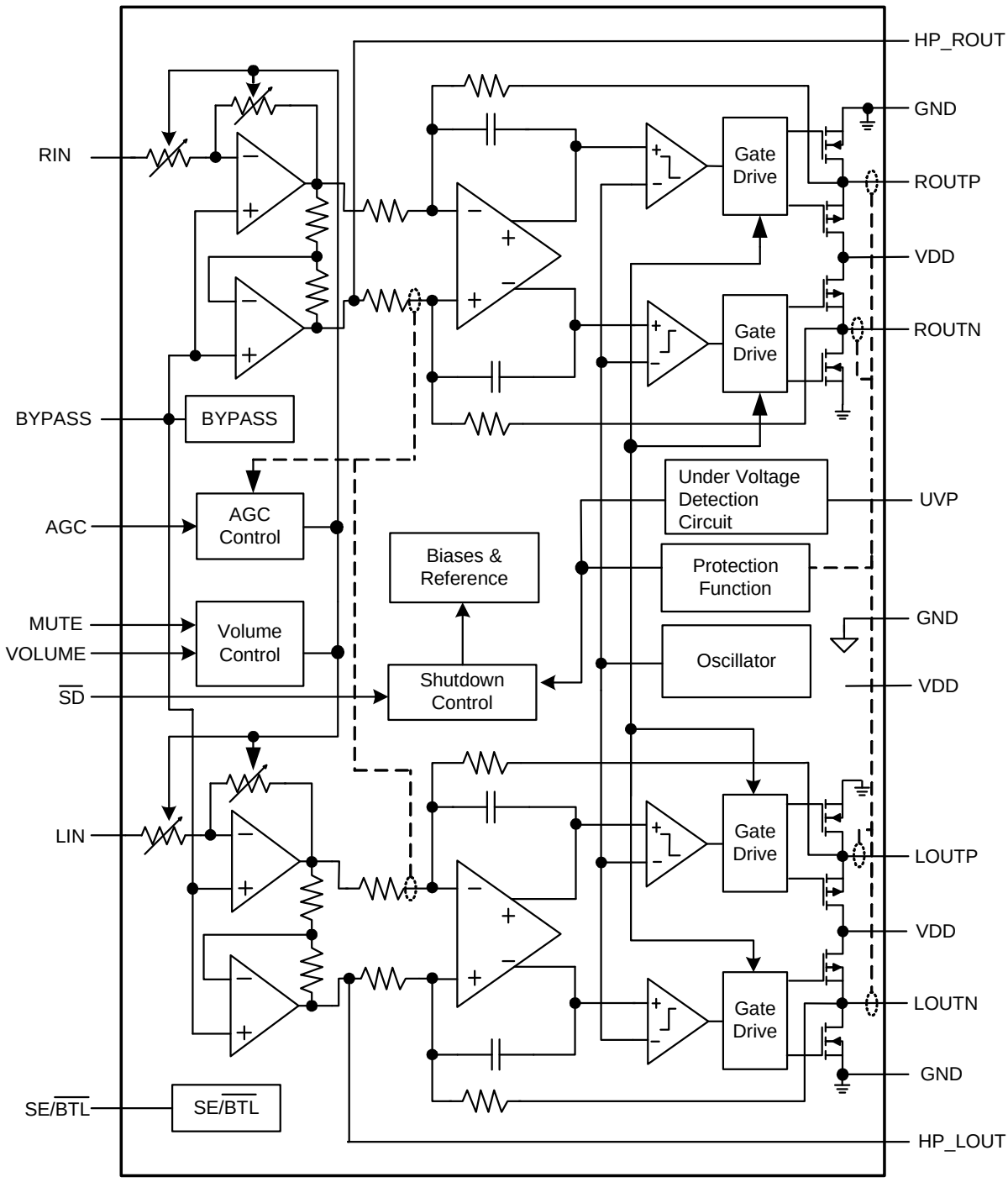
AGC Function
Output Power vs. Input AC



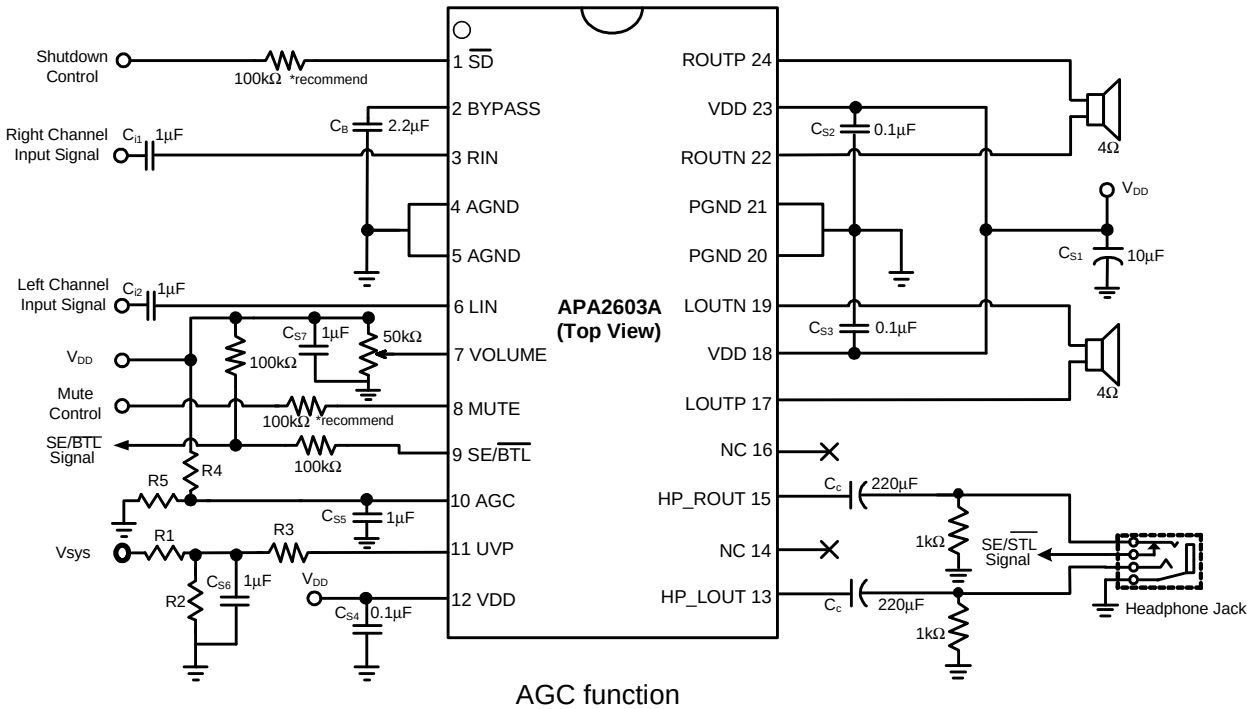
AGC Function
Output Power vs. Input AC



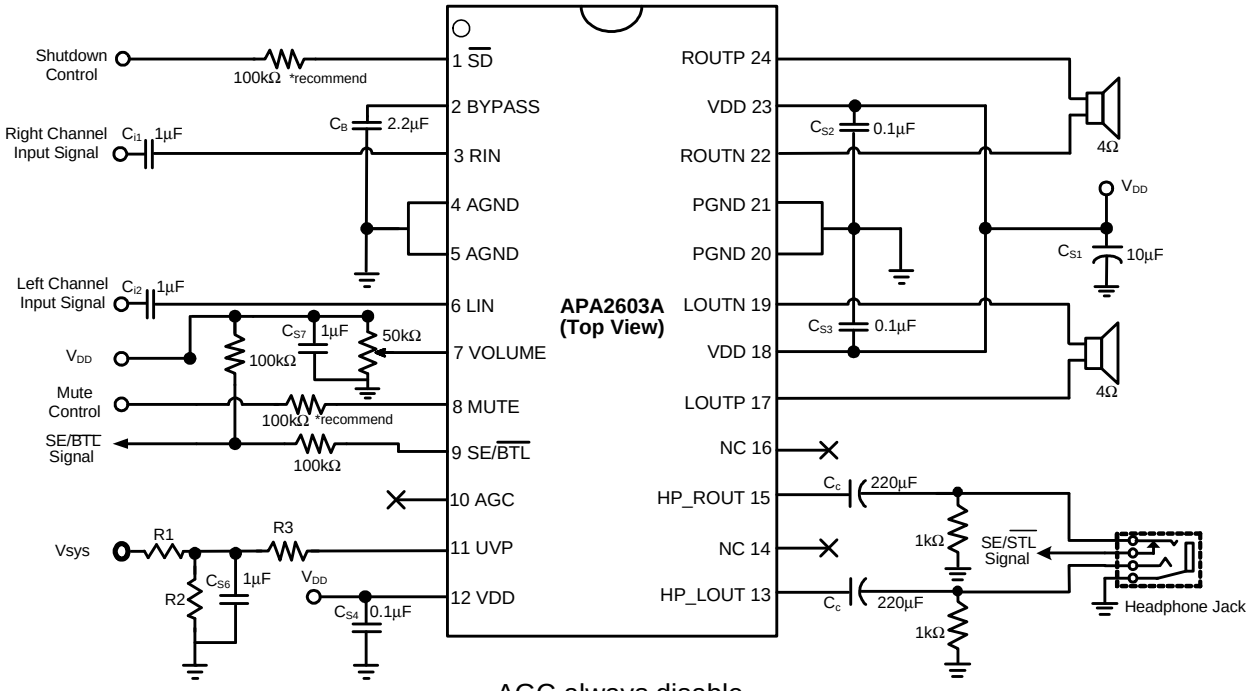
Block Diagram



Typical Application Circuit



AGC function



AGC always disable

DC Volume Control Table

Step	BTL Gain (dB)	SE Gain (dB)	Low (%)	High (%)	Recom(%)	Low (V)	High(V)	Recom(V)
1	20.0	3.5	0.00	1.84	0.00	0.000	0.092	0.00
2	19.6	3.2	2.33	3.39	2.86	0.116	0.170	0.14
3	19.2	2.9	3.82	4.97	4.40	0.191	0.249	0.22
4	18.8	2.6	5.40	6.53	5.97	0.270	0.326	0.30
5	18.4	2.3	6.96	8.06	7.51	0.348	0.403	0.38
6	17.6	1.7	8.49	9.62	9.06	0.425	0.481	0.45
7	17.2	1.4	10.05	11.18	10.61	0.502	0.559	0.53
8	16.8	1.1	11.61	12.73	12.17	0.580	0.637	0.61
9	16.4	0.8	13.19	14.29	13.74	0.659	0.714	0.69
10	16.0	0.5	14.74	15.83	15.29	0.737	0.791	0.76
11	15.6	0.2	16.30	17.38	16.84	0.815	0.869	0.84
12	15.2	-0.2	17.83	18.92	18.38	0.892	0.946	0.92
13	14.8	-0.5	19.37	20.49	19.93	0.969	1.025	1.00
14	14.4	-0.8	20.91	22.04	21.47	1.045	1.102	1.07
15	14.0	-1.2	22.48	23.59	23.04	1.124	1.180	1.15
16	13.6	-1.5	24.04	25.13	24.59	1.202	1.256	1.23
17	13.6	-1.5	25.58	26.67	26.12	1.279	1.333	1.31
18	13.2	-1.8	27.12	28.20	27.66	1.356	1.410	1.38
19	12.8	-2.2	28.63	29.76	29.19	1.432	1.488	1.46
20	12.4	-2.5	30.21	31.29	30.75	1.510	1.565	1.54
21	12.0	-2.9	31.75	32.83	32.29	1.587	1.641	1.61
22	11.6	-3.2	33.28	34.39	33.83	1.664	1.719	1.69
23	11.2	-3.6	34.82	35.92	35.37	1.741	1.796	1.77
24	10.8	-3.9	36.37	37.50	36.94	1.819	1.875	1.85
25	10.4	-4.3	37.93	39.04	38.48	1.897	1.952	1.92
26	10.0	-4.6	39.49	40.59	40.04	1.974	2.030	2.00
27	9.6	-5.0	41.02	42.15	41.58	2.051	2.107	2.08
28	9.2	-5.4	42.58	43.69	43.13	2.129	2.184	2.16
29	8.8	-5.7	44.14	45.23	44.68	2.207	2.261	2.23
30	8.4	-6.1	45.68	46.76	46.22	2.284	2.338	2.31
31	8.0	-6.4	47.21	48.32	47.76	2.361	2.416	2.39
32	7.6	-6.8	48.75	49.85	49.30	2.438	2.493	2.47

DC Volume Control Table (Cont.)

Step	BTL Gain (dB)	SE Gain (dB)	Low (%)	High (%)	Recom(%)	Low (V)	High(V)	Recom(V)
33	7.2	-7.2	50.31	51.41	50.86	2.515	2.571	2.54
34	6.8	-7.5	51.86	52.96	52.41	2.593	2.648	2.62
35	6.4	-7.9	53.38	54.52	53.95	2.669	2.726	2.70
36	6.0	-8.3	54.95	56.06	55.51	2.748	2.803	2.78
37	5.6	-8.6	56.49	57.60	57.04	2.825	2.880	2.85
38	5.2	-9.0	58.03	59.17	58.60	2.901	2.959	2.93
39	4.8	-9.4	59.60	60.71	60.16	2.980	3.036	3.01
40	4.4	-9.8	61.14	62.24	61.69	3.057	3.112	3.08
41	4.0	-10.1	62.65	63.78	63.22	3.133	3.189	3.16
42	3.6	-10.5	64.21	65.32	64.77	3.211	3.266	3.24
43	3.2	-10.9	65.75	66.83	66.29	3.287	3.342	3.31
44	2.8	-11.3	67.27	68.39	67.83	3.363	3.420	3.39
45	2.4	-11.6	68.82	69.95	69.39	3.441	3.497	3.47
46	2.0	-12.0	70.38	71.51	70.94	3.519	3.575	3.55
47	1.6	-12.4	71.94	73.06	72.50	3.597	3.653	3.62
48	1.2	-12.8	73.49	74.62	74.06	3.675	3.731	3.70
49	0.8	-13.1	75.05	76.17	75.61	3.753	3.809	3.78
50	0.4	-13.5	76.59	77.71	77.15	3.829	3.886	3.86
51	0.0	-13.9	78.12	79.23	78.68	3.906	3.962	3.93
52	-1.0	-14.9	79.66	80.78	80.22	3.983	4.039	4.01
53	-2.0	-15.8	81.20	82.32	81.76	4.060	4.116	4.09
54	-3.0	-16.8	82.75	83.88	83.32	4.138	4.194	4.17
55	-5.0	-18.8	84.29	85.43	84.86	4.214	4.272	4.24
56	-7.0	-20.7	85.82	86.99	86.41	4.291	4.350	4.32
57	-9.0	-22.7	87.38	88.53	87.95	4.369	4.426	4.40
58	-11.0	-24.7	88.92	90.06	89.49	4.446	4.503	4.47
59	-17.0	-30.7	90.46	91.62	91.04	4.523	4.581	4.55
60	-23.0	-36.9	92.01	93.20	92.61	4.601	4.660	4.63
61	-29.0	-43.0	93.57	94.71	94.14	4.678	4.736	4.71
62	-35.0	-49.3	95.10	96.25	95.68	4.755	4.813	4.78
63	-41.0	-55.3	96.64	97.81	97.22	4.832	4.890	4.86
64	-80.0	-80.0	98.20	100.00	100.00	4.910	5.000	5.00

Function Description

Class-D Operation

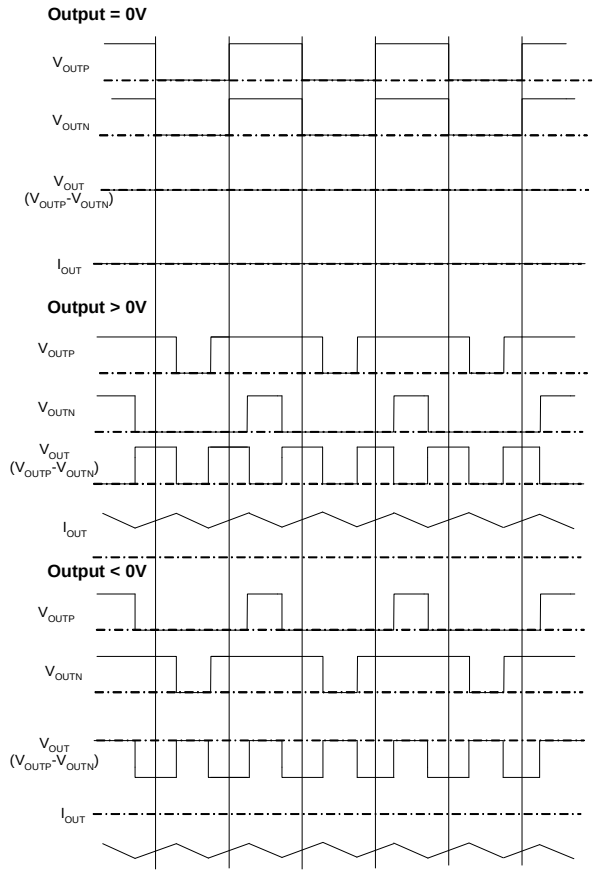


Figure1. The APA2603A Output Waveform (Voltage& Current)

The APA2603A power amplifier modulation scheme is shown in figure 1; the outputs V_{OUTP} and V_{OUTN} are in phase with each other when no input signals. When output > 0V, the duty cycle of V_{OUTP} is greater than 50% and V_{OUTN} is less than 50%; when Output <0V, the duty cycle of V_{OUTP} is less than 50% and V_{OUTN} is greater than 50%. This method reduces the switching current across the load, and reduces the I^2R losses in the load that improve the amplifier's efficiency.

This modulation scheme has very short pulses across the load, this making the small ripple current and very little loss on the load, and the LC filter can be eliminate in most applications. Added the LC filter can increase the efficiency by filter the ripple current.

Bypass Voltage

The bypass voltage is equal to $V_{DD}/2$, this voltage is for bias the internal preamplifier stages. The external capacitor for this reference (C_B) is a critical component and serves several important functions.

DC Volume Control Function

The APA2603A has an internal stereo volume control whose setting is the function of the DC voltage applied to the VOLUME input pin. The APA2603A volume control consists of 64 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps controlled by the DC voltage, are from +20dB to -80dB. Each gain step corresponds to a specific input voltage range, as shown in the table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in the "DC Volume Control Graph".

For the highest accuracy, the voltage shown in the "recommended voltage" column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions. The gains level have are 0.4dB/step from 20dB to 0dB; 1dB/step from 0dB to -3dB; 2dB/step from -3dB to -11dB and 6dB/step from -11dB to -41dB and the last step at -80dB as mute mode.

AGC (Non-Clipping) Function

The APA2603A provides the 64 steps non-clipping control, and the range is from 20dB to -80dB. When the output reaches the maximum power setting value, the internal Programmable Gain Amplifier (PGA) will decrease the gain for prevent the output waveform clipping. This feature prevents speaker damage from occurring clipping. Using the AGC pin to set the non-clipping function and limit the output power.

Function Description (Cont.)

Table 1: AGC Setting Threshold v.s Output Power

AGC Function	Output Power
VDD~0.45VDD or AGC Floating	Disable AGC Function
0.45VDD~0.27VDD	$Po = \frac{8(½VDD - V_{AGC})^2}{RL}$ x0.95
0.27VDD~GND	(Max Output Power 4Ω) Po=2.45W (Max Output Power 8Ω) Po=1.225W

MUTE Operation

When place the logic high on MUTE pin, the APA2603A's outputs runs at a constant 50% duty cycle, and the APA2603A is at mute state. Place the logic low on MUTE pin enables the outputs, and the output changes the duty cycle with the input signal. This pin could be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources. The MUTE pin must not be floating.

Shutdown Operation

In order to reduce power consumption while not in use, the APA2603A contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin for APA2603A. The trigger point between a logic high and logic low level is typically 0.65V. It is the best to switch between ground and the supply voltage V_{DD} to provide maximum device performance. By switching the $\overline{SD}$ pin to a low level, the amplifier enters a low-consumption-current state, I_{DD} for APA2603A is in shutdown mode. On normal operating, APA2603A's $\overline{SD}$ pin should pull to a high level to keep the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state changes.

Over-Current Protection

The APA2603A monitors the output current, and when the current exceeds the current-limit threshold, the APA2603A turn-off the output stage to prevent the output device from damages in over-current or short-circuit condition. The IC will turn-on the output buffer after 200ms, but if the over-current or short-circuits condition is still remain, it enters the Over-Current protection again. The situation will circulate until the over-current or short-circuits has be removed.

Thermal Protection

The over-temperature circuit limits the junction temperature of the APA2603A. When the junction temperature exceeds T_J=+165°C, a thermal sensor turns off the output buffer, allowing the devices to cool. The thermal sensor allows the amplifier to start-up after the junction temperature down about 140 °C. The thermal protection is designed with a 25 °C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Under-Voltage Protection

External under voltage detection can be used to Shutdown the APA2603A before an input device can generate a pop. The shutdown threshold at the UVP pin is 1.2V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as below:

With the condition: R3 >> R1// R2

VUVP=[1.2-(5.7μAxR3)] x (R1+R2)/R2

Hysteresis=4.6μA x R3 x (R1+R2)/R2

For example, to obtain VUVP=3.7V and 0.9V hysteresis, R1=3kΩ, R2=1kΩ and R3=50kΩ. Only if external voltage V_{system} is lower than the shutdown thershold VUVP, the APA2603A is in shutdown mode. On the other hand, V_{system} could be pulled higher than V_{Hys} (VUVP + hysteresis=4.6V) to keep the IC out of shutdown mode.

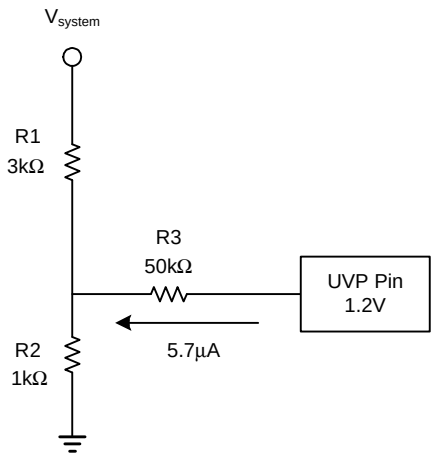


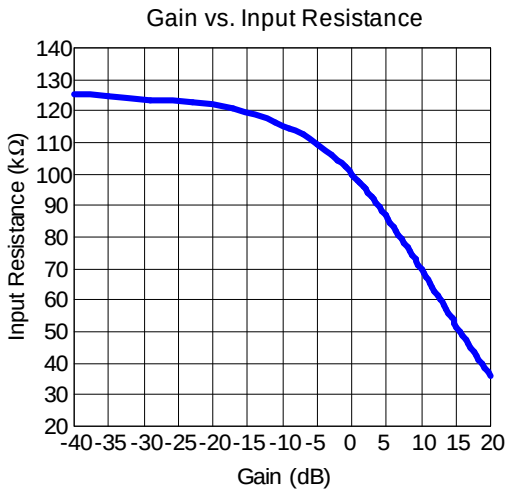
Figure2. Under-Voltage Protection

Application Information

Square Wave into the Speaker

Apply the square wave into the speaker may cause the voice coil of speaker jumping out the air gap and defacing the voice coil. However, this depends on the amplitude of square wave is high enough and the bandwidth of speaker is higher than the square wave¡¦s frequency. For 500kHz switching frequency, this is not issued for the speaker because the frequency is beyond the audio band and can¡¦t significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistor, R_i



For achieving the 64 steps gain setting, it varies the input resistance network (R_i & R_f) of amplifier. The input resistor's range form smallest to maximum is about 3.5 times. Therefore, the input high-pass filter's low cutoff frequency will change 3.5 times from low to high. The cutoff frequency can be calculated by equation 1.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Where R_i is 36kΩ (minimum) and the specification calls for a flat bass response down to 50Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

When the input resistance variation is considered, the C_i is 0.08µF, so a value in the range of 0.01µF to 0.022µF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifiers' input in most applications because the DC level of the amplifiers' inputs are held at $V_{DD}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_B

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The bypass capacitance sffects the startiup time. It is determined in the following wquation:

$$T_{START-UP}=0.5(sec/\mu F) \times C_B + 0.2(sec) \quad (3)$$

The capacitor location on the bypass pin should be as close to the device as possible. The effect of a larger half bypass capacitor is improved PSRR due to increased half-supply stability. The selection of bypass capacitors, especially C_B, is thus dependent upon desired PSRR requirements, click and pop performance.To avoid the start-up pop noise occurred, choose C_i which is not larger than C_B.

Application Information (Cont.)

Ferrite Bead Selection

If the traces form APA2603A to speaker are short, the ferrite bead filters can reduce the high frequency radiated to meet the FCC & CE required.
A ferrite that has very low impedance at low frequencies and high impedance at high frequencies (above 1 MHz) is recommended.

Output Low-Pass Filter

If the traces form APA2603A to speaker are short, it doesn't require output filter for FCC & CE standard.
A ferrite bead may be needed if it's failing the test for FCC or CE tested without the LC filter. The figure 2 is the sample for added ferrite bead; the ferrite shows choosing high impedance in high frequency.

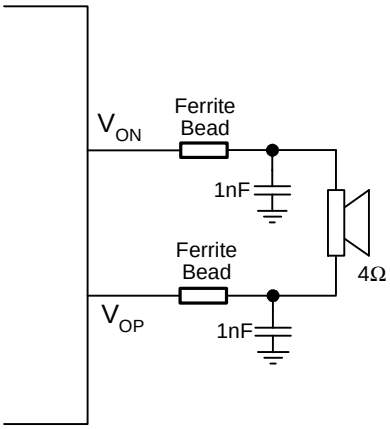


Figure 2. Ferrite bead output filter

Figure 3 and 4 are examples for added the LC filter (Butterworth), it's recommended for the situation that the trace form amplifier to speaker is too long and needs to eliminate the radiated emission or EMI.

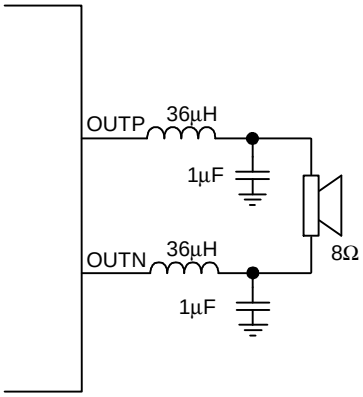


Figure 3. LC output filter for 8Ω speaker

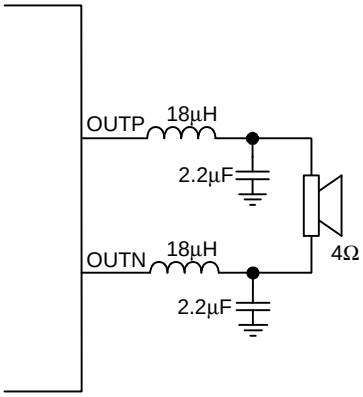


Figure 4. LC output filter for 4Ω speaker

Figure 3 and 4's low pass filter cut-off frequency are 25kHz (F_C).

$$f_{C(lowpass)} = \frac{1}{2\pi\sqrt{LC}} \quad (5)$$

Power-Supply Decoupling Capacitor, C_S

The APA2603A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

Application Information (Cont.)

Power-Supply Decoupling Capacitor, C_s (Cont.)

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device VDD pin for works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Layout Recommendation

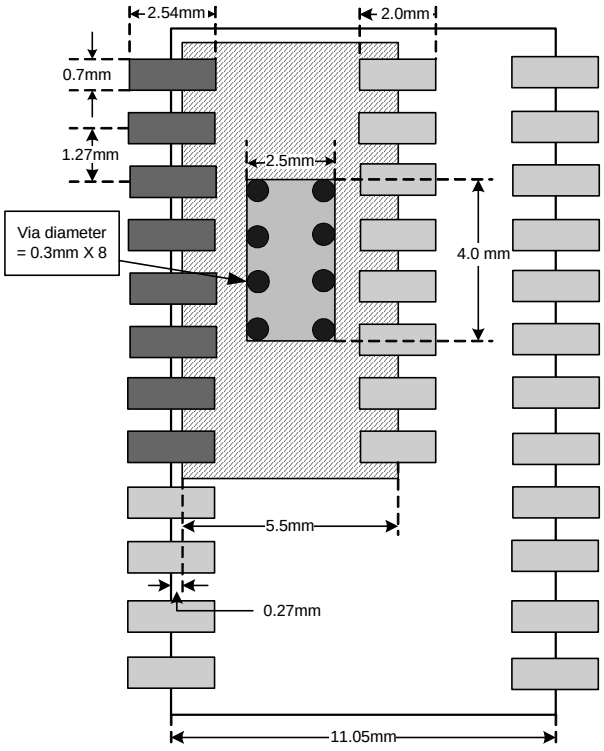


Figure 5. APA2603 SOP-16P & APA2603A SOP-24co-layout Land Pattern Recommendation

1. All components should be placed close to the APA2603A. For example, the input capacitor (C_i) should be close to APA2603A's input pins to avoid causing noise coupling to APA2603A's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA2603A's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil) and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The SOP-16P Thermal PAD should be soldered on PCB
6. APA2603 and APA2603A share the first 8 pins to avoid soldering short. APA2603's right half pads are connected to APA2603A by lines.

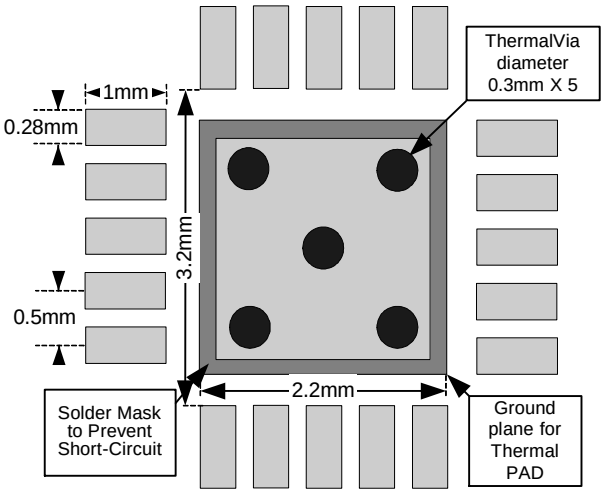
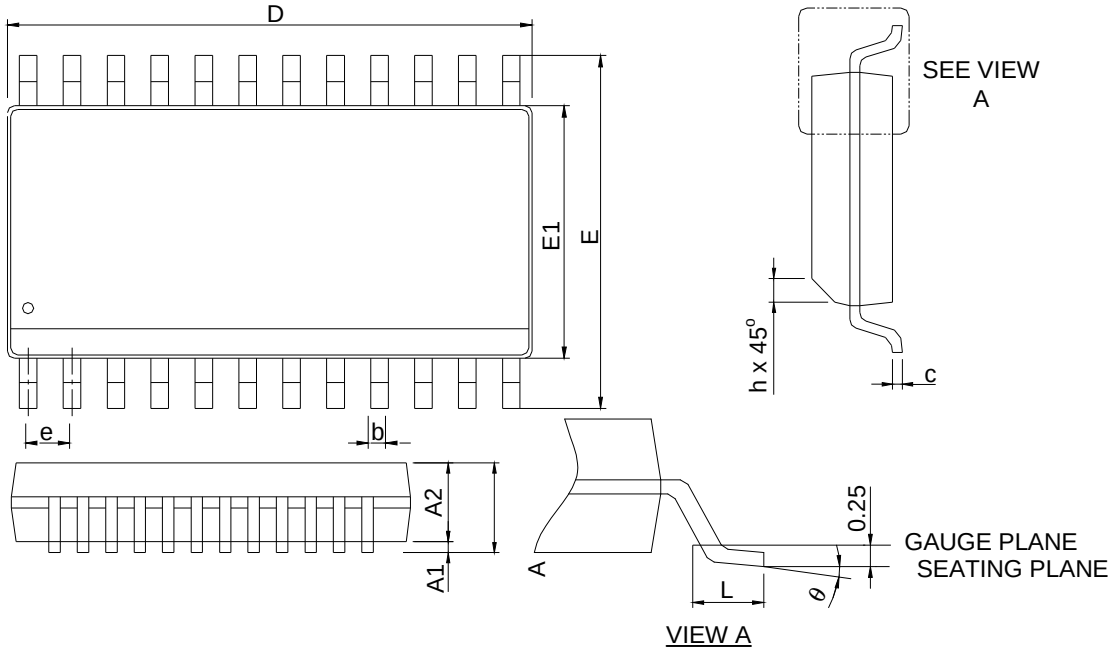


Figure 6. QFN4x4-20A Land Pattern Recommendation

1. All components should be placed close to the APA2603A. For example, the input capacitor (C_i) should be close to APA2603A's input pins to avoid causing noise coupling to APA2603A's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA2603A's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The QFN4X4-20A Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short-circuit) except the Thermal PAD area.

Package Information

SOP-24

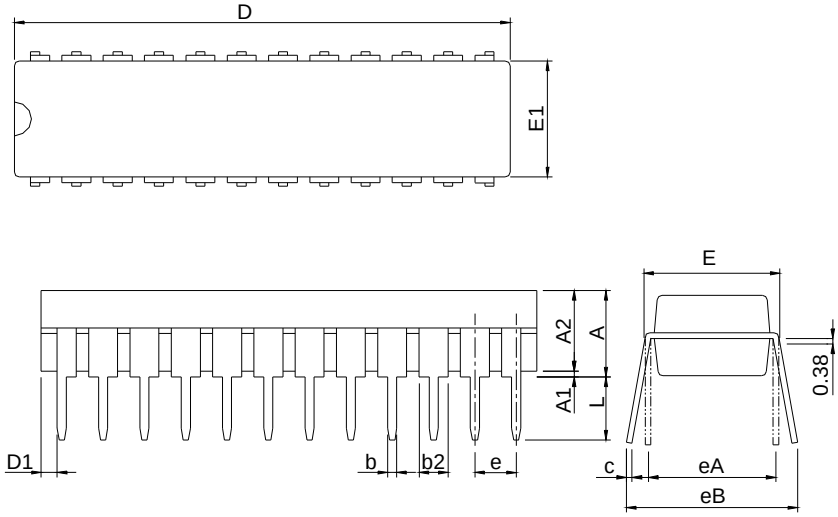


SYMBOL	SOP-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		2.65		0.104
A1	0.10	0.30	0.004	0.012
A2	2.05		0.081	
b	0.31	0.51	0.012	0.020
c	0.20	0.33	0.008	0.013
D	15.20	15.60	0.598	0.614
E	10.10	10.50	0.398	0.413
E1	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
h	0.25	0.75	0.010	0.030
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-013 AD.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

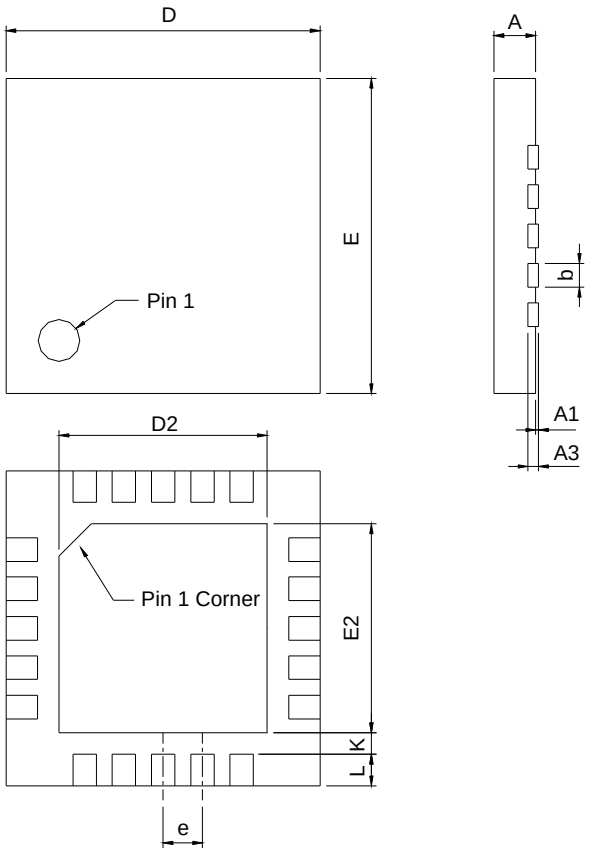
DIP-24



SYMBOL	DIP-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	29.46	30.35	1.160	1.195
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Package Information

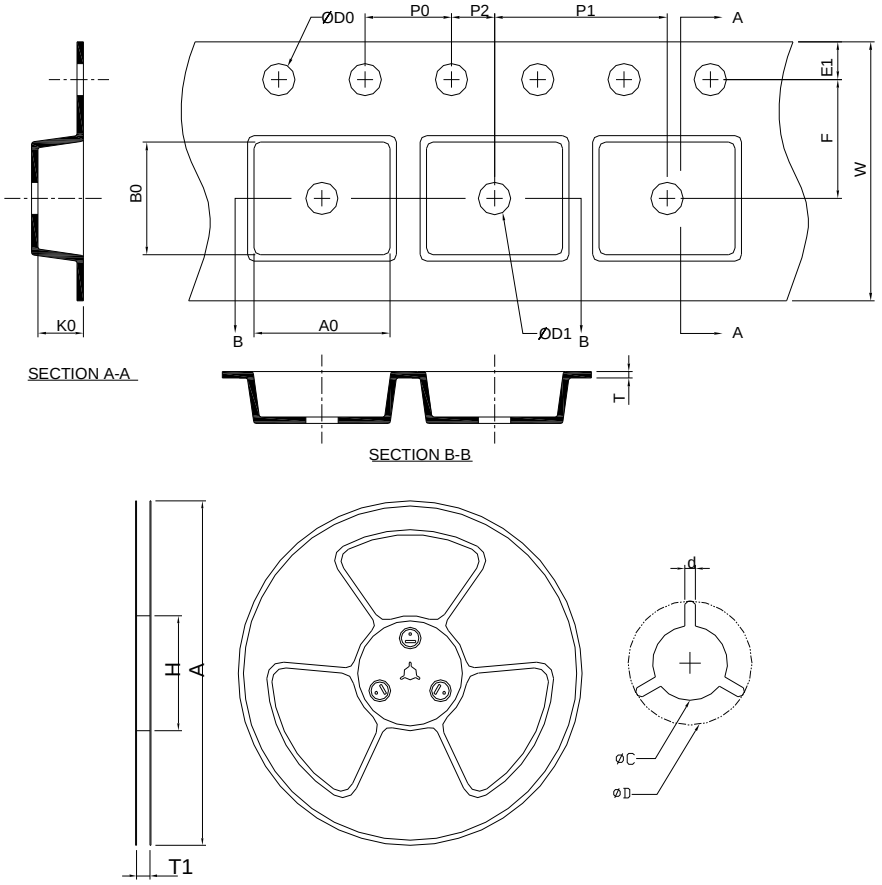
QFN4x4-20A



SYMBOL	QFN4x4-20A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.00	2.50	0.079	0.098
E	3.90	4.10	0.154	0.161
E2	2.00	2.50	0.079	0.098
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 VGGD-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-24	330.0±2.00	50 MIN.	24.40+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	24.0±0.30	1.75±0.10	11.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	10.9±0.20	15.80±0.20	3.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
QFN4x4-20A	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

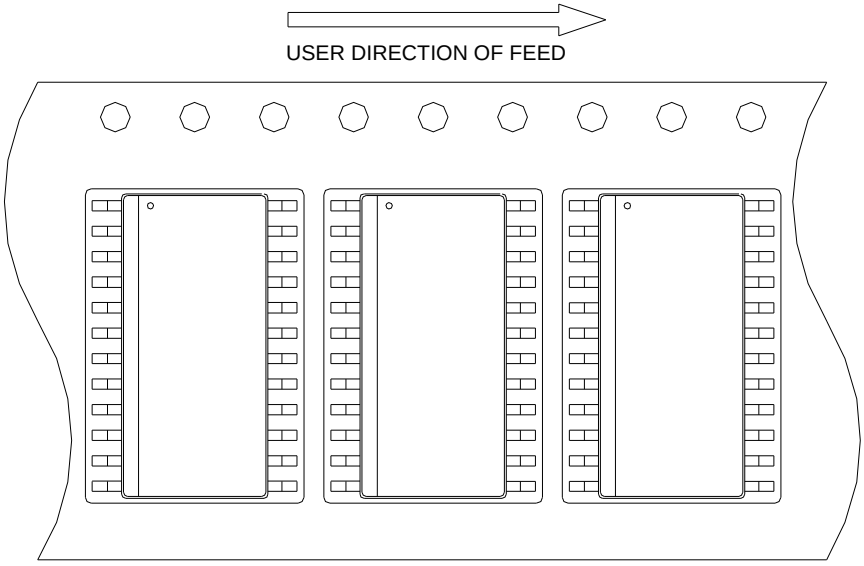
(mm)

Devices Per Unit

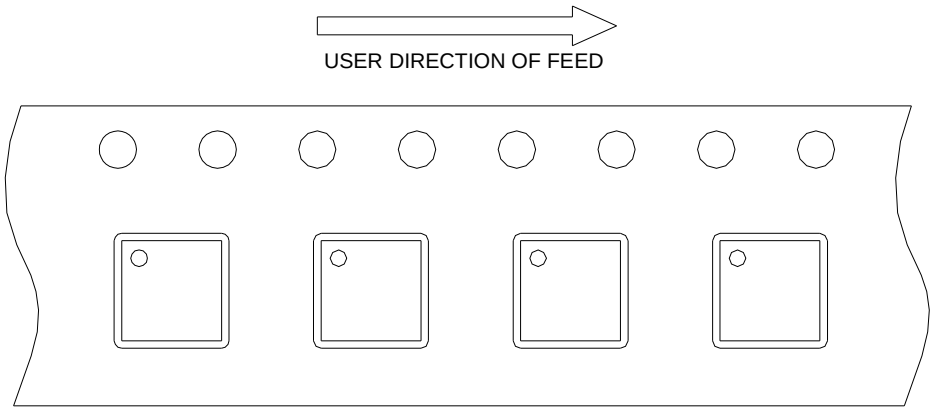
Application	Unit	Quantity
SOP-24	Tape & Real	1000
QFN4x4-20A	Tape & Real	3000

Taping Direction Information

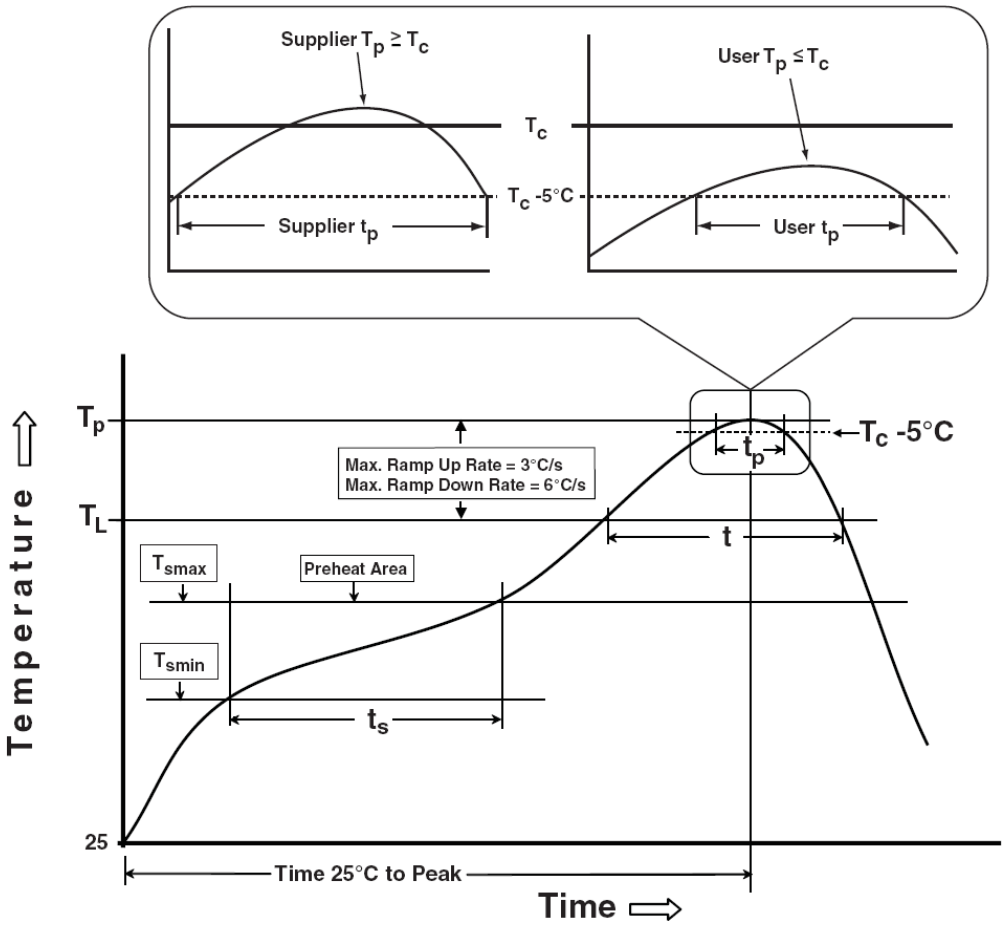
SOP-24



QFN4x4-20A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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