

M210x Series

5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML, Clock Oscillator



Ordering Information

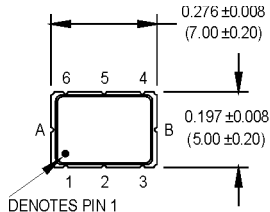
| | | | | | | | | | |
|--------------------------------|------|---|---|---|---|---|---|---------|-----|
| | M210 | 0 | 6 | 8 | B | P | N | 00.0000 | MHz |
| Product Series | | | | | | | | | |
| Supply Voltage | | | | | | | | | |
| 0: 3.3 V | | | | | | | | | |
| 1: 2.5 V | | | | | | | | | |
| 2: 1.8 V | | | | | | | | | |
| Temperature Range | | | | | | | | | |
| 2: -40°C to +85°C (see Note 1) | | | | | | | | | |
| 6: -20°C to +70°C | | | | | | | | | |
| Stability | | | | | | | | | |
| 4: ±50 ppm | | | | | | | | | |
| 3: 100 ppm | | | | | | | | | |
| 8: ±20 ppm | | | | | | | | | |
| Enable/Disable | | | | | | | | | |
| B: Enable High (pin 1) | | | | | | | | | |
| G: Enable High (pin 2) | | | | | | | | | |
| S: Enable Low (pin 1) | | | | | | | | | |
| M: Enable Low (pin 2) | | | | | | | | | |
| U: No Enable/Disable | | | | | | | | | |
| Logic Type | | | | | | | | | |
| P: LVPECL | | | | | | | | | |
| L: LVDS | | | | | | | | | |
| M: CML | | | | | | | | | |
| Package/Lead Configuration | | | | | | | | | |
| N: 5x7 mm Leadless | | | | | | | | | |
| Frequency (customer specified) | | | | | | | | | |

Features:

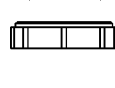
- Featuring *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 150 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

Applications:

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications



DENOTES PIN 1



ACTUAL SIZE



All dimensions in inches (mm).

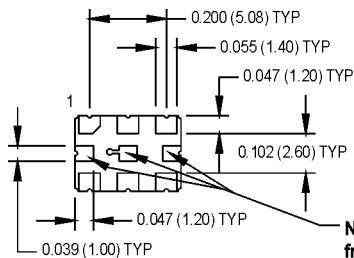


PIN 1 ENABLE

- Pad1: Enable/Disable
- Pad2: N/C
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML)
- Pad5: Output \bar{Q} (LVPECL, LVDS, CML)
- Pad6: Vcc
- PadA: Do not connect!
- PadB: Do not connect!
- PadC: Do not connect!

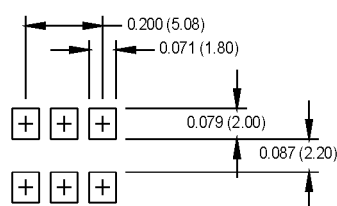
PIN 2 ENABLE

- Pad1: N/C
- Pad2: Enable/Disable
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML)
- Pad5: Output \bar{Q} (LVPECL, LVDS, CML)
- Pad6: Vcc
- PadA: Do not connect!
- PadB: Do not connect!
- PadC: Do not connect!



NOTE: These 3 pads must be isolated from any traces or vias appearing beneath this port.

SUGGESTED SOLDER PAD LAY OUT



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Revision: 8-16-06

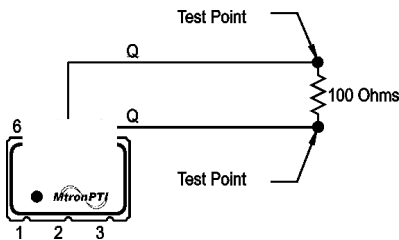
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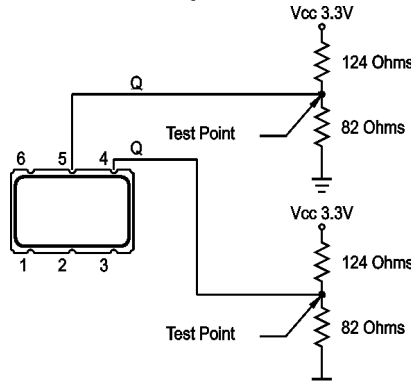


| PARAMETER | Symbol | Min. | Typ. | Max. | Units | Condition/Notes | |
|----------------------------|--------------------------------|---|------------|------------------------|--------|--|------------|
| Frequency Range | F | 150 | | 1400 | MHz | See Note 2 | |
| Operating Temperature | T _A | (See ordering information) | | | | | See Note 1 |
| Storage Temperature | T _S | -55 | | +125 | °C | | |
| Frequency Stability | ΔF/F | (See ordering information) | | | | | See Note 3 |
| Aging | | | | | | | |
| 1st Year | | -3 | | +3 | ppm | | |
| Thereafter (per year) | | -1 | | +1 | ppm | | |
| Supply Voltage | V _{CC} | 1.71 | 1.8 | 1.89 | V | | |
| | | 2.375 | 2.5 | 2.625 | V | | |
| | | 3.135 | 3.3 | 3.465 | V | | |
| Input Current | I _{CC} | | | 125 | mA | LVPECL/LVDS/CML | |
| Load | | 50 Ohms to (V _{CC} - 2) V _{DC} 100 Ohm differential load | | | | See Note 4 LVPECL Waveform LVDS/CML Waveform | |
| Symmetry (Duty Cycle) | | 45 | | 55 | % | @ 50% of waveform | |
| Output Skew | | | TBD | | | | |
| Differential Voltage | | 350 | 425 TBD | 500 | mVppd | LVDS CML | |
| Common Mode Output Voltage | V _{CM} | | 1.2 | | V | LVDS | |
| Logic "1" Level | V _{OH} | V _{CC} - 1.02 | | | V | LVPECL | |
| Logic "0" Level | V _{OL} | | | V _{CC} - 1.63 | V | LVPECL | |
| Rise/Fall Time | T _r /T _f | | 0.23 | 0.50 | ns | @ 20/80% LVPECL | |
| Enable Function | | 80% V _{CC} min. or N/C: output active 20% V _{CC} max.: output disables to high-Z | | | | Output Option B or G | |
| | | 20% V _{CC} max.: output active 80% V _{CC} min.: output disables to high-Z | | | | Output Option S or M | |
| Start up Time | | | 10 | | ms | | |
| Phase Jitter @ 622.08 MHz | φ _J | | 0.3 | | ps RMS | Integrated 12 kHz – 20 MHz | |
| Phase Noise | | | | | | @ 622.08 MHz | |
| 10 Hz | | | -50 | | | dBc/Hz | |
| 100 Hz | | | -80 | | | dBc/Hz | |
| 1 KHz | | | -106 | | | dBc/Hz | |
| 10 KHz | | | -117 | | | dBc/Hz | |
| 100 KHz | | | -120 | | | dBc/Hz | |
| 1 MHz | | | -130 | | | dBc/Hz | |
| 10 MHz | | | -147 | | | dBc/Hz | |
| 40 MHz | | | -150 | | | dBc/Hz | |
| Environmental | | | | | | | |
| Mechanical Shock | | Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave) | | | | | |
| Vibration | | Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz) | | | | | |
| Hermeticity | | Per MIL-STD-202, Method 112, (1x10 ⁻³ atm. cc/s of Helium) | | | | | |
| Thermal Cycle | | Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles) | | | | | |
| Solderability | | Per EIAJ-STD-002 | | | | | |
| Soldering Conditions | | +240°C max. for 10 secs. | | | | | |

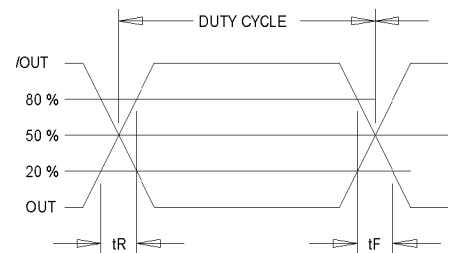
- Note 1: If the device is powered up below -20°C and then the ambient temperature rises 105°C during normal operation, the output will be interrupted for approximately 2-3 ms. A correction is in process and will be available Q1 2007.
- Note 2: Contact factory for exact frequency availability over 945 MHz
- Note 3: Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.
- Note 4: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.



LVDS Load Circuit



3.3V LVPECL Load Circuit



Output Waveform: LVDS/CML/PECL

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