

# HD74LS95B

## 4-bit Parallel Access Shift Register

REJ03D0424-0400

Rev.4.00

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The 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three mode operation:

- Parallel (broadside) load
- Shift right (the direction  $Q_A$  toward  $Q_D$ )
- Shift left (the direction  $Q_D$  toward  $Q_A$ )

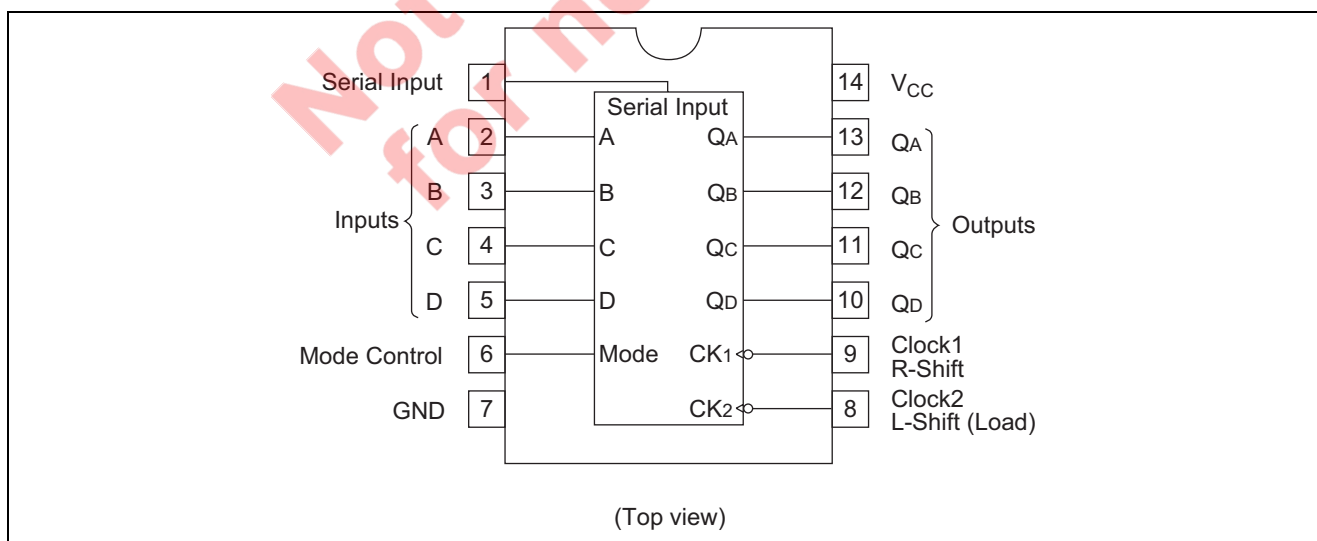
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited. Shift right is accomplished on the high-to-low transition of clock-1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock-2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop ( $Q_D$  to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock-1 and clock-2 if both modes can be clocked from the same source. Changes at the mode control inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

### Features

- Ordering Information

| Part Name     | Package Type       | Package Code<br>(Previous Code) | Package<br>Abbreviation | Taping Abbreviation<br>(Quantity) |
|---------------|--------------------|---------------------------------|-------------------------|-----------------------------------|
| HD74LS95BFPEL | SOP-14 pin (JEITA) | PRSP0014DF-B<br>(FP-14DAV)      | FP                      | EL (2,000 pcs/reel)               |

### Pin Arrangement



## Function Table

| Mode control | Inputs |      |        |                  |                  |                  |   | Outputs         |                 |                 |                 |
|--------------|--------|------|--------|------------------|------------------|------------------|---|-----------------|-----------------|-----------------|-----------------|
|              | Clocks |      | Serial | Parallel         |                  |                  |   | Q <sub>A</sub>  | Q <sub>B</sub>  | Q <sub>C</sub>  | Q <sub>D</sub>  |
|              | 2(L)   | 1(R) |        | A                | B                | C                | D |                 |                 |                 |                 |
| H            | H      | X    | X      | X                | X                | X                | X | Q <sub>AO</sub> | Q <sub>BO</sub> | Q <sub>CO</sub> | Q <sub>DO</sub> |
| H            | ↓      | X    | X      | a                | b                | c                | d | a               | b               | c               | d               |
| H            | ↓      | X    | X      | Q <sub>B</sub> * | Q <sub>C</sub> * | Q <sub>D</sub> * | d | Q <sub>Bn</sub> | Q <sub>Cn</sub> | Q <sub>Dn</sub> | d               |
| L            | L      | H    | X      | X                | X                | X                | X | Q <sub>AO</sub> | Q <sub>BO</sub> | Q <sub>CO</sub> | Q <sub>DO</sub> |
| L            | X      | ↓    | H      | X                | X                | X                | X | H               | Q <sub>An</sub> | Q <sub>Bn</sub> | Q <sub>Cn</sub> |
| L            | X      | ↓    | L      | X                | X                | X                | X | L               | Q <sub>An</sub> | Q <sub>Bn</sub> | Q <sub>Cn</sub> |
| ↑            | L      | L    | X      | X                | X                | X                | X | Q <sub>AO</sub> | Q <sub>BO</sub> | Q <sub>CO</sub> | Q <sub>DO</sub> |
| ↓            | L      | L    | X      | X                | X                | X                | X | Q <sub>AO</sub> | Q <sub>BO</sub> | Q <sub>CO</sub> | Q <sub>DO</sub> |
| ↓            | L      | H    | X      | X                | X                | X                | X | Q <sub>AO</sub> | Q <sub>BO</sub> | Q <sub>CO</sub> | Q <sub>DO</sub> |
| ↑            | H      | L    | X      | X                | X                | X                | X | Q <sub>AO</sub> | Q <sub>BO</sub> | Q <sub>CO</sub> | Q <sub>DO</sub> |
| ↑            | H      | H    | X      | X                | X                | X                | X | Q <sub>AO</sub> | Q <sub>BO</sub> | Q <sub>CO</sub> | Q <sub>DO</sub> |

Notes: 1. H; high level, L; low level, X; irrelevant

2. ↑; transition from low to high level

3. ↓; transition from high to low level

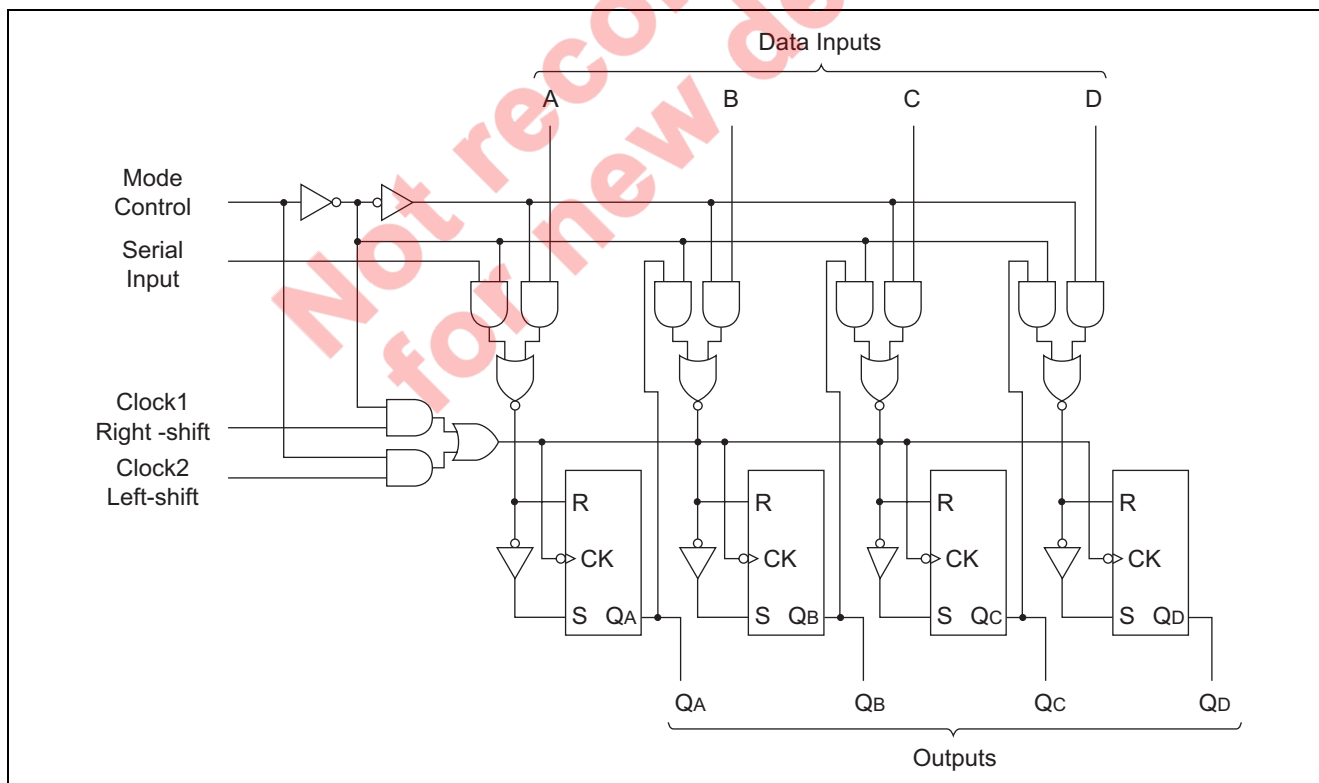
4. a to d; the level of steady-state input at inputs A, B, C, or D, respectively.

5. Q<sub>AO</sub> to Q<sub>DO</sub>; the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the indicated steady-state input conditions were established.

6. Q<sub>An</sub> to Q<sub>Dn</sub>; the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the most-recent (↑) transition of the clock.

7. \*; Shifting left require external connection of Q<sub>B</sub> to A, Q<sub>C</sub> to B, and Q<sub>D</sub> to C. Serial data is entered at input D.

## Block Diagram



## Absolute Maximum Ratings

| Item                | Symbol    | Ratings     | Unit |
|---------------------|-----------|-------------|------|
| Supply voltage      | $V_{CC}$  | 7           | V    |
| Input voltage       | $V_{IN}$  | 7           | V    |
| Power dissipation   | $P_T$     | 400         | mW   |
| Storage temperature | $T_{stg}$ | -65 to +150 | °C   |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

| Item                  | Symbol          | Min  | Typ  | Max  | Unit |
|-----------------------|-----------------|------|------|------|------|
| Supply voltage        | $V_{CC}$        | 4.75 | 5.00 | 5.25 | V    |
| Output current        | $I_{OH}$        | —    | —    | -400 | μA   |
|                       | $I_{OL}$        | —    | —    | 8    | mA   |
| Operating temperature | $T_{opr}$       | -20  | 25   | 75   | °C   |
| Clock frequency       | $f_{clock}$     | 0    | —    | 25   | MHz  |
| Clock pulse width     | $t_w (CK)$      | 20   | —    | —    | ns   |
| Setup time            | $t_{su}$        | 20   | —    | —    | ns   |
| Hold time             | $t_h$           | 10   | —    | —    | ns   |
| Enable time 1         | $t_{enable 1}$  | 20   | —    | —    | ns   |
| Enable time 2         | $t_{enable 2}$  | 20   | —    | —    | ns   |
| Inhibit time 1        | $t_{inhibit 1}$ | 20   | —    | —    | ns   |
| Inhibit time 2        | $t_{inhibit 2}$ | 20   | —    | —    | ns   |

## Electrical Characteristics

( $T_a = -20$  to  $+75$  °C)

| Item                         | Symbol   | min. | typ.* | max. | Unit | Condition                                                               |
|------------------------------|----------|------|-------|------|------|-------------------------------------------------------------------------|
| Input voltage                | $V_{IH}$ | 2.0  | —     | —    | V    |                                                                         |
|                              | $V_{IL}$ | —    | —     | 0.8  | V    |                                                                         |
| Output voltage               | $V_{OH}$ | 2.7  | —     | —    | V    | $V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -400$ μA |
|                              | $V_{OL}$ | —    | —     | 0.4  | V    | $I_{OL} = 4$ mA, $V_{CC} = 4.75$ V, $V_{IH} = 2$ V,                     |
|                              |          | —    | —     | 0.5  |      | $I_{OL} = 8$ mA, $V_{IL} = 0.8$ V                                       |
| Input current                | $I_{IH}$ | —    | —     | 20   | μA   | $V_{CC} = 5.25$ V, $V_I = 2.7$ V                                        |
|                              | $I_{IL}$ | —    | —     | -0.4 | mA   | $V_{CC} = 5.25$ V, $V_I = 0.4$ V                                        |
|                              | $I_I$    | —    | —     | 0.1  | mA   | $V_{CC} = 5.25$ V, $V_I = 7$ V                                          |
| Short-circuit output current | $I_{OS}$ | -20  | —     | -100 | mA   | $V_{CC} = 5.25$ V                                                       |
| Supply current**             | $I_{CC}$ | —    | 13    | 21   | mA   | $V_{CC} = 5.25$ V                                                       |
| Input clamp voltage          | $V_{IK}$ | —    | —     | -1.5 | V    | $V_{CC} = 4.75$ V, $I_{IN} = -18$ mA                                    |

Notes: \*  $V_{CC} = 5$  V,  $T_a = 25$  °C

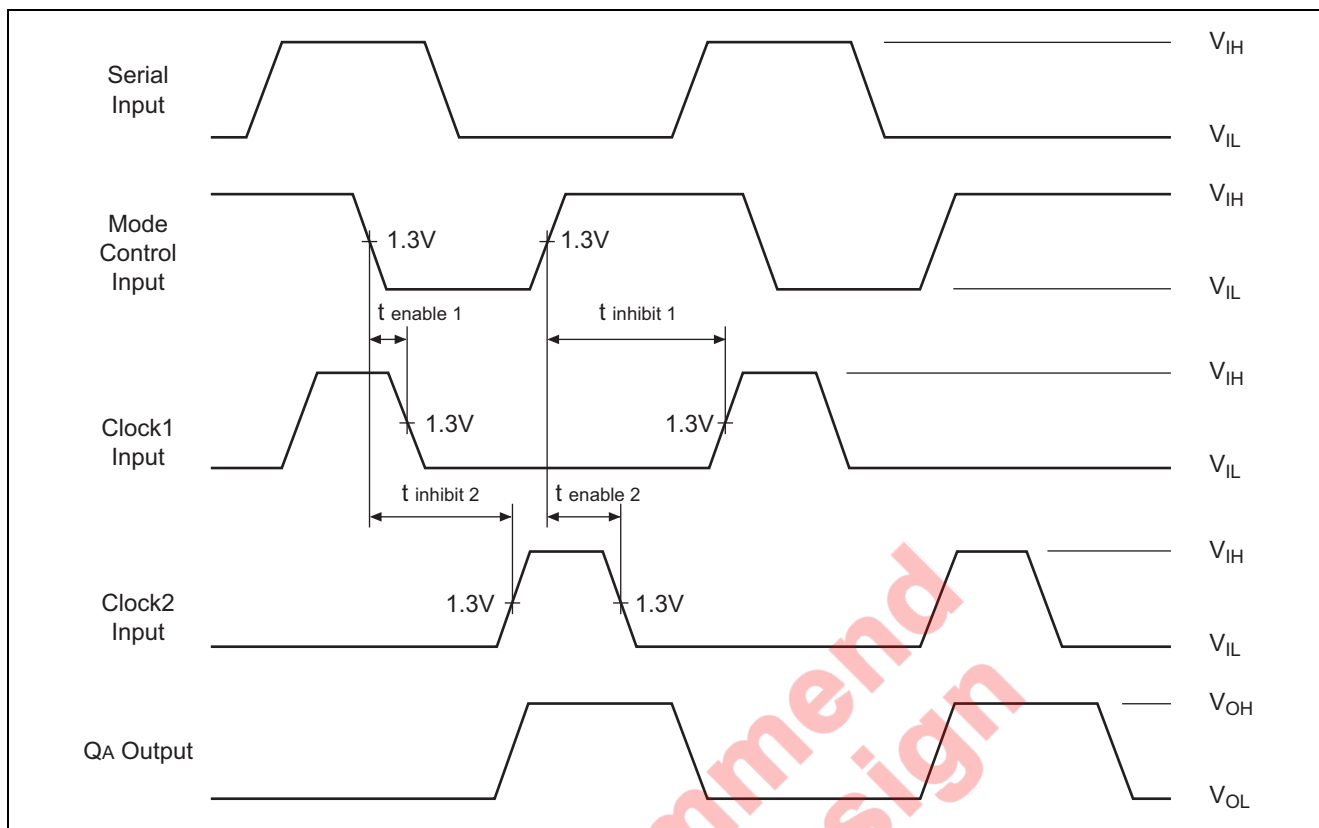
\*\*  $I_{CC}$  is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and momentary 3 V, then ground, applied both clock inputs.

## Switching Characteristics

( $V_{CC} = 5$  V,  $T_a = 25$  °C)

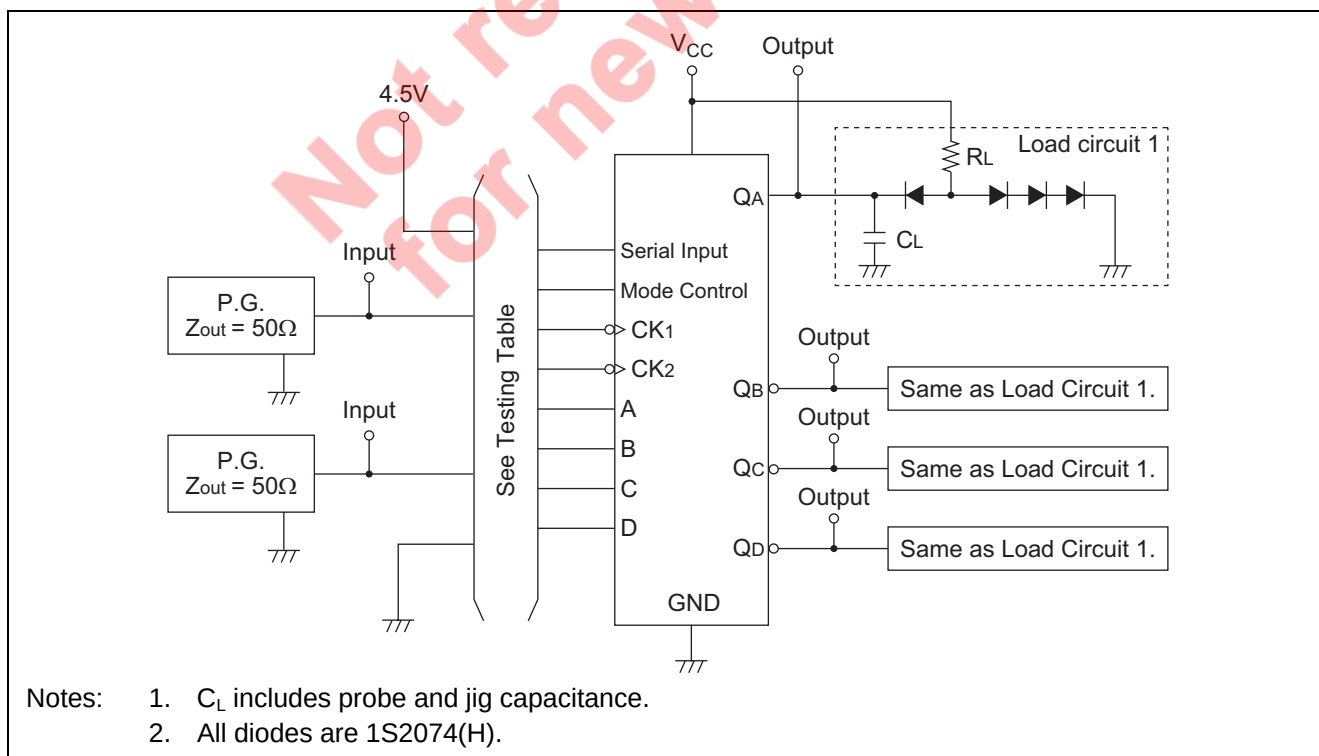
| Item                    | Symbol    | min. | typ. | max. | Unit | Condition                   |
|-------------------------|-----------|------|------|------|------|-----------------------------|
| Maximum clock frequency | $f_{max}$ | 25   | 36   | —    | MHz  | $C_L = 15$ pF, $R_L = 2$ kΩ |
| Propagation delay time  | $t_{PLH}$ | —    | 18   | 27   | ns   |                             |
|                         | $t_{PHL}$ | —    | 21   | 32   | ns   |                             |

## Clock Enable / Inhibit Times



## Testing Method

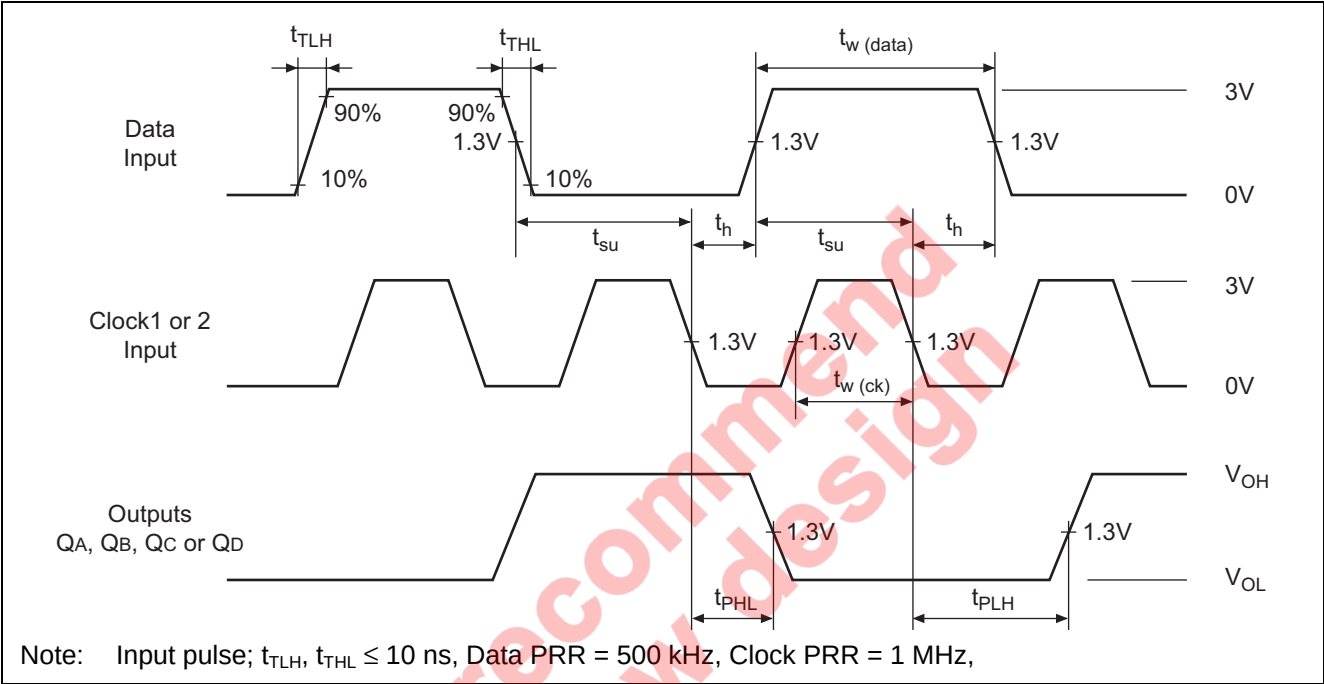
### Test Circuit



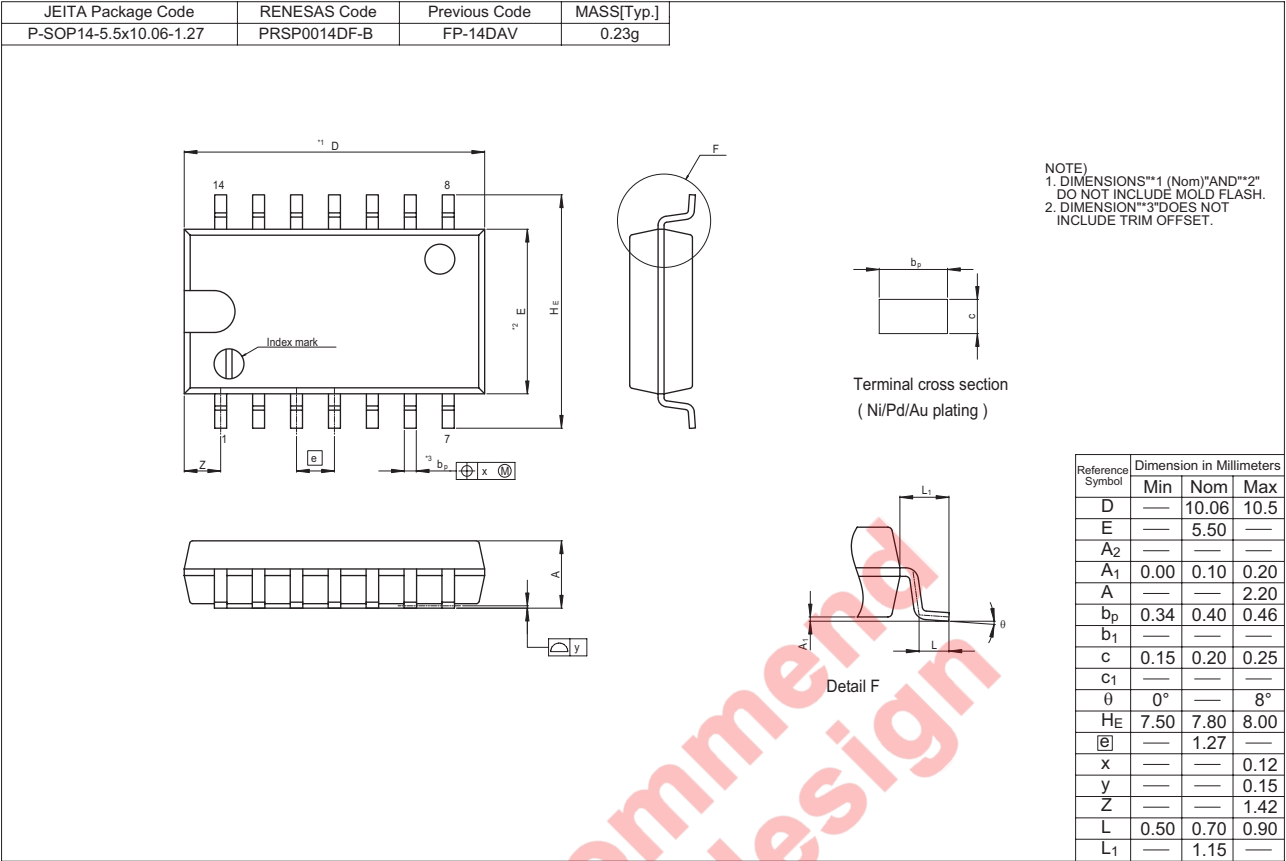
Testing Table

| Item                                 | From input to output | Inputs |       |              |               |       |       |       |       | Outputs        |                |                |                |
|--------------------------------------|----------------------|--------|-------|--------------|---------------|-------|-------|-------|-------|----------------|----------------|----------------|----------------|
|                                      |                      | CK-1   | CK-2  | Mode control | Serial Inputs | A     | B     | C     | D     | Q <sub>A</sub> | Q <sub>B</sub> | Q <sub>C</sub> | Q <sub>D</sub> |
| f <sub>max</sub>                     | CK-1 → Q             | IN     | 4.5 V | 0 V          | IN            | 4.5 V | 4.5 V | 4.5 V | 4.5 V | OUT            | OUT            | OUT            | OUT            |
|                                      | CK-2 → Q             | 4.5 V  | IN    | 4.5 V        | 4.5 V         | IN    | IN    | IN    | IN    | OUT            | OUT            | OUT            | OUT            |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | CK-1 → Q             | IN     | 4.5 V | 0 V          | IN            | 4.5 V | 4.5 V | 4.5 V | 4.5 V | OUT            | OUT            | OUT            | OUT            |
|                                      | CK-2 → Q             | 4.5 V  | IN    | 4.5 V        | 4.5 V         | IN    | IN    | IN    | IN    | OUT            | OUT            | OUT            | OUT            |

Waveform



Package Dimensions



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