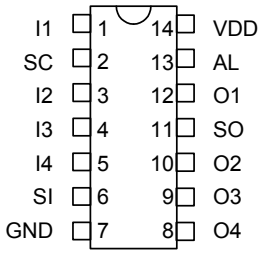
MONOLITHIC QUAD 4-BIT PROGRAMMABLE DELAY LINE (SERIES 3D7424)

FEATURES

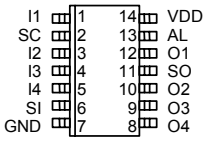
- Four indep't programmable lines on a single chip
- All-silicon CMOS technology
- Low quiescent current (5mA typical)
- Leading- and trailing-edge accuracy
- Vapor phase, IR and wave solderable
- **Increment range:** 0.75ns through 400ns
- **Delay tolerance:** 3% or 2ns (see Table 1)
- **Line-to-line matching:** 1% or 1ns typical
- **Temperature stability:** ±1.5% typical (-40C to 85C)
- **Vdd stability:** ±0.5% typical (4.75V to 5.25V)
- **Minimum input pulse width:** 10% of total delay

RoHS Compliant

PACKAGES



DIP-14
3D7424-xx



SOIC-14
3D7424D-xx

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7424 device is a small, versatile, quad 4-bit programmable monolithic delay line. Delay values, programmed via the serial interface, can be independently varied over 15 equal steps. The step size (in ns) is determined by the device dash number. Each input is reproduced at the corresponding output without inversion, shifted in time as per user selection. For each line, the delay time is given by:

$$TD_n = T0 + A_n * TI$$

where T0 is the inherent delay, A_n is the delay address of the n-th line and TI is the delay increment (dash number). The desired addresses are shifted into the device via the SC and SI inputs, and the addresses are latched using the AL input. The serial interface can also be used to enable/disable each delay line. The 3D7424 operates at 5 volts and has a typical T0 of 6ns. The 3D7424 is TTL/CMOS-compatible, capable of sourcing or sinking 4mA loads, and features both rising- and falling-edge accuracy. The device is offered in a standard 14-pin auto-insertable DIP and a space saving surface mount 14-pin SOIC.

PIN DESCRIPTIONS

I1-I4	Signal Inputs
O1-O4	Signal Outputs
AL	Address Latch In
SC	Serial Clock In
SI	Serial Data In
SO	Serial Data Out
VDD	5.0V
GND	Ground

TABLE 1: PART NUMBER SPECIFICATIONS

	DELAYS & TOLERANCES (NS)				INPUT RESTRICTIONS			
Part Number	Delay Step	Inherent Delay	Total Delay	Relative Tolerance	Max Frequency		Min Pulse Width	
					Recom'd	Absolute	Recom'd	Absolute
3D7424-.75	.75 ± 0.19	6.0 ± 2.0	17.25 ± 2.0	3% or 0.50ns	19 MHz	166 MHz	26 ns	3.0 ns
3D7424-1	1.0 ± 0.25	6.0 ± 2.0	21.0 ± 2.0	3% or 0.50ns	16 MHz	166 MHz	32 ns	3.0 ns
3D7424-1.5	1.5 ± 0.38	6.0 ± 2.0	28.5 ± 2.0	3% or 0.50ns	12 MHz	111 MHz	43 ns	4.5 ns
3D7424-2	2.0 ± 0.50	6.0 ± 2.0	36.0 ± 2.0	3% or 0.75ns	9.2 MHz	83 MHz	54 ns	6.0 ns
3D7424-4	4.0 ± 1.00	6.0 ± 2.0	66.0 ± 2.0	3% or 0.75ns	5.0 MHz	83 MHz	99 ns	6.0 ns
3D7424-5	5.0 ± 1.25	6.0 ± 2.0	81.0 ± 2.5	3% or 0.75ns	4.1 MHz	66 MHz	122 ns	7.5 ns
3D7424-10	10 ± 2.50	6.0 ± 2.0	156 ± 5.0	3% or 1.25ns	2.1 MHz	33 MHz	234 ns	15.0 ns
3D7424-15	15 ± 3.75	6.0 ± 2.0	231 ± 7.5	3% or 1.88ns	1.4 MHz	22 MHz	347 ns	22.5 ns
3D7424-20	20 ± 5.00	6.0 ± 2.0	306 ± 10	3% or 2.50ns	1.0 MHz	16 MHz	459 ns	30.0 ns
3D7424-40	40 ± 10.0	6.0 ± 2.0	606 ± 20	3% or 5.00ns	550 KHz	8.3 MHz	909 ns	60.0 ns
3D7424-50	50 ± 10.0	6.0 ± 2.0	756 ± 25	3% or 6.25ns	440 KHz	6.6 MHz	1.2 us	75.0 ns
3D7424-100	100 ± 12.5	6.0 ± 2.0	1506 ± 50	3% or 12.5ns	220 KHz	3.3 MHz	2.3 us	150 ns
3D7424-200	200 ± 20.0	6.0 ± 2.0	3006 ± 100	3% or 25.0ns	110 KHz	1.6 MHz	4.5 us	300 ns
3D7424-400	400 ± 40.0	6.0 ± 2.0	6006 ± 200	3% or 50.0ns	55 KHz	833 KHz	9.0 us	600 ns

NOTE: Any increment between 0.75ns and 400ns not shown is also available as standard
See page 4 for details regarding input restrictions

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APPLICATION NOTES

THEORY OF OPERATION

The quad 4-bit programmable 3D7424 device architecture is comprised of four independently operating delay lines. Each delay line produces at its output a replica of the signal present at its input, shifted in time. A single delay line is comprised of a number of delay cells connected in series. Delay selection is achieved by routing one output in each string of cells to its respective output pin (O1-O4). The delay of each of the four lines can be controlled independently, via the serial interface, as described in the next section.

The change in delay from one address setting to the next is called the *increment*, or LSB. It is nominally equal to the device dash number. The minimum delay, achieved by setting the address of a line to zero, is called the *inherent delay*.

For best performance, it is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred. Also, signal traces should be kept as short as possible.

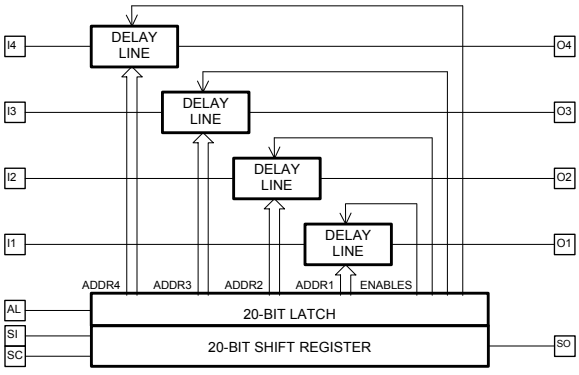


Figure 1: Functional block diagram

PROGRAMMED DELAY INTERFACE

Figure 1 illustrates the main functional blocks of the 3D7424 device. Since the device is a CMOS design, all unused input pins must be returned to well defined logic levels (VDD or GND). The delays are adjusted by first shifting a 20-bit programming word into the device via the SC and SI pins, then strobing the AL signal to latch the values. The bit sequence is shown in Table 2, and the associated timing diagram is shown in Figure 2. Each line has associated with it an enable bit. Setting this bit low will force the corresponding delay line output to a high impedance state, while setting it high returns the line to its normal operation. The device contains an SO output, which can be used to cascade multiple devices, as shown in Figure 3.

TABLE 2: BIT SEQUENCE

Bit	Delay Line	Function
1	4	Output Enable
2	3	Output Enable
3	2	Output Enable
4	1	Output Enable
5	1	Address Bit 3
6		Address Bit 2
7		Address Bit 1
8		Address Bit 0
9	2	Address Bit 3
10		Address Bit 2
11		Address Bit 1
12		Address Bit 0
13	3	Address Bit 3
14		Address Bit 2
15		Address Bit 1
16		Address Bit 0
17	4	Address Bit 3
18		Address Bit 2
19		Address Bit 1
20		Address Bit 0

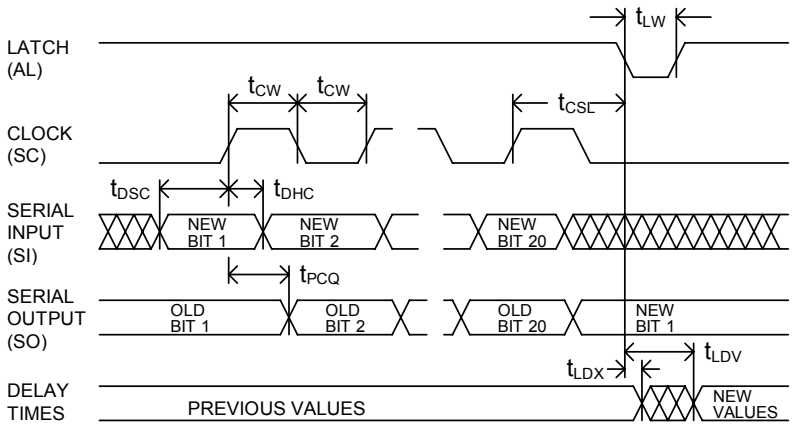


Figure 2: Serial interface timing diagram

APPLICATION NOTES (CONT'D)

DELAY ACCURACY

There are a number of ways of characterizing the delay accuracy of a programmable line. The first is the *differential nonlinearity* (DNL), also referred to as the increment error. It is defined as the deviation of the delay step at a given address from its nominal value. For all dash numbers, the DNL is within 1/4 LSB at every address (see Table 1: Delay Step).

The *integrated nonlinearity* (INL) is determined by first constructing the least-squares best fit straight line through the delay-versus-address data. The INL is then the deviation of a given delay from this line. For all dash numbers, the INL is within 1.0 LSB at every address.

The *relative error* is defined as follows:

$$e_{rel} = (T_i - T_0) - i * T_{inc}$$

where i is the address, T_i is the measured delay at the i'th address, T_0 is the measured inherent delay, and T_{inc} is the nominal increment. It is very similar to the INL, but simpler to calculate. For most dash numbers, the relative error is less than 1/8 LSB at every address (see Table 1: Relative Tolerance).

The *absolute error* is defined as follows:

$$e_{abs} = T_i - (T_{inh} + i * T_{inc})$$

where T_{inh} is the nominal inherent delay. The absolute error tolerance is given for addresses 0 and 15 (see Table 1: Inherent Delay, Total Delay, respectively). At any intermediate address, the tolerance can be found via linear interpolation of the address 0 & address 15 tolerances.

The *matching error* is a measure of how well the delay of the four lines track each other when they are all programmed to the same address. The lines are typically matched to within 1% or 1ns, whichever is greater, for all addresses and all dash numbers.

DELAY STABILITY

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The 3D7424 utilizes novel compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

With regard to stability, the delay of the 3D7424 at a given address, i, can be split into two components: the *inherent delay* (T_0) and the *relative delay* ($T_i - T_0$). These components exhibit very different stability coefficients, both of which must be considered in very critical applications.

The thermal coefficient of the relative delay is limited to ±250 PPM/C, which is equivalent to a variation, over the -40C to 85C operating range, of ±1.5% from the room-temperature delay settings. This holds for dash numbers greater than 1. For smaller dash numbers, the thermal drift will be larger and will always be positive. The thermal coefficient of the inherent delay is nominally +15ps/C for all dash numbers.

The power supply sensitivity of the relative delay is ±0.5% over the 4.75V to 5.25V operating range, with respect to the delay settings at the nominal 5.0V power supply. This holds for all dash numbers greater than 1. For smaller dash numbers, the voltage sensitivity will be greater and will always be negative. The sensitivity of the inherent delay is nominally -1ps/mV for all dash numbers.

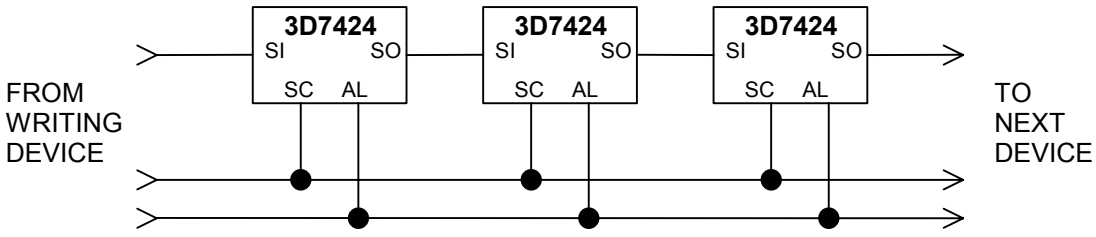


Figure 3: Cascading Multiple Devices

APPLICATION NOTES (CONT'D)

INPUT SIGNAL CONSIDERATIONS

The frequency and/or pulse width (high or low) of operation may adversely impact the specified delay and increment accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore, a recommended and an absolute maximum operating input frequency and a recommended and an absolute minimum operating pulse width have been specified.

OPERATING FREQUENCY

The absolute maximum operating frequency specification, tabulated in Table 1, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle distortion.

The recommended maximum operating frequency specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed. Operation above the recommended maximum frequency will cause the delays to shift slighty with respect to their values at low-frequency operation. The magnitudes of these deviations will increase as the absolute maximum frequency is approached. However, if the input frequency and pulse width remain constant, the device will exhibit the same delays from one period to the next (ie, no appreciable jitter).

OPERATING PULSE WIDTH

The absolute minimum operating pulse width (high or low) specification, tabulated in Table 1, determines the smallest pulse width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion.

The minimum operating pulse width (high or low) specification determines the smallest pulse width of the delay line input signal for which the output delay accuracy tabulated in Table 1 is guaranteed.

Operation below the recommended minimum pulse width will cause the delays to shift slighty with respect to their values at long-pulse-width operation. The magnitudes of these deviations will increase as the absolute minimum pulse width is approached. However, if the input pulse width and frequency remain constant, the device will exhibit the same delays from one period to the next (ie, no appreciable jitter).

PROGRAMMED DELAY UPDATE

A delay line is a memory device. It stores information present at the input for a time equal to the delay setting before presenting it at the output. Each 4-bit delay line in the 3D7424 is represented by 15 serially connected delay elements (individually addressed by the programming data), each capable of storing data for a time equal to the device increment (step time). The delay line memory property, in conjunction with the operational requirement of "instantaneously" connecting the delay element addressed by the programming data to the output, may inject spurious information onto the output data stream. In order to ensure that spurious outputs do not occur, it is essential that the input signal be idle (held high or low) for a short duration prior to updating the programmed delay. This duration is given by the maximum programmable delay. Satisfying this requirement allows the delay line to "clear" itself of spurious edges. Once the new address is loaded, the input signal can begin to switch.

DEVICE SPECIFICATIONS

TABLE 3: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 4: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		5.0	7.0	mA	V_{DD} = 5.25V
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}	-0.1	0.0	0.1	µA	V_{IH} = V_{DD}
Low Level Input Current	I_{IL}	-0.1	0.0	0.1	µA	V_{IL} = 0V
High Level Output Current	I_{OH}		-8.0	-6.0	mA	V_{DD} = 4.75V V_{OH} = 2.4V
Low Level Output Current	I_{OL}	6.0	7.5		mA	V_{DD} = 4.75V V_{OL} = 0.4V
Output Rise & Fall Time	T_R & T_F		2		ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 4 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/line (pf)
F = Input frequency (GHz)

Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 5: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Latch Width	T_{LW}	10			ns	
Data Setup to Clock	t_{DSC}	10			ns	
Data Hold from Clock	t_{DHC}	1			ns	
Clock Width (High or Low)	t_{CW}	15			ns	
Clock Setup to Latch	t_{CSL}	20			ns	
Clock to Serial Output	t_{PCQ}		12	20	ns	
Latch to Delay Valid	t_{LDV}		35	45	ns	**1**
Latch to Delay Invalid	t_{LDX}	5			ns	**1**
Input Pulse Width	t_{WI}	10			% of Total Delay	See Table 1
Input Period	Period	20			% of Total Delay	See Table 1
Input to Output Delay	t_{PLH}, t_{PHL}				ns	See Text

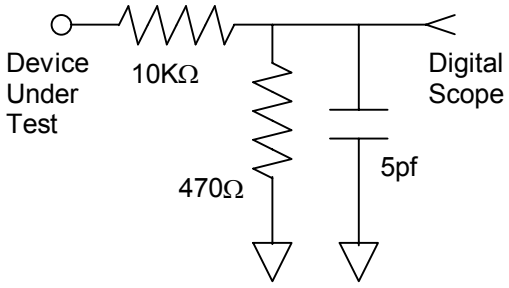
NOTES: 1 - Refer to **PROGRAMMED DELAY UPDATE** section

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (VDD): 5.0V ± 0.1V
Input Pulse: High = 3.3V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.7V)
Pulse Width: PW_{IN} = 1.25 x Total Delay
Period: PER_{IN} = 2.5 x Total Delay

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.65V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

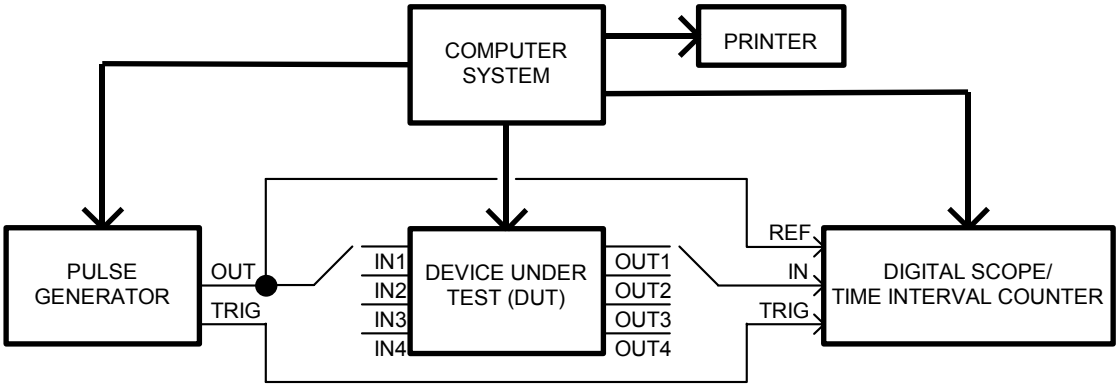


Figure 4: Test Setup

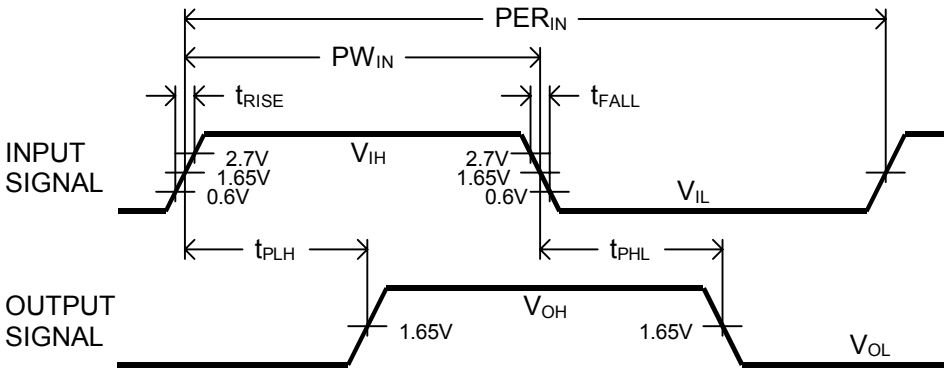


Figure 5: Timing Diagram