Arm® Cortex®-M

32-bit Microcontroller

NuMicro® Family
NUC131LD2AEU
Datasheet

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1 GENERAL DESCRIPTION

The NUC131LD2AEU is a 32-bit ARM® Cortex®-M0 based microcontroller running up to 50 MHz with built-in Controller Area Network (CAN) 2.0 B interface, qualified by AEC-Q100 grade 2, designed for automotive, industrial control applications which needs reliable and robust CAN communication.

The NUC131LD2AEU features 68 KB Flash, 8 KB SRAM, and 4 KB ISP ROM, operating voltage from 2.5 V to 5.5 V and temperature range from -40 °C to 105 °C. In addition to the CAN interface, it is equipped with plenty of peripheral devices, such as 6 set of UARTs, 2 set of I^2C, 1 set SPI, 24 channels of 100 MHz high resolution PWMs with brake function and complimentary output to drive both stepping motor or HVAC compresser; 760 kSPS 12-bit ADC to sample different kind of data from sensors.

2 FEATURES

- Arm® Cortex®-M0 core
  - Runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 68 KB Flash for program code
  - Configurable Flash memory for data memory (Data Flash), 4 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 8 KB embedded SRAM
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 °C and V_{DD} = 5 V
    - Trimmed to ±2 % at -40 °C ~ +105 °C and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL output frequency up to 200 MHz, BPWM/PWM clock frequency up to 100 MHz, and System operation frequency up to 50 MHz
  - External 4~24 MHz high speed crystal input for precise timing operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- Watchdog Timer
  - Multiple clock sources
    - System clock (HCLK)
    - Internal 10 kHz oscillator (LIRC)
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- BPWM/Capture
  - Supports maximum clock frequency up to 100 MHz
  - Supports up to two BPWM modules, each module provides one 16-bit timer and 6 output

channels
  - Supports independent mode for BPWM output/Capture input channel
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution BPWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each BPWM pin
  - Supports interrupt on the following events:
    - BPWM counter match zero, period value or compared value
  - Supports trigger ADC on the following events:
    - BPWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- PWM/Capture
  - Supports maximum clock frequency up to 100 MHz
  - Supports up to two PWM modules, each module provides three 16-bit timers and 6 output channels
  - Supports independent mode for PWM output/Capture input channel
  - Supports complementary mode for 3 complementary paired PWM output channel
    - Dead-time insertion with 12-bit resolution
    - Two compared values during one period
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution PWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each PWM pin
  - Supports brake function
    - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
    - Noise filter for brake source from pin
    - Edge detect brake source to control brake state until brake interrupt cleared
    - Level detect brake source to auto recover function after brake condition removed
  - Supports interrupt on the following events:
    - PWM counter match zero, period value or compared value
    - Brake condition happened
  - Supports trigger ADC on the following events:
    - PWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- UART
  - Up to six UART controllers
  - UART0 and UART1 ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0, UART1 and UART2 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Supports auto baud-rate generator
- SPI
  - One set of SPI controller
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently

  - Supports Byte Suspend mode in 32-bit transmission
  - Supports three wire, no slave select signal, bi-direction interface
- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- CAN 2.0
  - One set of CAN device
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1 Mbit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Support power-down wake-up function
- ADC
  - 12-bit SAR ADC with 760 kSPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming or external input
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- Brown-out Detector
  - With 4 levels: 4.4 V / 3.7 V / 2.7 V / 2.2 V
  - Supports Brown-out Interrupt and Reset option.
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40°C ~ +105°C
- AEC-Q100 Grade 2 Qualified.
- Packages:
  - All Green package (RoHS)
  - LQFP 48-pin (7mm x 7mm)

3 ABBREVIATIONS

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
BPWM	Basic Pulse Width Modulation
CAN	Controller Area Network
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® NUC131LD2AEU Features and Peripherals

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity					PWM (16-Bit)	ADC (12-Bit)	ISP/ICP/IAP	AEC-Q100	Package
							UART	SPI	I^2C	LIN	CAN					
NUC131LD2AEU	68	8	Configurable	4	42	4	6	1	2	3	1	24	8 ch	√	√	LQFP48

4.2 Pin Configuration

4.2.1 NuMicro® NUC131LD2AEU Pin Diagram

4.2.1.1 NuMicro® NUC131LD2AEU LQFP 48 pin

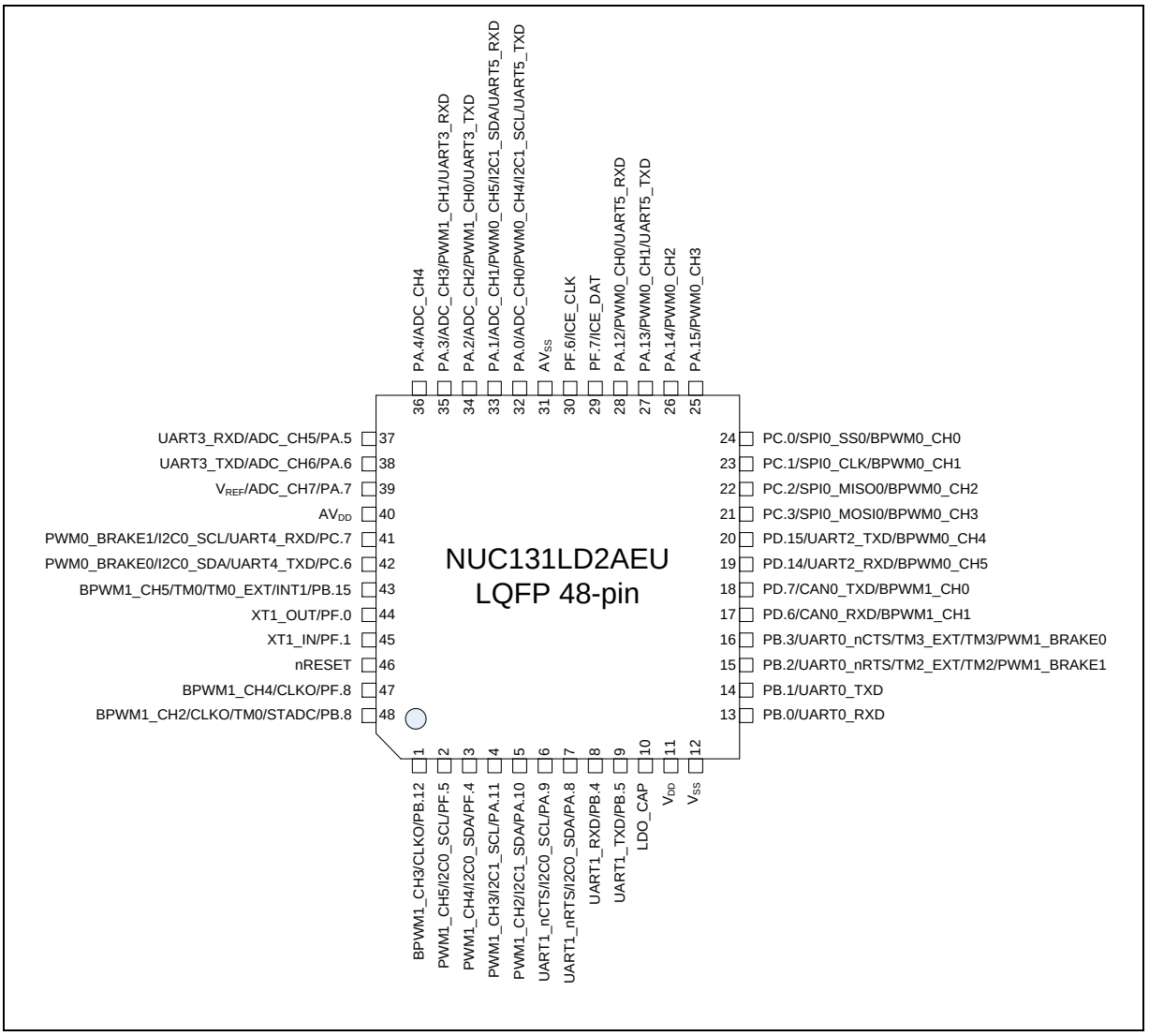


Figure 4.2-1 NuMicro® NUC131LD2AEU LQFP 48-pin Diagram

4.3 Pin Description

4.3.1 NuMicro® NUC131LD2AEU Pin Description

Pin No. LQFP 48-pin	Pin Name	Pin Type	Description
1	PB.12	**I/O**	General purpose digital I/O pin.
	CLKO	**O**	Frequency divider clock output pin.
	BPWM1_CH3	**I/O**	BPWM1 CH3 output/Capture input.
2	PF.5	**I/O**	General purpose digital I/O pin.
	I2C0_SCL	**I/O**	I^2C0 clock pin.
	PWM1_CH5	**I/O**	PWM1 CH5 output/Capture input.
3	PF.4	**I/O**	General purpose digital I/O pin.
	I2C0_SDA	**I/O**	I^2C0 data input/output pin.
	PWM1_CH4	**I/O**	PWM1 CH4 output/Capture input.
4	PA.11	**I/O**	General purpose digital I/O pin.
	I2C1_SCL	**I/O**	I^2C1 clock pin.
	PWM1_CH3	**I/O**	PWM1 CH3 output/Capture input.
5	PA.10	**I/O**	General purpose digital I/O pin.
	I2C1_SDA	**I/O**	I^2C1 data input/output pin.
	PWM1_CH2	**I/O**	PWM1 CH2 output/Capture input.
6	PA.9	**I/O**	General purpose digital I/O pin.
	I2C0_SCL	**I/O**	I^2C0 clock pin.
	UART1_nCTS	**I**	Clear to Send input pin for UART1.
7	PA.8	**I/O**	General purpose digital I/O pin.
	I2C0_SDA	**I/O**	I^2C0 data input/output pin.
	UART1_nRTS	**O**	Request to Send output pin for UART1.
8	PB.4	**I/O**	General purpose digital I/O pin.
	UART1_RXD	**I**	Data receiver input pin for UART1.
9	PB.5	**I/O**	General purpose digital I/O pin.
	UART1_TXD	**O**	Data transmitter output pin for UART1.
10	LDO_CAP	**P**	LDO output pin.
11	V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
12	V_{SS}	**P**	Ground pin for digital circuit.
13	PB.0	**I/O**	General purpose digital I/O pin.

Pin No. LQFP 48-pin	Pin Name	Pin Type	Description
	UART0_RXD	I	Data receiver input pin for UART0.
14	PB.1	I/O	General purpose digital I/O pin.
	UART0_TXD	O	Data transmitter output pin for UART0.
15	PB.2	I/O	General purpose digital I/O pin.
	UART0_nRTS	O	Request to Send output pin for UART0.
	TM2_EXT	I	Timer2 external capture input pin.
	TM2	O	Timer2 toggle output pin.
	PWM1_BRAKE1	I	PWM1 brake input pin.
16	PB.3	I/O	General purpose digital I/O pin.
	UART0_nCTS	I	Clear to Send input pin for UART0.
	TM3_EXT	I	Timer3 external capture input pin.
	TM3	O	Timer3 toggle output pin.
	PWM1_BRAKE0	I	PWM1 brake input pin.
17	PD.6	I/O	General purpose digital I/O pin.
	CAN0_RXD	I	Data receiver input pin for CAN0.
	BPWM1_CH1	I/O	BPWM1 CH1 output/Capture input.
18	PD.7	I/O	General purpose digital I/O pin.
	CAN0_TXD	O	Data transmitter output pin for CAN0.
	BPWM1_CH0	I/O	BPWM1 CH0 output/Capture input.
19	PD.14	I/O	General purpose digital I/O pin.
	UART2_RXD	I	Data receiver input pin for UART2.
	BPWM0_CH5	I/O	BPWM0 CH5 output/Capture input.
20	PD.15	I/O	General purpose digital I/O pin.
	UART2_TXD	O	Data transmitter output pin for UART2.
	BPWM0_CH4	I/O	BPWM0 CH4 input/Capture input.
21	PC.3	I/O	General purpose digital I/O pin.
	SPI0_MOSI0	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	BPWM0_CH3	O	BPWM0 CH3 input/Capture input.
22	PC.2	I/O	General purpose digital I/O pin.
	SPI0_MISO0	I/O	SPI0 MISO (Master In, Slave Out) pin.
	BPWM0_CH2	I	BPWM0 CH2 input/Capture input.

Pin No. LQFP 48-pin	Pin Name	Pin Type	Description
23	PC.1	**I/O**	General purpose digital I/O pin.
	SPI0_CLK	**I/O**	SPI0 serial clock pin.
	BPWM0_CH1	**I/O**	BPWM0 CH1 input/Capture input.
24	PC.0	**I/O**	General purpose digital I/O pin.
	SPI0_SS0	**I/O**	SPI0 slave select pin.
	BPWM0_CH0	**I/O**	BPWM0 CH0 input/Capture input.
25	PA.15	**I/O**	General purpose digital I/O pin.
	PWM0_CH3	**I/O**	PWM0 CH3 output/Capture input.
26	PA.14	**I/O**	General purpose digital I/O pin.
	PWM0_CH2	**I/O**	PWM0 CH2 output/Capture input.
27	PA.13	**I/O**	General purpose digital I/O pin.
	PWM0_CH1	**I/O**	PWM0 CH1 output/Capture input.
	UART5_TXD	**O**	Data transmitter output pin for UART5.
28	PA.12	**I/O**	General purpose digital I/O pin.
	PWM0_CH0	**I/O**	PWM0 CH0 output/Capture input.
	UART5_RXD	**I**	Data receiver input pin for UART5.
29	PF.7	**I/O**	General purpose digital I/O pin.
	ICE_DAT	**I/O**	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
30	PF.6	**I/O**	General purpose digital I/O pin.
	ICE_CLK	**I**	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
31	AV_{SS}	**AP**	Ground pin for analog circuit.
32	PA.0	**I/O**	General purpose digital I/O pin.
	ADC_CH0	**AI**	ADC_CH0 analog input.
	PWM0_CH4	**I/O**	PWM0 CH4 output/Capture input.
	I2C1_SCL	**I/O**	I^2C1 clock pin.
	UART5_TXD	**O**	Data transmitter output pin for UART5.
33	PA.1	**I/O**	General purpose digital I/O pin.
	ADC_CH1	**AI**	ADC_CH1 analog input.
	PWM0_CH5	**I/O**	PWM0 CH5 output/Capture input.
	I2C1_SDA	**I/O**	I^2C1 data input/output pin.

Pin No. LQFP 48-pin	Pin Name	Pin Type	Description
	UART5_RXD	I	Data receiver input pin for UART5.
34	PA.2	I/O	General purpose digital I/O pin.
	ADC_CH2	AI	ADC_CH2 analog input.
	PWM1_CH0	I/O	PWM1 CH0 output/Capture input.
	UART3_TXD	O	Data transmitter output pin for UART3.
35	PA.3	I/O	General purpose digital I/O pin.
	ADC_CH3	AI	ADC_CH3 analog input.
	PWM1_CH1	I/O	PWM1 CH1 output/Capture input.
	UART3_RXD	I	Data receiver input pin for UART3.
36	PA.4	I/O	General purpose digital I/O pin.
	ADC_CH4	AI	ADC_CH4 analog input.
37	PA.5	I/O	General purpose digital I/O pin.
	ADC_CH5	AI	ADC_CH5 analog input.
	UART3_RXD	I	Data receiver input pin for UART3.
38	PA.6	I/O	General purpose digital I/O pin.
	ADC_CH6	AI	ADC_CH6 analog input.
	UART3_TXD	O	Data transmitter output pin for UART3.
39	PA.7	I/O	General purpose digital I/O pin.
	ADC_CH7	AI	ADC_CH7 analog input.
	V_{REF}	AP	Voltage reference input for ADC.
40	AV_{DD}	AP	Power supply for internal analog circuit.
41	PC.7	I/O	General purpose digital I/O pin.
	UART4_RXD	I	Data reveiver input pin for UART4.
	I2C0_SCL	I/O	I^2C0 clock pin.
	PWM0_BRAKE1	I	PWM0 brake input pin.
42	PC.6	I/O	General purpose digital I/O pin.
	UART4_TXD	O	Data transmitter output pin for UART4.
	I2C0_SDA	I/O	I^2C0 data input/output pin.
	PWM0_BRAKE0	I	PWM0 brake input pin.
43	PB.15	I/O	General purpose digital I/O pin.
	INT1	I	External interrupt1 input pin.
	TM0_EXT	I	Timer0 external capture input pin.

Pin No. LQFP 48-pin	Pin Name	Pin Type	Description
	TM0	**O**	Timer0 toggle output pin.
	BPWM1_CH5	**I/O**	BPWM1 CH5 output/Capture input.
44	PF.0	**I/O**	General purpose digital I/O pin.
	XT1_OUT	**O**	External 4~24 MHz (high speed) crystal output pin.
45	PF.1	**I/O**	General purpose digital I/O pin.
	XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
46	nRESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
47	PF.8	**I/O**	General purpose digital I/O pin.
	CLKO	**O**	Frequency divider clock output pin.
	BPWM1_CH4	**I/O**	BPWM1 CH4 output/Capture input.
48	PB.8	**I/O**	General purpose digital I/O pin.
	STADC	**I**	ADC external trigger input.
	TM0	**I/O**	Timer0 event counter input / toggle output.
	CLKO	**O**	Frequency divider clock output pin.
	BPWM1_CH2	**I/O**	BPWM1 CH2 output/Capture input.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

5.1 NuMicro® NUC131LD2AEU Block Diagram

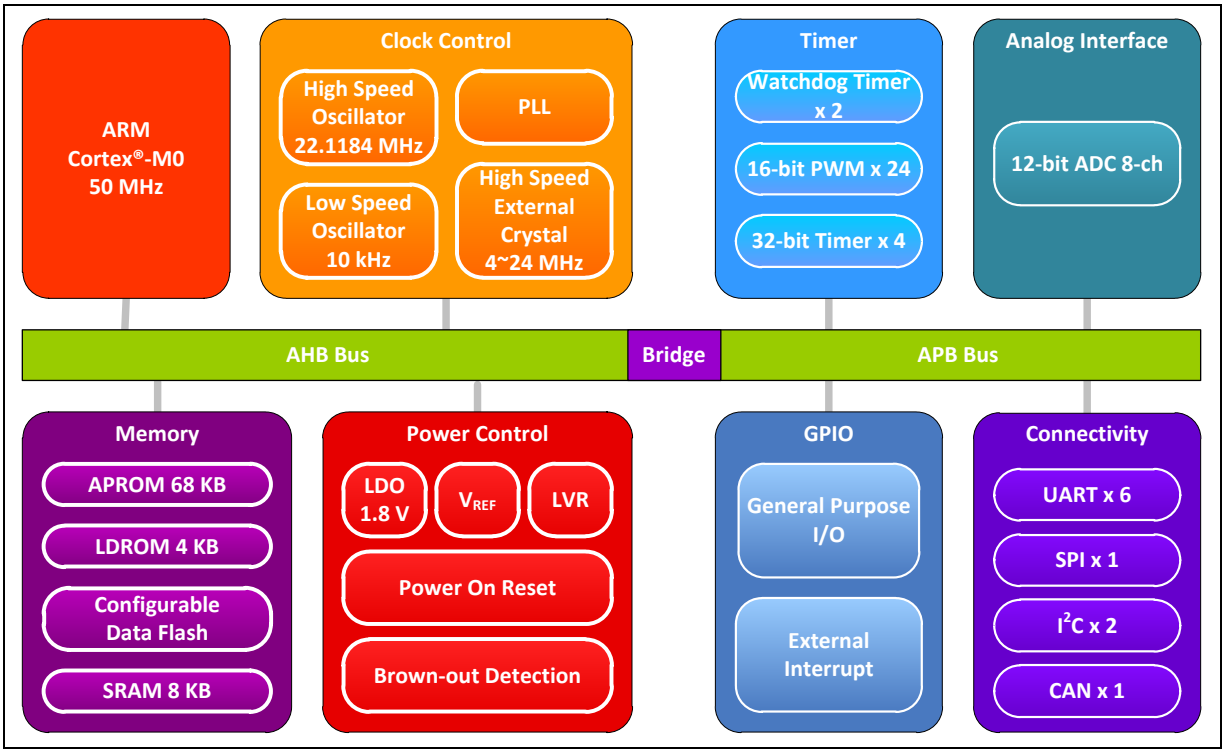


Figure 5.1-1 NuMicro® NUC131LD2AEU Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

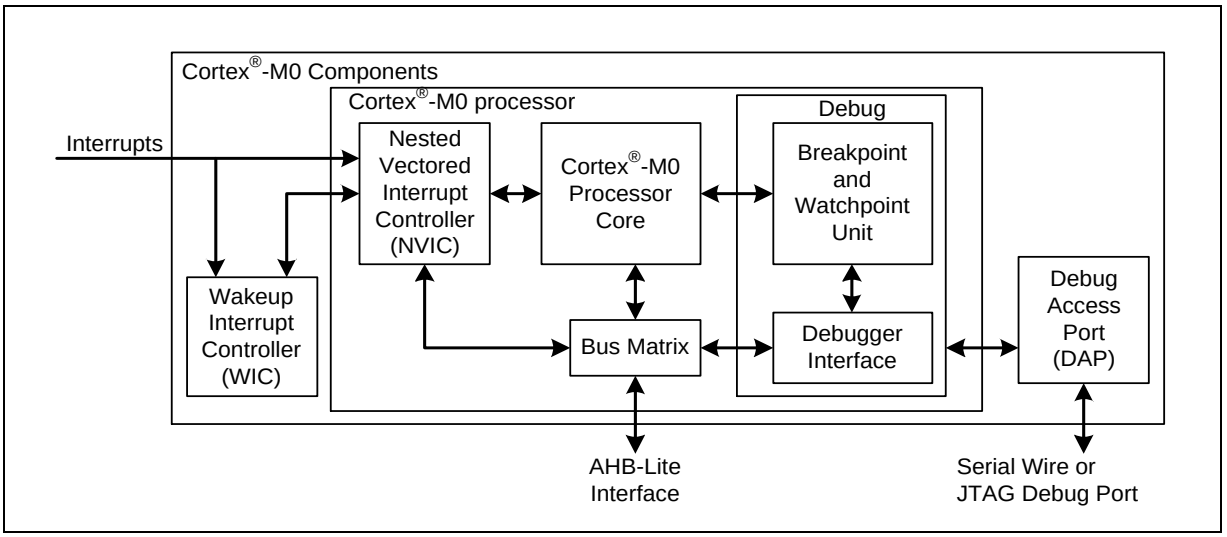


Figure 6.1-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Power-on Reset
- Low level on the nRESET pin
- Watchdog Time-out Reset
- Low Voltage Reset
- Brown-out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-on Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-on Reset is external crystal circuit and BS (ISPCON[1]) bit. System Reset does not reset external crystal circuit and BS (ISPCON[1]) bit, but Power-on Reset does.

6.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level with the digital power (V_{DD}). Figure 6.2-1 shows the NuMicro® NUC131LD2AEU power distribution.

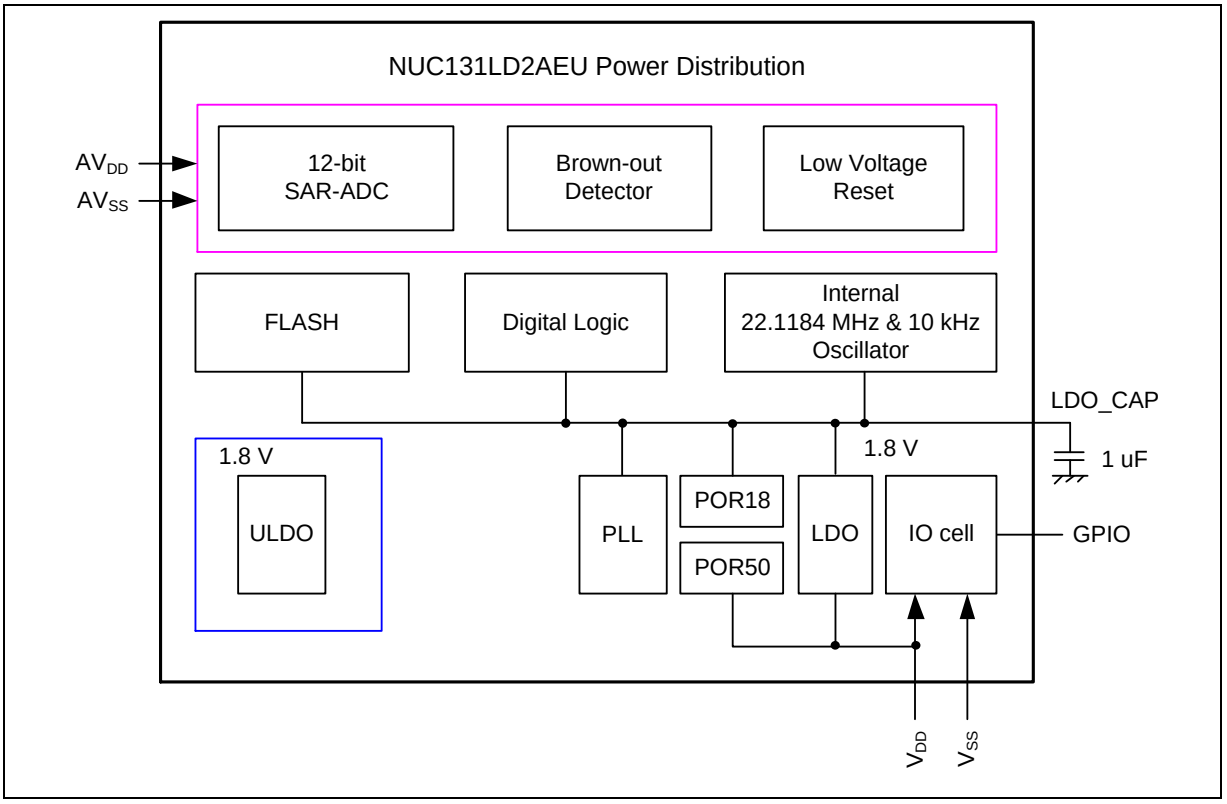


Figure 6.2-1 NuMicro® NUC131LD2AEU Power Distribution Diagram

6.2.4 System Memory Map

The NuMicro® NUC131LD2AEU provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripheral. The NuMicro® NUC131LD2AEU only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_0FFF	FLASH_BA	FLASH Memory Space (68 KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (8 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	BPWM0_BA	BPWM0 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4005_4000 – 0x4005_7FFF	UART3_BA	UART3 Control Registers
0x4005_8000 – 0x4005_BFFF	UART4_BA	UART4 Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4014_0000 – 0x4014_3FFF	PWM1_BA	PWM1 Control Registers
0x4014_4000 – 0x4014_7FFF	BPWM1_BA	BPWM1 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4015_8000 – 0x4015_BFFF	UART5_BA	UART5 Control Registers
0x4018_0000 – 0x4018_3FFF	CAN0_BA	CAN0 Bus Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		

0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-1 Address Space Assignments for On-Chip Controllers

6.2.5 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is unknown on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex€-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.6 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.6.1 Exception Model and System Interrupt Map

Table 6.2-2 and Table 6.2-3 lists the exception model supported by NuMicro® NUC131LD2AEU. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-2 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description
1 ~ 15	-	**-**	-	System exceptions
16	0	**BOD_INT**	Brown-out	Brown-out low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	**GPCDEF_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]/PE[15:0]/PF[8:0]
22	6	**-**	-	Reserved
23	7	**-**	-	Reserved
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt
28	12	**UART02_INT**	UART0/2	UART0 and UART2 interrupt
29	13	**UART1_INT**	UART1	UART1 interrupt

30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**UART3_INT**	UART3	UART3 interrupt
32	16	**UART4_INT**	UART4	UART4 interrupt
33	17	**UART5_INT**	UART5	UART5 interrupt
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**CAN0_INT**	CAN0	CAN0 interrupt
37	21	**-**	-	Reserved
38	22	**PWM0_INT**	PWM0	PWM0 interrupt
39	23	**PWM1_INT**	PWM1	PWM1 interrupt
40	24	**BPWM0_INT**	BPWM0	BPWM0 interrupt
41	25	**BPWM1_INT**	BPWM1	BPWM1 interrupt
42	26	**BRAKE0_INT**	PWM0	PWM0 brake interrupt
43	27	**BRAKE1_INT**	PWM1	PWM1 brake interrupt
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state
45	29	**ADC_INT**	ADC	ADC interrupt
46	30	**CKD_INT**	CLKC	Clock detection interrupt
47	31	**-**	-	Reserved

Table 6.2-3 System Interrupt Map

6.2.6.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6.2-4 Vector Table Format

6.2.6.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.7 System Control

The Cortex®-M0 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex®-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184 MHz internal high speed RC oscillator to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 5 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency(PLL FOUT),PLL source can be from external 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC))
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

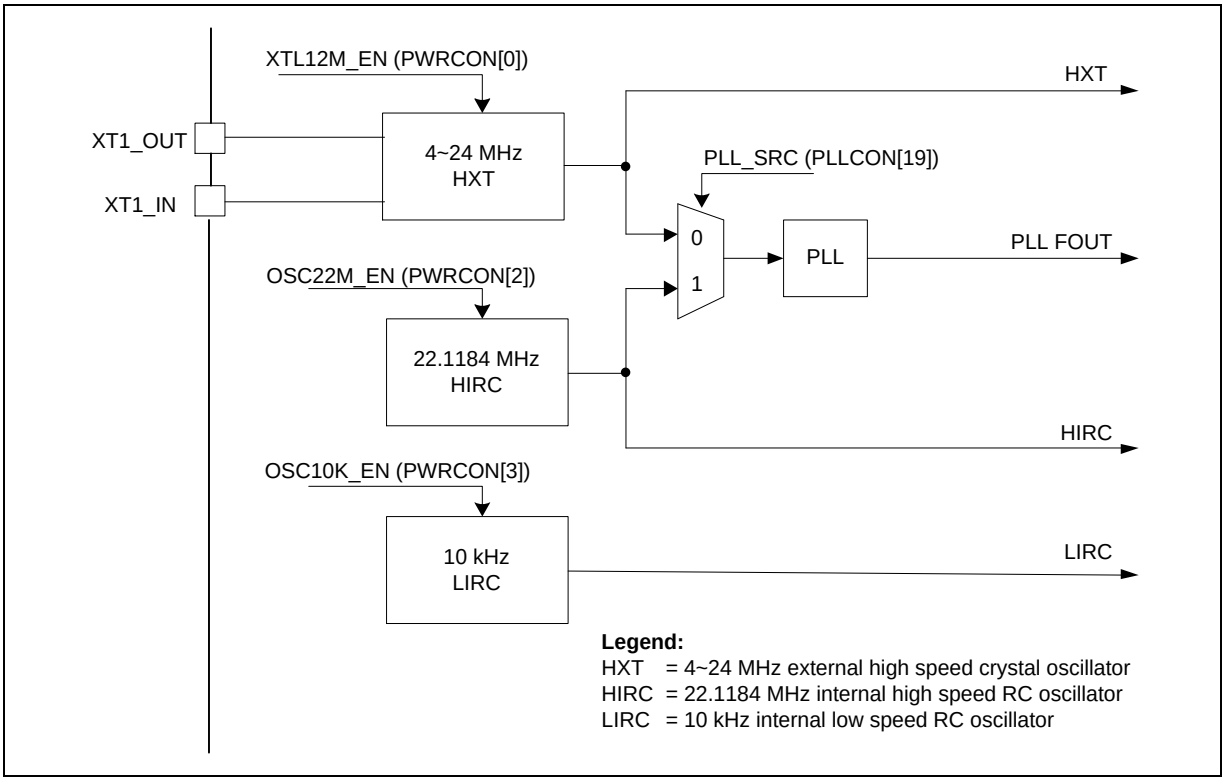


Figure 6.3-1 Clock Generator Block Diagram

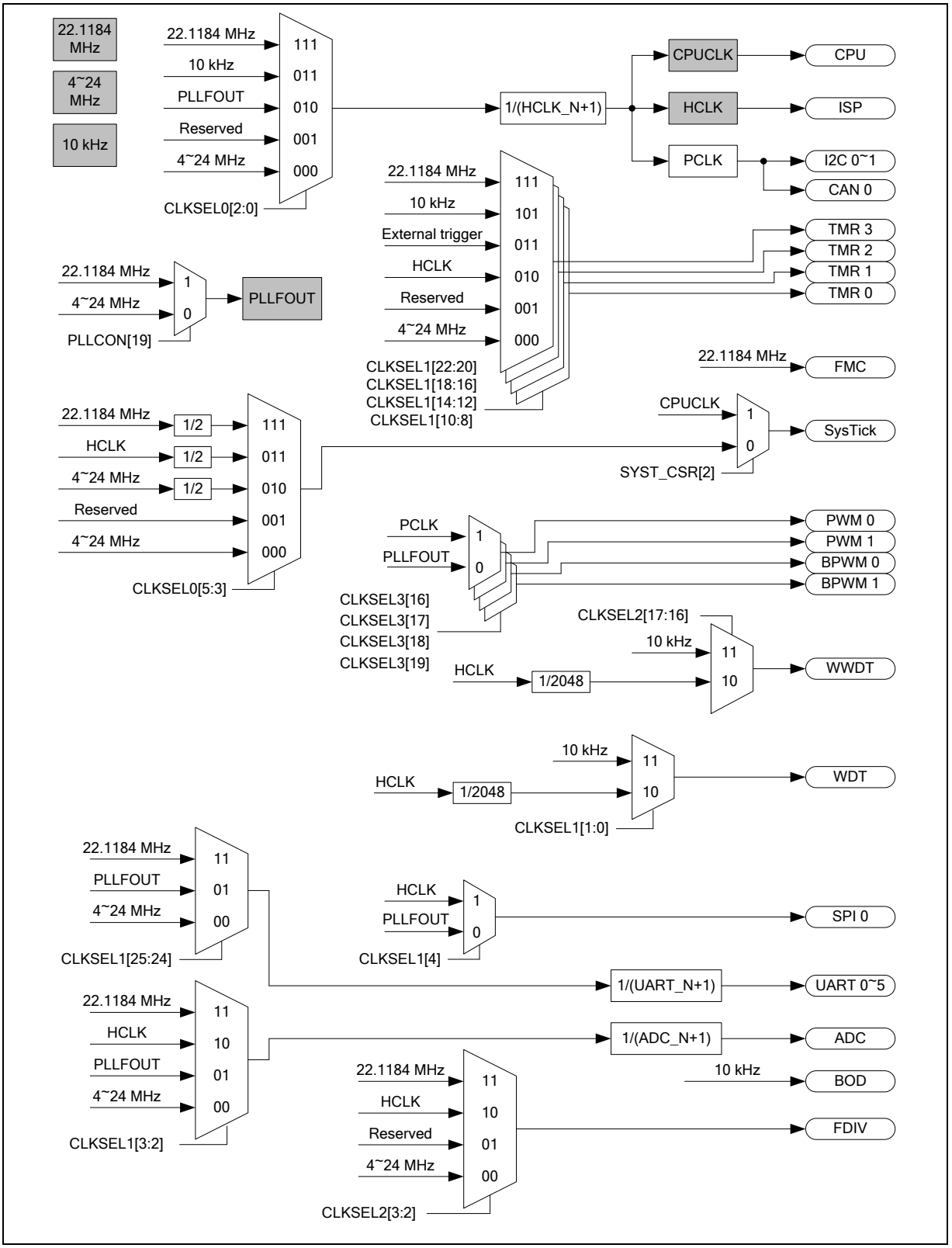


Figure 6.3-2 Clock Generator Global View Diagram

6.3.2 System Clock and SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.

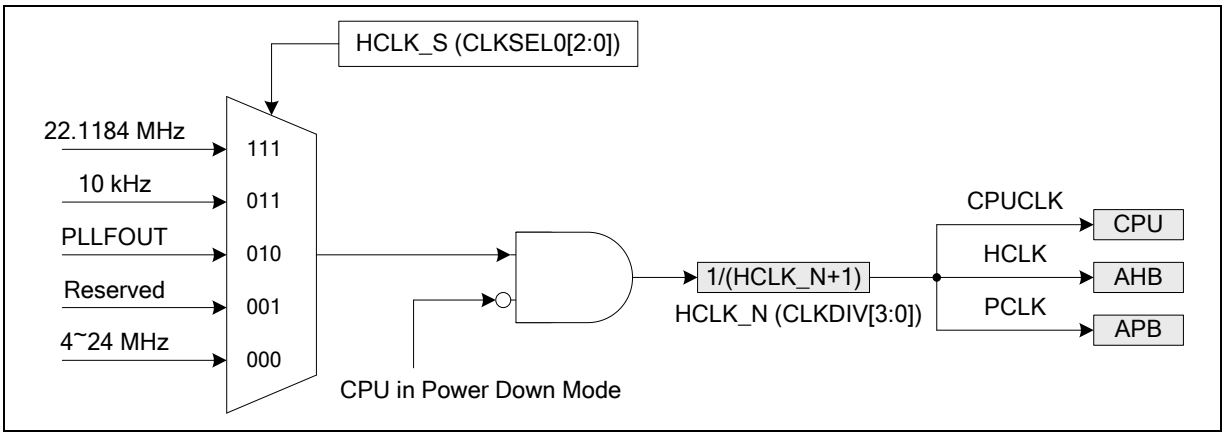


Figure 6.3-3 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-4.

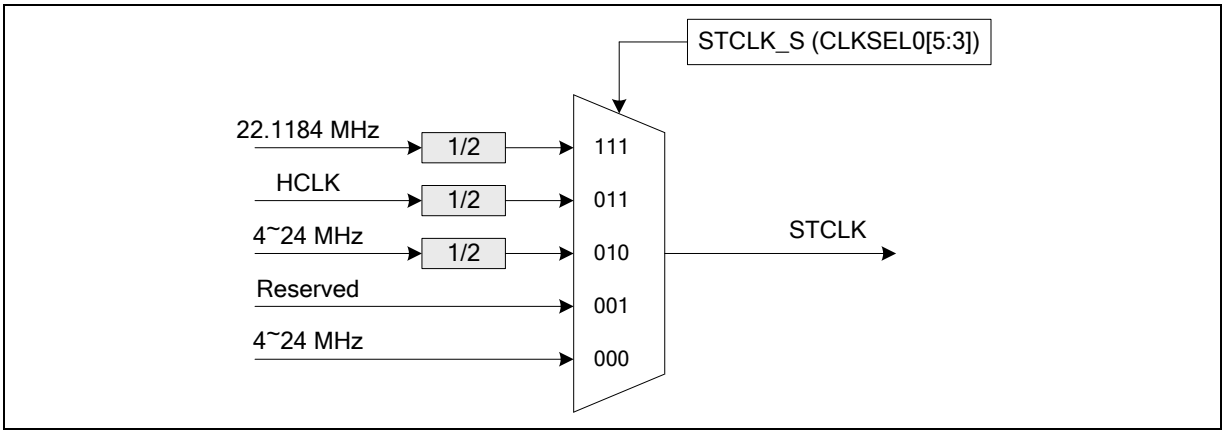


Figure 6.3-4 SysTick Clock Control Block Diagram

6.3.3 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
- WDT/Timer Peripherals Clock (when 10 kHz intertnal low speed RC oscillator (LIRC) is adopted as clock source)

6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

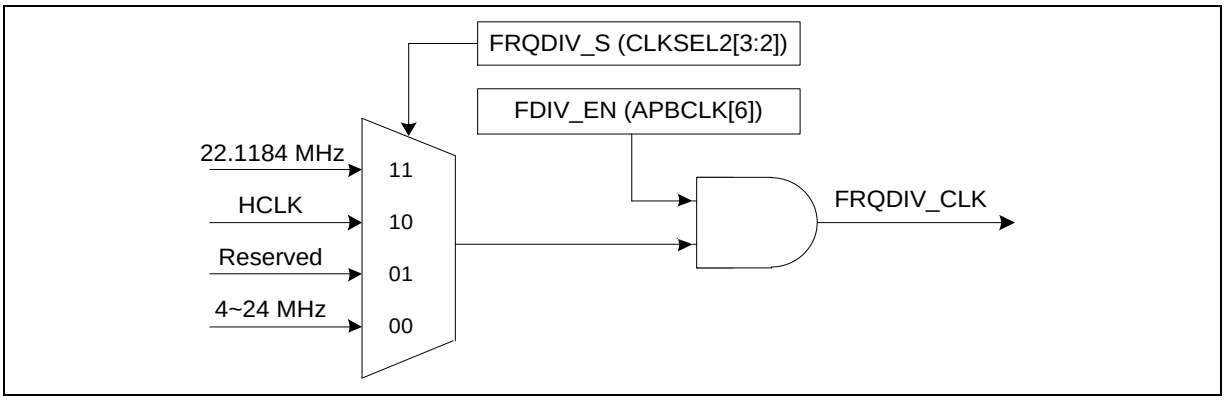


Figure 6.3-5 Clock Source of Frequency Divider

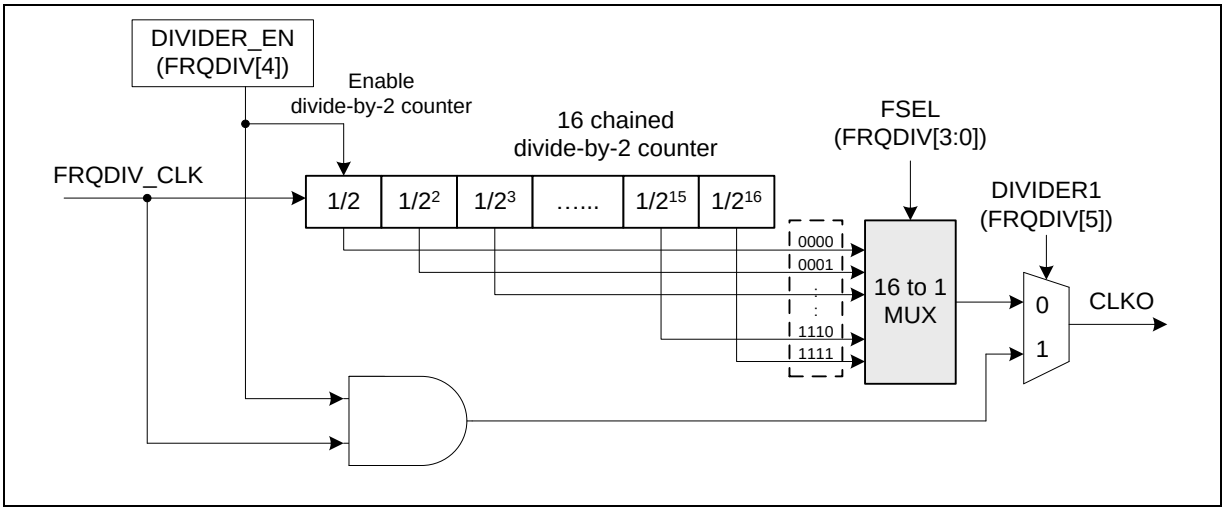


Figure 6.3-6 Frequency Divider Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® NUC131LD2AEU has 68 KB on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro® NUC131LD2AEU also provides additional Data Flash for user to store some application dependent data.

The NuMicro® NUC131LD2AEU supports another flexible feature: configurable Data Flash size. The Data Flash size is decided by Data Flash variable size enable (DFVSEN), Data Flash enable (DFEN) in Config0 and Data Flash base address (DFBADR) in Config1. When DFVSEN is set to 1, the Data Flash size is fixed at 4 KB and the address is started from 0x0001_F000, and the APROM size is become 64 KB. When DFVSEN is set to 0 and DFEN is set to 1, the Data Flash size is zero and the APROM size is 68 KB. When DFVSEN is set to 0 and DFEN is set to 0, the APROM and Data Flash share 68 KB continuous address and the start address of Data Flash is defined by (DFBADR) in Config1.

6.4.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 68 KB application program memory (APROM)
- 4 KB In-System-Programming (ISP) loader program memory (LDROM)
- Configurable Data Flash size
- 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro® NUC131LD2AEU has up to 42 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 42 pins are arranged in 5 ports named as GPIOA, GPIOB, GPIOC, GPIOD and GPIOF. The GPIOA port has 16 pins. The GPIOB port has 9 pins. The GPIOC port has 6 pins. The GPIOD port has 4 pins. The GPIOF port has 7 pins. Each of the 42 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 kΩ for V_{DD} from 5.0 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function

6.6 Timer Controller (TIMER)

6.6.1 Overview

The timer controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external counter pin (TM0~TM3)
- Supports external pin capture (TM0_EXT~TM3_EXT) for interval measurement
- Supports external pin capture (TM0_EXT~TM3_EXT) for reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.7 PWM Generator and Capture Timer (PWM)

6.7.1 Overview

The NUC131LD2AEU provides two PWM generators – PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses the comparator compared with counter to generate events. These events are used to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, which have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask, tri-state output enable and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.7.2 Features

6.7.2.1 PWM function features

- Supports maximum clock frequency up to100 MHz
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter, each module provides 3 PWM counters
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter match zero, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM counter match zero, period value or compared value

6.7.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.7.2.3 Compare table

Feature	PWM	BPWM
Counter number	2 channels share 1 timer, total 6 timers	6 channels share 1 timer, total 1 timer
Complementary mode	V	X
Dead-time function	V	X
Brake function	V	X
Capture reload	2 channels reload 1 timer	6 channels reload 1 timer

Table 6.7-1 PWM and BPWM Features Different Table

6.8 Basic PWM Generator and Capture Timer (BPWM)

6.8.1 Overview

The NUC131LD2AEU provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for ADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.8.2 Features

6.8.2.1 BPWM function features

- Supports maximum clock frequency up to100 MHz
- Supports up to two BPWM modules, each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution BPWM counter, each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt on the following events:
  - BPWM counter match zero, period value or compared value
- Supports trigger ADC on the following events:
  - BPWM counter match zero, period value or compared value

6.8.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.8.2.3 Compare table

Feature	PWM	BPWM
Counter number	2 channels share 1 timer, total 6 timers	6 channels share 1 timer, total 1 timer
Complementary mode	V	X
Dead-time function	V	X
Brake function	V	X
Capture reload	2 channels reload 1 timer	6 channels reload 1 timer

Table 6.8-1 PWM and BPWM Features Different Table

6.9 Watchdog Timer (WDT)

6.9.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.9.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer reset delay period
  - Selectable reset delay period includes (1026, 130, 18 or 3) * WDT_CLK reset delay period
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG0[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.10 Window Watchdog Timer (WWDT)

6.10.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.10.2 Features

- 6-bit down counter value (WWDTVAL[5:0]) and 6-bit compare window value (WWDTCR[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value to programmable maximum 11-bit prescale counter period of WWDT counter

6.11 UART Interface Controller (UART)

6.11.1 Overview

The NuMicro® NUC131LD2AEU provides up to six channels of Universal Asynchronous Receiver/Transmitters (UART). UART0/UART1/UART2 supports 16 bytes entry FIFO and UART3/UART4/UART5 support 1 byte buffer for data payload. Besides, only UART0 and UART1 support the flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function. UART0/UART1 provides RS-485 function mode. UART0/UART1/UART2 provides LIN master/slave function.

6.11.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16/16 bytes (UART0/UART1/UART2 support) entry FIFO and 1/1 bytes buffer for data payloads (UART3/UART4/UART5 support)
- Supports hardware auto-flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0/UART1 support).
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0/UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- LIN function mode (UART0/UART1/UART2 support)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode. (UART0/UART1 support)
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin.

6.12 I²C Serial Interface Controller (I²C)

6.12.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.12.2 Features

The I²C bus uses two wires (I2Cn_SDA and I2Cn_SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C serial interface controller
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function

6.13 Serial Peripheral Interface (SPI)

6.13.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro® NUC131LD2AEU contains one set of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. This SPI controller can be configured as a master or a slave device.

The SPI controller supports the variable bus clock function for special applications.

6.13.2 Features

- One set of SPI controller
- Supports Master or Slave mode operation
- Supports Dual I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32 bits
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the Byte Reorder function
- Supports Byte or Word Suspend mode
- Variable output bus clock frequency in Master mode
- Supports 3-wire, no slave select signal, bi-direction interface

6.14 Controller Area Network (CAN)

6.14.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.14.2 Features

- Supports CAN protocol version 2.0 part A and B.
- Bit rates up to 1 MBit/s.
- 32 Message Objects.
- Each Message Object has its own identifier mask.
- Programmable FIFO mode (concatenation of Message Objects).
- Maskable interrupt.
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications.
- Programmable loop-back mode for self-test operation.
- 16-bit module interfaces to the AMBA APB bus.
- Supports wake-up function

6.15 Analog-to-Digital Converter (ADC)

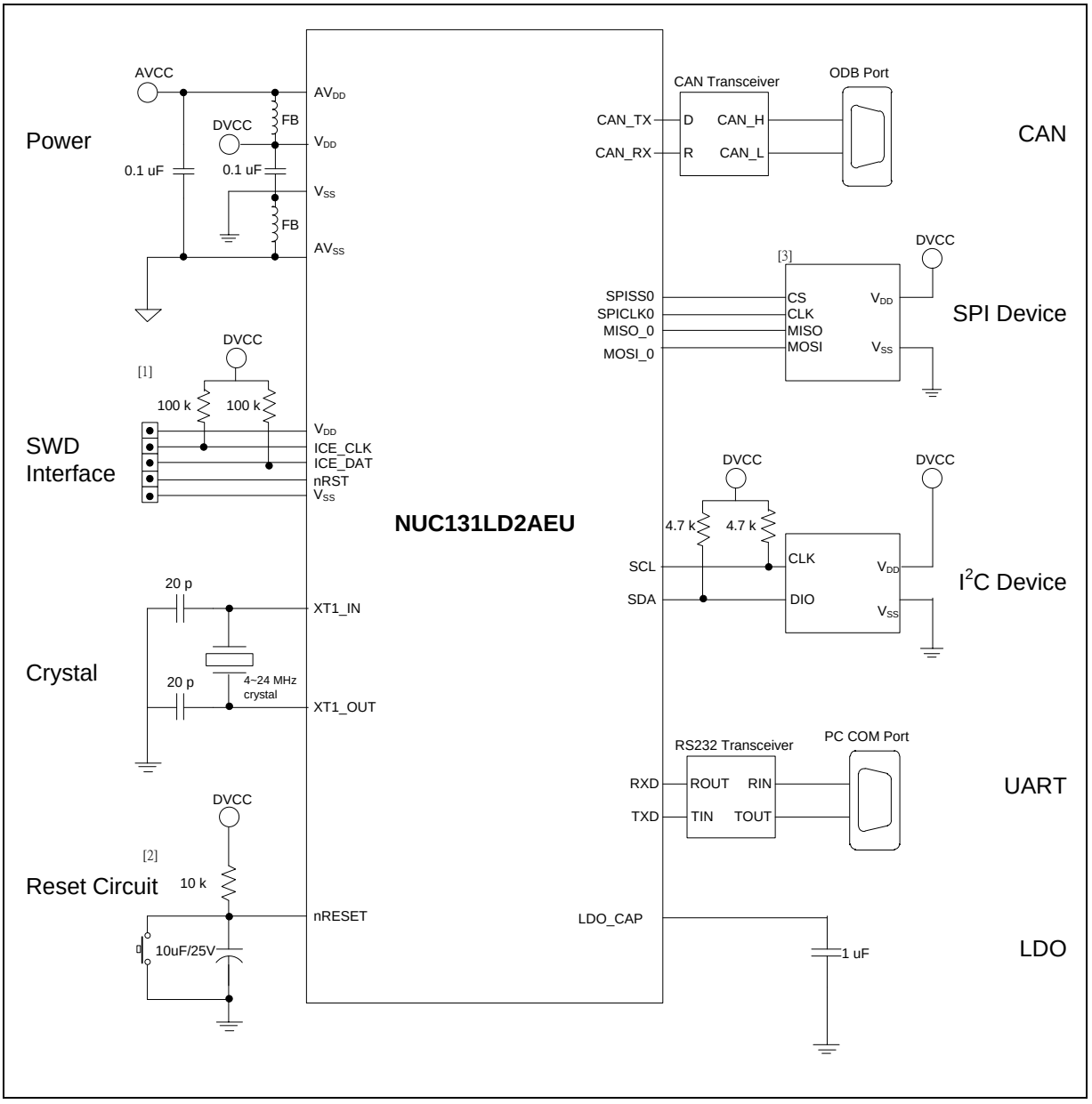
6.15.1 Overview

The NuMicro® NUC131LD2AEU contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM, BPWM trigger and external STADC pin.

6.15.2 Features

- Analog input voltage range: 0~V_{REF}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Up to 760 kSPS conversion rate (chip working at 5 V)
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by:
  - Writing 1 to ADST bit (ADCR[11])through software
  - PWM and BPWM trigger
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Supports two set digital comparators. The conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: external analog voltage, and internal Band-gap voltage

7 APPLICATION CIRCUIT



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Note 3: For the SPI device, the chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the NUC131LD2AEU chip supply voltage must also be 3.3 V

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply[*1]	V_{DD}–V_{SS}	-0.3	+6.1	V
Variations between different V_{DD} power pins	ΔV_{DD}	-	50	mV
Allowed voltage difference for V_{DD} and AV_{DD}	$\|V_{DD} – AV_{DD}\|$	-	50	mV
Variations between different V_{SS} ground pins	ΔV_{SS}	-	50	mV
Allowed voltage difference for V_{SS} and AV_{SS}	$\|V_{SS} – AV_{SS}\|$	-	50	mV
Input Voltage[*2]	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
	T_j	-40	+125	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}[*3]	ΣI_{DD}	-	120	mA
Maximum Current out of V_{SS}	ΣI_{SS}	-	120	mA
Maximum Current sunk by a I/O pin	-	-	35	mA
Maximum Current sourced by a I/O pin	-	-	35	mA
Maximum Current sunk by total I/O pins[*4]	-	-	100	mA
Maximum Current sourced by total I/O pins[*4]	-	-	100	mA
Maximum injected current by a I/O Pin[*5]	$I_{INJ(PIN)}$	-	±5	mA
Maximum injected current by total I/O Pins[*5]	$\Sigma I_{INJ(PIN)}$		±25	mA

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer the values of the maximum allowed injected current I_{INJ}
3. Maximum allowable current is a function of device maximum power dissipation.
4. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
5. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin

8.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=5.5 V, T_A = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation Voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5V ~ 5.5V up to 50 MHz				
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} ≥ 2.5V				
Band-gap Voltage	V_{BG}	1.13	1.20	1.27	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = -40°C~105°C				
Analog Operating Voltage	AV_{DD}	V_{DD}			V					
Operating Current Normal Run Mode at 50 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD1}	-	26	-	mA	V_{DD}	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{DD2}	-	12	-	mA	5.5V	12 MHz	X	V	X
	I_{DD3}	-	24	-	mA	3.3V	12 MHz	X	V	V
	I_{DD4}	-	11	-	mA	3.3V	12 MHz	X	V	X
Operating Current Normal Run Mode at 22.1184 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD5}	-	10	-	mA	5.5V	X	V	X	V
	I_{DD6}	-	4.1	-	mA	5.5V	X	V	X	X
	I_{DD7}	-	10	-	mA	3.3V	X	V	X	V
	I_{DD8}	-	4.1	-	mA	3.3V	X	V	X	X
Operating Current Normal Run Mode at 12 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD9}	-	8.3	-	mA	5.5V	12 MHz	X	X	V
	I_{DD10}	-	4.4	-	mA	5.5V	12 MHz	X	X	X
	I_{DD11}	-	6.8	-	mA	3.3V	12 MHz	X	X	V
	I_{DD12}	-	2.8	-	mA	3.3V	12 MHz	X	X	X
Operating Current Normal Run Mode at 4 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD13}	-	4.0	-	mA	5.5V	4 MHz	X	X	V
	I_{DD14}	-	2.6	-	mA	5.5V	4 MHz	X	X	X
	I_{DD15}	-	2.6	-	mA	3.3V	4 MHz	X	X	V
	I_{DD16}	-	1.3	-	mA	3.3V	4 MHz	X	X	X
Operating Current Normal Run Mode at 10 kHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD21}	-	111	-	µA	VDD	HXT/HIRC	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{DD22}	-	108	-	µA	5.5V	X	10	X	X
	I_{DD23}	-	98	-	µA	3.3V	X	10	X	V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{DD24}	-	96	-	µA	3.3V	X	10	X	X
Operating Current Idle Mode at 50 MHz V_{LDO} =1.8 V	I_{IDLE1}	-	21	-	mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{IDLE2}	-	8.2	-	mA	5.5V	12 MHz	X	V	X
	I_{IDLE3}	-	20	-	mA	3.3V	12 MHz	X	V	V
	I_{IDLE4}	-	6.7	-	mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 22.1184 MHz V_{LDO} =1.8 V	I_{IDLE5}	-	7.7	-	mA	5.5V	X	V	X	X
	I_{IDLE6}	-	2.1	-	mA	5.5V	X	V	X	X
	I_{IDLE7}	-	7.7	-	mA	3.3V	X	V	X	V
	I_{IDLE8}	-	2.1	-	mA	3.3V	X	V	X	X
Operating Current Idle Mode at 12 MHz V_{LDO} =1.8 V	I_{IDLE9}	-	7.3	-	mA	5.5V	12 MHz	X	X	V
	I_{IDLE10}	-	3.2	-	mA	5.5V	12 MHz	X	X	X
	I_{IDLE11}	-	5.8	-	mA	3.3V	12 MHz	X	X	V
	I_{IDLE12}	-	1.7	-	mA	3.3V	12 MHz	X	X	X
Operating Current Idle Mode at 4 MHz V_{LDO} =1.8 V	I_{IDLE13}	-	3.6	-	mA	5.5V	4 MHz	X	X	V
	I_{IDLE14}	-	2.2	-	mA	5.5V	4 MHz	X	X	X
	I_{IDLE15}	-	2.3	-	mA	3.3V	4 MHz	X	X	V
	I_{IDLE16}	-	0.96	-	mA	3.3V	4 MHz	X	X	X
Operating Current Idle Mode at 10 kHz V_{LDO} =1.8 V	I_{IDLE21}	-	110	-	µA	V_{DD}	HXT/HIRC	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{IDLE22}	-	107	-	µA	5.5V	X	10	X	X
	I_{IDLE23}	-	97	-	µA	3.3V	X	10	X	V
	I_{IDLE24}	-	95	-	µA	3.3V	X	10	X	X
Standby Current Power-down Mode (Deep Sleep Mode) V_{LDO} =1.6 V	I_{PWD1}	-	15	-	µA	V_{DD}	HXT/HIRC	LIRC (kHz)	PLL	RAM retension
						5.5V	X	10	X	V
	I_{PWD2}	-	15	-	µA	3.3V	X	10	X	V
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}	-	-67	-75	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}				

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-1	-	+1	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD} Open-drain or input only mode.
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]	-	-610	-650	µA	V_{DD} = 5.5V, V_{IN}=2.0V
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD}	V	V_{DD} = 5.5V
		1.5	-	V_{DD}		V_{DD} =3.0V
Input Low Voltage XT1_IN[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1_IN[*2]	V_{IH3}	3.5	-	V_{DD}	V	V_{DD} = 5.5V
		2.4	-	V_{DD}		V_{DD} = 3.0V
Negative going threshold (Schmitt input), nRESET	V_{ILS}	0	-	0.2*V_{DD}	V	
Positive going threshold (Schmitt input), nRESET	V_{IHS}	0.7*V_{DD}	-	V_{DD}	V	
Internal nRESET pin pull up resistor	R_{RST}	40	-	150	kΩ	
Negative going threshold (Schmitt input),	V_{ILS}	0	-	0.3*VDD	V	
Positive going threshold (Schmitt input),	V_{IHS}	0.7*V_{DD}	-	V_{DD}	V	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-400	-	µA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-80	-	µA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-73	-	µA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-20	-26	-	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-3	-5.2	-	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-2.5	-5	-	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional	I_{SK1}	10	17	-	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	6	11	-	mA	V_{DD} = 2.7V, V_S = 0.45V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
and Push-pull Mode)	I_{SK1}	5	10	-	mA	V_{DD} = 2.5V, V_S = 0.45V

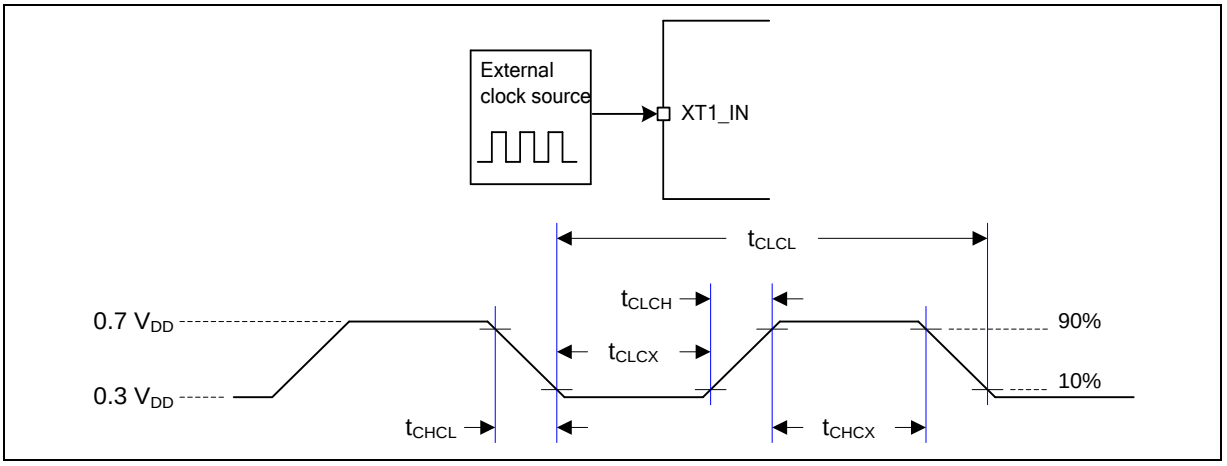
Note:

1. nRESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD, PE and PF can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD} = 5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode, the HXT oscillator is enabled, XT1_IN is a standard input pin to receive external clock and XT1_OUT is output pin to ouput inversed signal of XT1_IN. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	ns
t_{CLCX}	Clock Low Time		10	-	-	ns
t_{CLCH}	Clock Rise Time		2	-	15	ns
t_{CHCL}	Clock Fall Time		2	-	15	ns

8.3.2 External 4~24 MHz High Speed Crystal

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

SYMBOL	PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
V_{HXT}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
T_A	Temperature	-	-40	-	105	°C
I_{HXT}	Operating Current	12 MHz at V_{DD} = 5 V	-	2	-	mA
		12 MHz at V_{DD} = 3 V	-	0.8	-	mA
f_{HXT}	Clock Frequency	External crystal	4	-	24	MHz

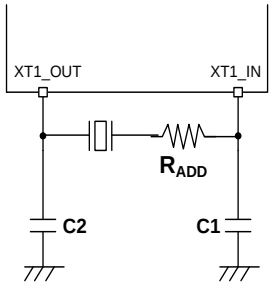
Notes:

1. Safety factor (S_f) must be higher than 10 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

   $$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

   R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

   R_S: Equivalent series resisotr(ESR) of crystal.



8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20 pF	10~20 pF	without

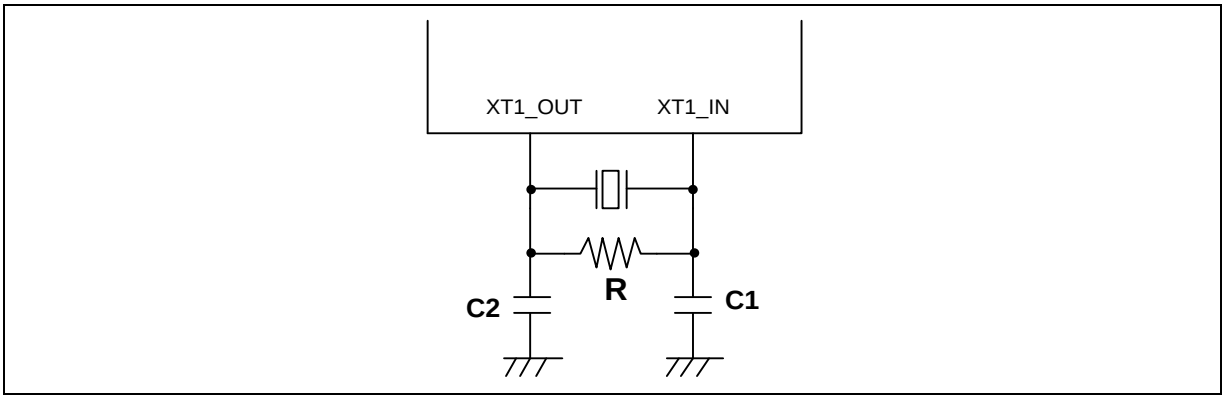


Figure 8.3-1 Typical Crystal Application Circuit

8.3.3 Internal 22.1184 MHz High Speed Oscillator

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HRC}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
f_{HRC}	Center Frequency	-	-	22.1184	-	MHz
	Calibrated Internal Oscillator Frequency	+25°C; V_{DD} = 5 V	-1	-	+1	%
		-40°C ~ +105°C; V_{DD} = 2.5 V ~ 5.5 V	-2	-	+2	%
I_{HRC}	Operation Current	V_{DD} = 5 V	-	744	-	μA

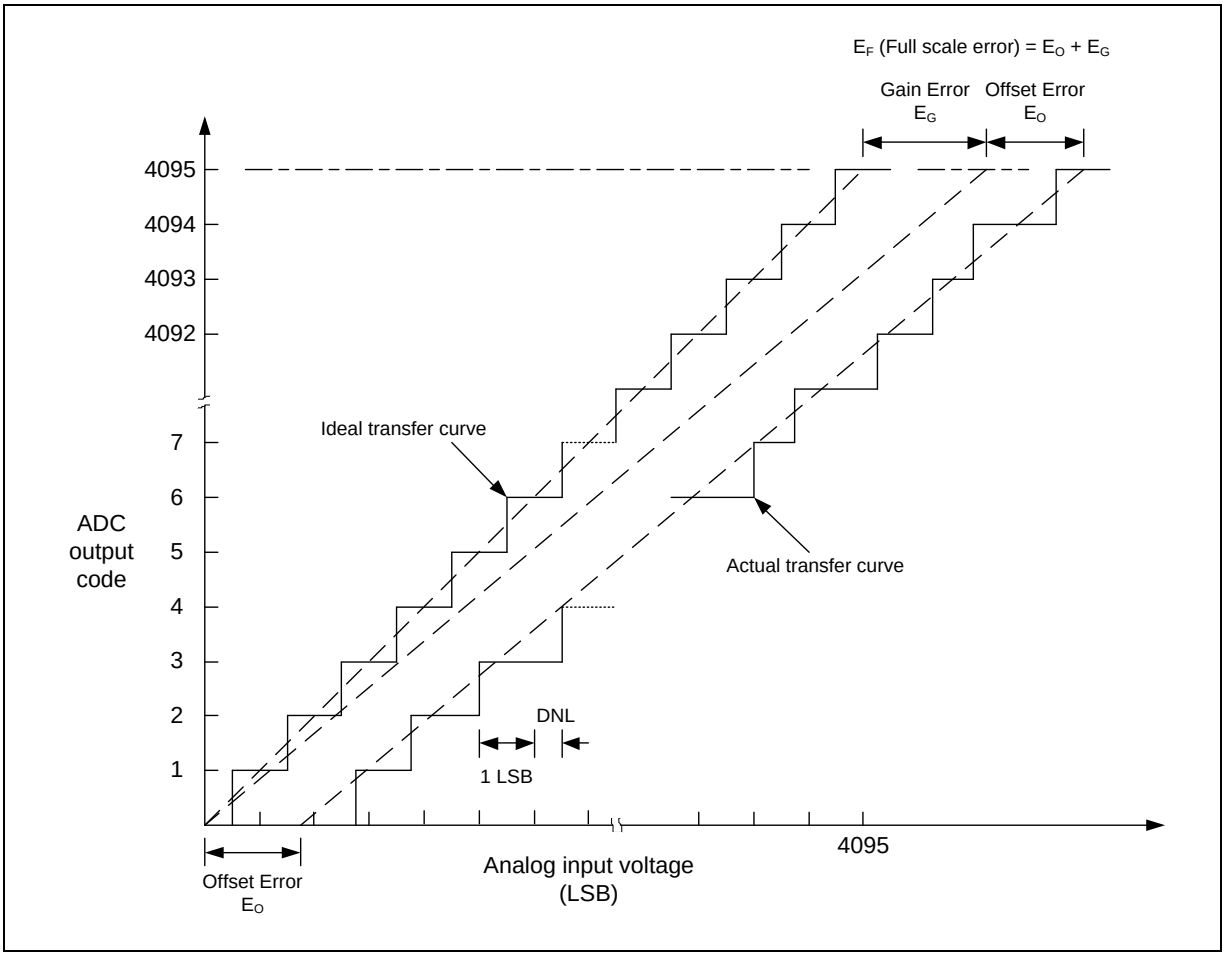
8.3.4 Internal 10 kHz Low Speed Oscillator

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{LRC}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
f_{LRC}	Center Frequency	-	-	10	-	kHz
-	Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5 V	-10	-	+10	%
		-40°C ~ +105°C; V_{DD} = 2.5 V ~ 5.5 V	-50	-	+50	%

8.4 Analog Characteristics

8.4.1 12-bit SARADC Specification

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	-1~2	-1~4	LSB
INL	Integral nonlinearity error	-	±2	±4	LSB
E_O	Offset error	-	3	-	LSB
E_G	Gain error (Transfer gain)	-	-3	-	-
E_A	Absolute Error	-	4	-	LSB
-	Monotonic	Guaranteed			
F_{ADC}	ADC clock frequency (AV_{DD} = 4.5V~5.5V)	-	-	16	MHz
F_S	Sample rate (F_{ADC}/T_{CONV})	-	-	760	kSPS
T_{ACQ}	Acquisition Time (Sample Stage)	2~9			$1/F_{ADC}$
T_{CONV}	Total Conversion Time	16~23			$1/F_{ADC}$
V_{DDA}	Supplt Current	3	-	5.5	V
I_{DDA}	Supply current (Avg.)	-	2.9	-	mA
V_{IN}	Input voltage	0	-	AV_{DD}	V
C_{IN}	Input Capacitance	-	6	-	pF
R_{IN}	Input Load	-	6.5	-	kΩ



8.4.2 LDO and Power Management Specification

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{DD}	Input Voltage V_{DD}	2.5	-	5.5	V	V_{DD} input voltage
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5 V
T_A	Operating Temperature	-40	25	105	°C	

Note:

1. It is recommended a 0.1 µF bypass capacitor is connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 1 µF Capacitor must be connected between LDO_CAP pin and the closest VSS pin of the device.

8.4.3 Low Voltage Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Quiescent Current	AV_{DD} = 5.5 V	-	1	5	μA
I_{LVR}	Operation Temperature	-	-40	25	105	°C
V_{LVR}	Threshold Voltage	TA = 25 °C	2.00	2.0	2.4	V
		TA = -40 °C	1.95	1.98	2.02	V
		TA = 105 °C	2.04	2.13	2.25	V

8.4.4 Brown-out Detector Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Temperature	-	-40	25	105	°C
I_{BOD}	Quiescent Current	AVDD=5.5 V	-	-	140	μA
V_{BOD}	Brown-out Voltage (Falling edge)	BOD_VL[1:0]=11	4.45	4.53	4.56	V
		BOD_VL [1:0]=10	3.74	3.8	3.84	V
		BOD_VL [1:0]=01	2.73	2.77	2.85	V
		BOD_VL [1:0]=00	2.22	2.25	2.28	V
V_{BOD}	Brown-out Voltage (Rising edge)	BOD_VL[1:0]=11	4.34	4.39	4.41	V
		BOD_VL [1:0]=10	3.65	3.69	3.71	V
		BOD_VL [1:0]=01	2.66	2.69	2.7	V
		BOD_VL [1:0]=00	2.16	2.19	2.2	V

8.4.5 Power-on Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
T_A	Operation Temperature	-	-40	25	105	°C
V_{POR}	Reset Voltage	V+	1.6	2	2.4	V
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	-	100	mV
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	-	0.025	-	20	ms/V
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	-	0.5	-	-	ms

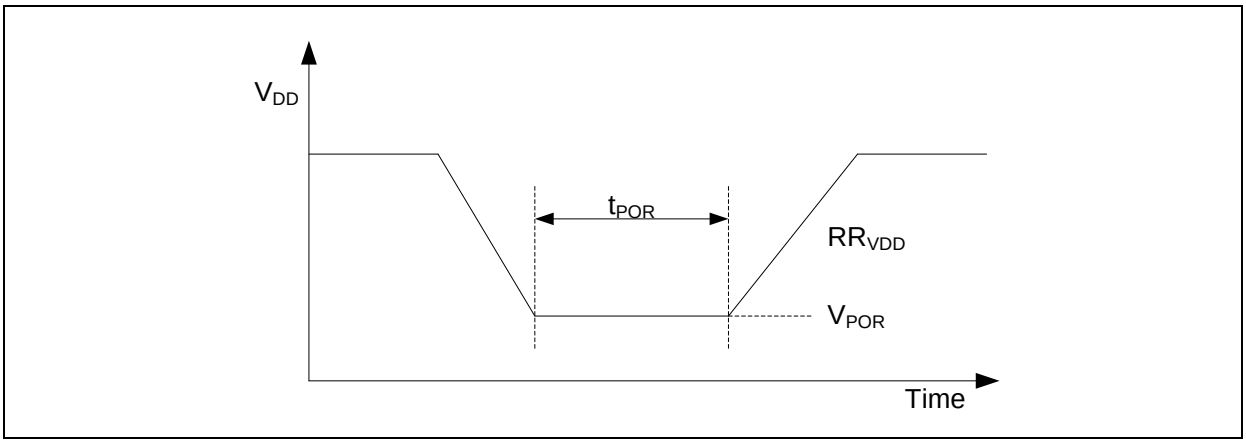


Figure 8.4-1 Power-up Ramp Condition

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{FLA}[1]	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		20000	-	-	cycles[2]
T_{RET}	Data Retention	At 85°C	10	-	-	year
T_{ERASE}	Page Erase Time		20	-	-	ms
T_{MER}	Mass Erase Time		40	-	-	ms
T_{PROG}	Program Time		40	-	-	μs

Note:

1. V_{FLA} is source from chip LDO output voltage
2. Number of program/erase cycles.

8.6 I²C Dynamic Characteristics

SYMBOL	PARAMETER	STANDARD MODE[1][2]		FAST MODE[1][2]		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{LOW}	SCL low period	4.7	-	1.3	-	µs
t_{HIGH}	SCL high period	4	-	0.6	-	µs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	µs
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

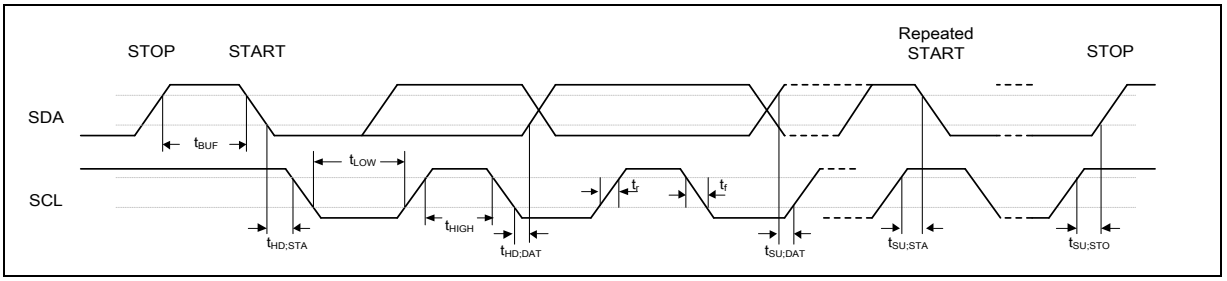


Figure 8.6-1 I²C Timing Diagram

8.7 SPI Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4	-	-	ns
t_V	Data output valid time	-	1	2	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	2	4	ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	3.5	-	-	ns
t_V	Data output valid time	-	16	22	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	18	24	ns

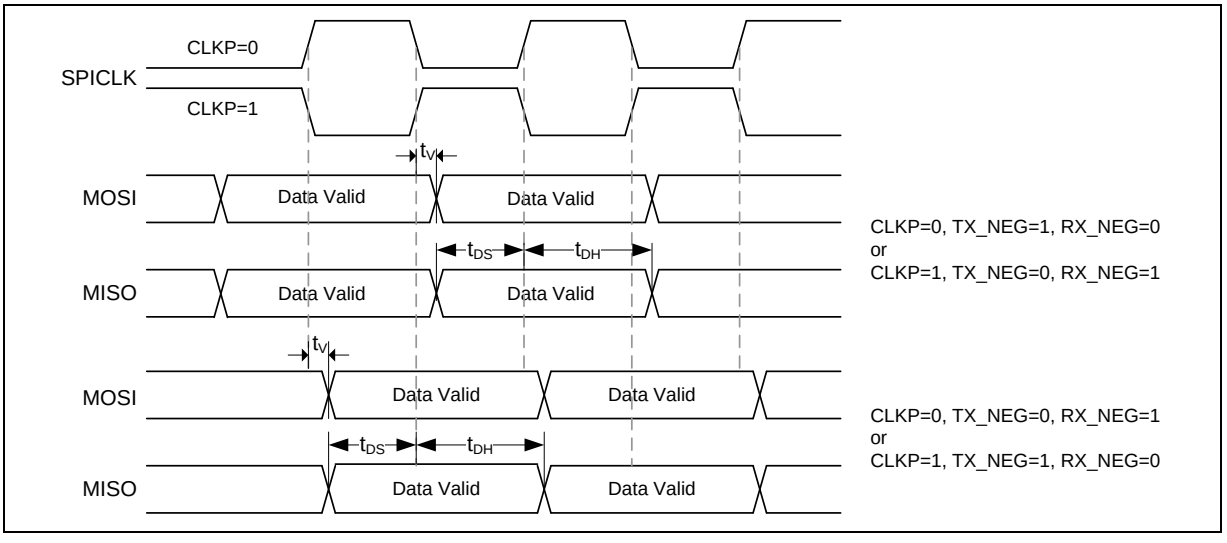


Figure 8.7-1 SPI Master Mode Timing Diagram

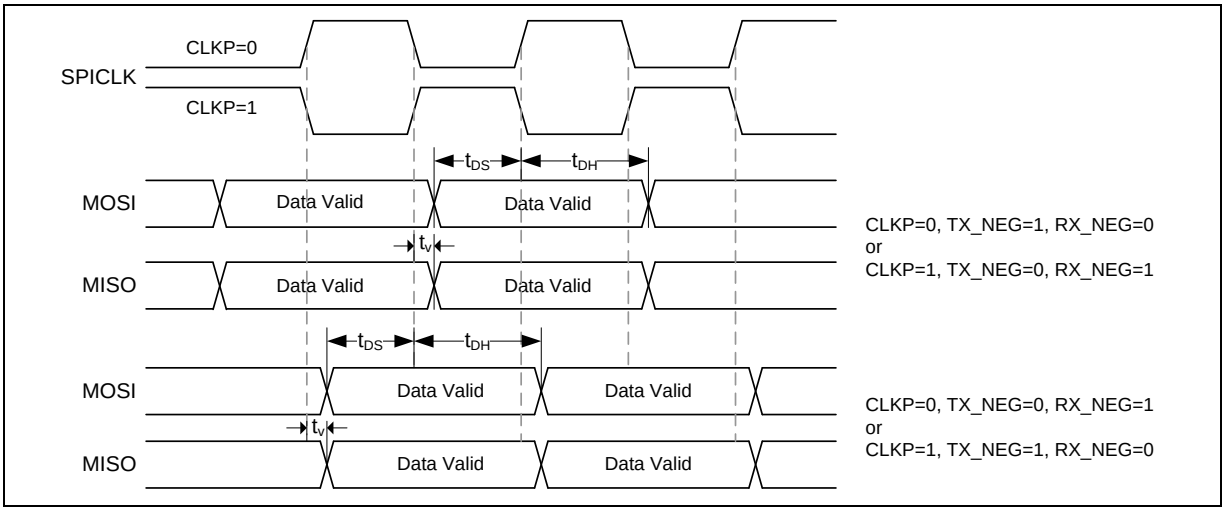
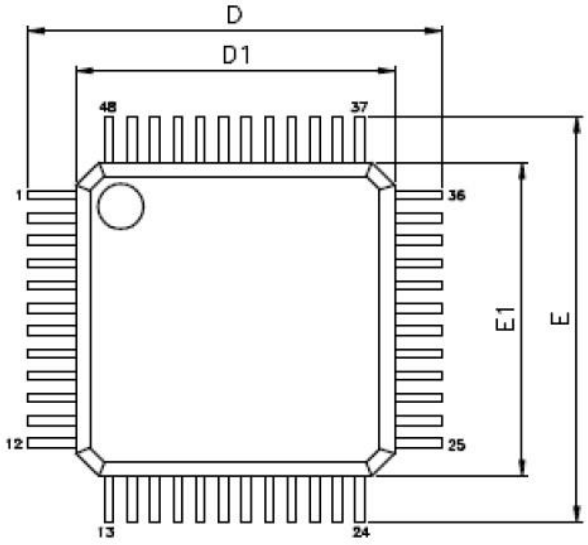
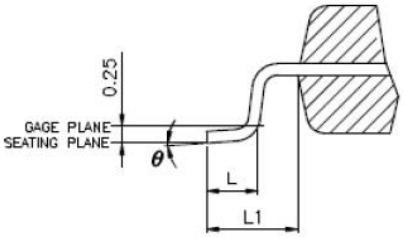


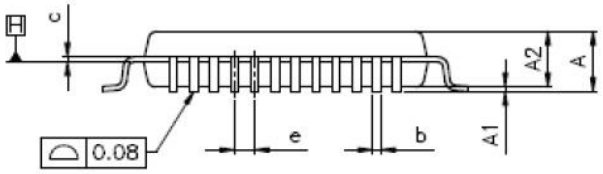
Figure 8.7-2 SPI Slave Mode Timing Diagram

9 PACKAGE DIMENSIONS

9.1 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

10 REVISION HISTORY

Date	Revision	Description
2020.04.07	1.00	Initial version

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