

## Features

- 2.7V to 3.6V Supply
  - Full Read and Write Operation
- Low Power Dissipation
  - 8 mA Active Current
  - 50  $\mu$ A CMOS Standby Current
- Read Access Time – 300 ns
- Byte Write – 3 ms
- Direct Microprocessor Control
  - $\overline{\text{DATA}}$  Polling
  - $\text{READY}/\overline{\text{BUSY}}$  Open Drain Output
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-Wide Pinout
- Industrial Temperature Ranges

## 1. Description

The AT28BV64 is a low-voltage, low-power Electrically Erasable and Programmable Read-only Memory specifically designed for battery powered applications. Its 64K of memory is organized 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation less than 30 mW. When the device is deselected the standby current is less than 50  $\mu$ A.

The AT28BV64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of  $\text{RDY}/\overline{\text{BUSY}}$  and  $\overline{\text{DATA}}$  polling of  $\text{I/O}_7$ . Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28BV64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of EEPROM are available for device identification or tracking.



## 64K (8K x 8) Battery-Voltage Parallel EEPROMs

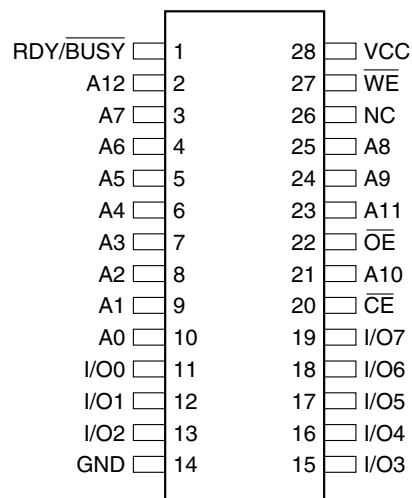
### AT28BV64

**Not Recommended  
for New Designs.**

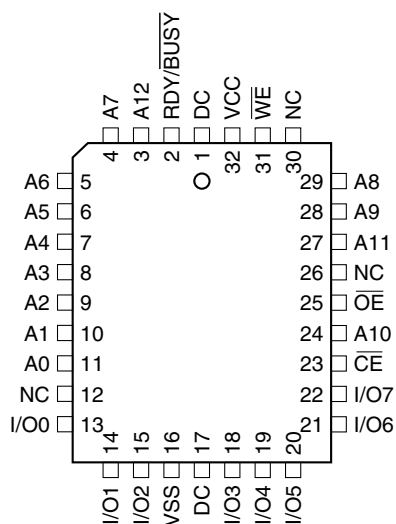
## 2. Pin Configurations

| Pin Name               | Function            |
|------------------------|---------------------|
| A0 - A12               | Addresses           |
| $\overline{CE}$        | Chip Enable         |
| $\overline{OE}$        | Output Enable       |
| $\overline{WE}$        | Write Enable        |
| I/O0 - I/O7            | Data Inputs/Outputs |
| RDY/ $\overline{BUSY}$ | Ready/Busy Output   |
| NC                     | No Connect          |
| DC                     | Don't Connect       |

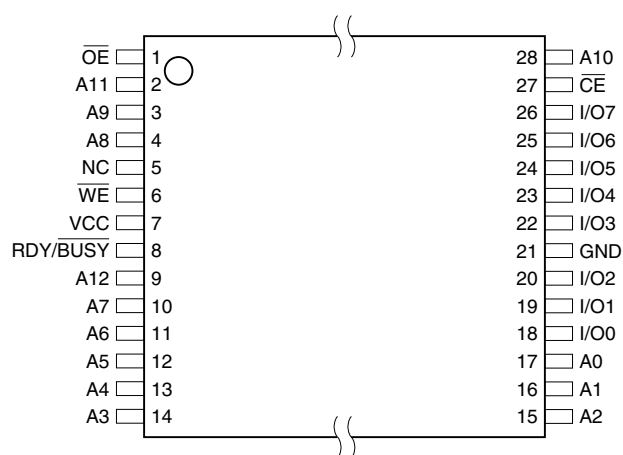
## 2.2 PDIP, SOIC Top View



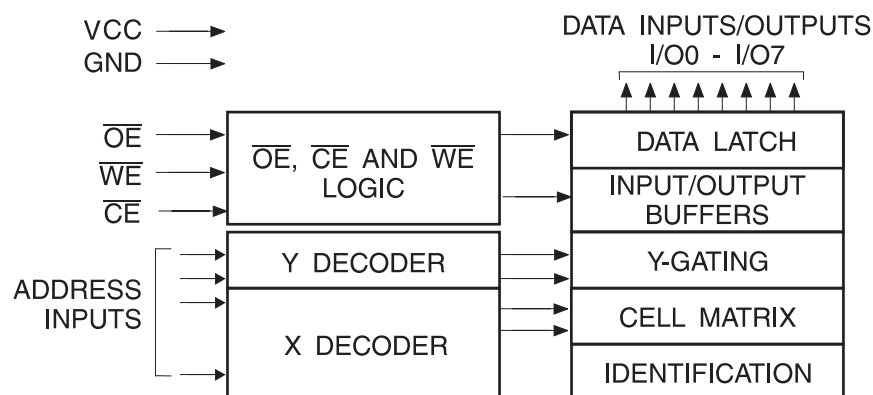
## 2.1 PLCC Top View



## 2.3 TSOP Top View



### 3. Block Diagram



### 4. Absolute Maximum Ratings\*

|                                                                        |                          |
|------------------------------------------------------------------------|--------------------------|
| Temperature Under Bias .....                                           | -55°C to +125°C          |
| Storage Temperature .....                                              | -65°C to +150°C          |
| All Input Voltages (including NC Pins)<br>with Respect to Ground ..... | -0.6V to +6.25V          |
| All Output Voltages<br>with Respect to Ground .....                    | -0.6V to $V_{CC} + 0.6V$ |
| Voltage on $\overline{OE}$ and A9<br>with Respect to Ground .....      | -0.6V to +13.5V          |

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## 5. Device Operation

### 5.1 Read

The AT28BV64 is accessed like a Static RAM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever  $\overline{CE}$  or  $\overline{OE}$  is high. This dual line control gives designers increased flexibility in preventing bus contention.

### 5.2 Byte Write

Writing data into the AT28BV64 is similar to writing into a Static RAM. A low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{OE}$  high and  $\overline{CE}$  or  $\overline{WE}$  low (respectively) initiates a byte write. The address location is latched on the falling edge of  $\overline{WE}$  (or  $\overline{CE}$ ); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of  $t_{WC}$ , a read operation will effectively be a polling operation.

### 5.3 $\overline{RDY}/\overline{BUSY}$

Pin 1 is an open drain  $\overline{RDY}/\overline{BUSY}$  output that can be used to detect the end of a write cycle.  $\overline{RDY}/\overline{BUSY}$  is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same  $\overline{RDY}/\overline{BUSY}$  line.

### 5.4 $\overline{DATA}$ Polling

The AT28BV64 provides  $\overline{DATA}$  Polling to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for  $I/O_7$  (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

### 5.5 Write Protection

Inadvertent writes to the device are protected against in the following ways: (a)  $V_{CC}$  sense – if  $V_{CC}$  is below 1.8V (typical) the write function is inhibited; (b)  $V_{CC}$  power on delay – once  $V_{CC}$  has reached 2.0V the device will automatically time out 10 ms (typical) before allowing a byte write; and (c) Write Inhibit – holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high or  $\overline{WE}$  high inhibits byte write cycles.

## 6. DC and AC Operating Range

|                              | AT28BV64-30  |
|------------------------------|--------------|
| Operating Temperature (Case) | -40°C - 85°C |
| V <sub>CC</sub> Power Supply | 2.7V to 3.6V |

## 7. Operating Modes

| Mode                  | $\overline{CE}$ | $\overline{OE}$  | $\overline{WE}$ | I/O              |
|-----------------------|-----------------|------------------|-----------------|------------------|
| Read                  | V <sub>IL</sub> | V <sub>IL</sub>  | V <sub>IH</sub> | D <sub>OUT</sub> |
| Write <sup>(2)</sup>  | V <sub>IL</sub> | V <sub>IH</sub>  | V <sub>IL</sub> | D <sub>IN</sub>  |
| Standby/Write Inhibit | V <sub>IH</sub> | X <sup>(1)</sup> | X               | High Z           |
| Write Inhibit         | X               | X                | V <sub>IH</sub> |                  |
| Write Inhibit         | X               | V <sub>IL</sub>  | X               |                  |
| Output Disable        | X               | V <sub>IH</sub>  | X               | High Z           |

Notes: 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.  
 2. Refer to AC Programming Waveforms.

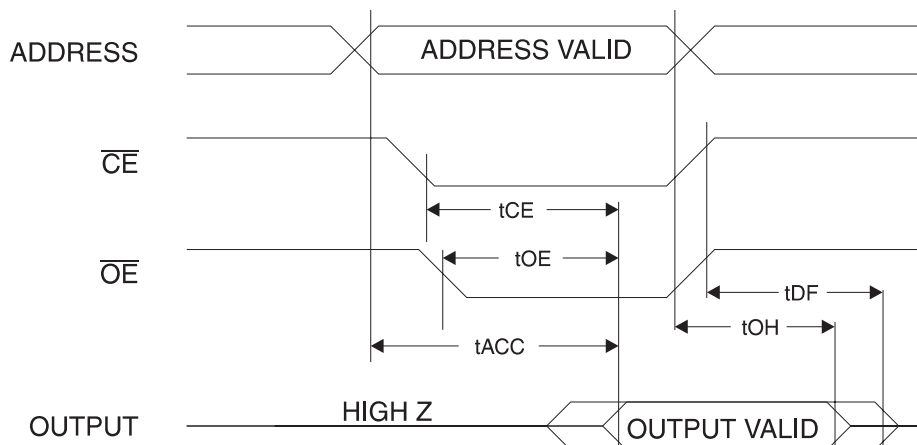
## 8. DC Characteristics

| Symbol          | Parameter                            | Condition                                                 | Min | Max | Units |
|-----------------|--------------------------------------|-----------------------------------------------------------|-----|-----|-------|
| I <sub>LI</sub> | Input Load Current                   | V <sub>IN</sub> = 0V to V <sub>CC</sub> + 1.0V            |     | 5   | μA    |
| I <sub>LO</sub> | Output Leakage Current               | V <sub>I/O</sub> = 0V to V <sub>CC</sub>                  |     | 5   | μA    |
| I <sub>SB</sub> | V <sub>CC</sub> Standby Current CMOS | $\overline{CE} = V_{CC} - 0.3V$ to V <sub>CC</sub> + 1.0V |     | 50  | μA    |
| I <sub>CC</sub> | V <sub>CC</sub> Active Current AC    | f = 5 MHz; I <sub>OUT</sub> = 0 mA; CE = V <sub>IL</sub>  |     | 8   | mA    |
| V <sub>IL</sub> | Input Low Voltage                    |                                                           |     | 0.6 | V     |
| V <sub>IH</sub> | Input High Voltage                   |                                                           | 2.0 |     | V     |
| V <sub>OL</sub> | Output Low Voltage                   | I <sub>OL</sub> = 1 mA                                    |     | 0.3 | V     |
|                 |                                      | I <sub>OL</sub> = 2 mA for RDY/ $\overline{BUSY}$         |     | 0.3 | V     |
| V <sub>OH</sub> | Output High Voltage                  | I <sub>OH</sub> = -100 μA                                 | 2.0 |     | V     |

## 9. AC Read Characteristics

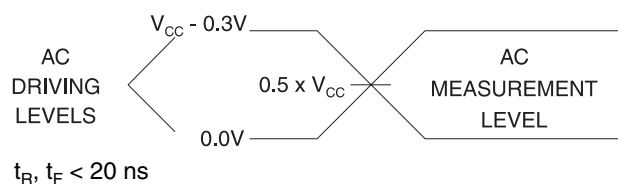
| Symbol            | Parameter                                                                               | AT28BV64-30 |     | Units |
|-------------------|-----------------------------------------------------------------------------------------|-------------|-----|-------|
|                   |                                                                                         | Min         | Max |       |
| $t_{ACC}$         | Address to Output Delay                                                                 |             | 300 | ns    |
| $t_{CE}^{(1)}$    | $\overline{CE}$ to Output Delay                                                         |             | 300 | ns    |
| $t_{OE}^{(2)}$    | $\overline{OE}$ to Output Delay                                                         | 0           | 150 | ns    |
| $t_{DF}^{(3)(4)}$ | $\overline{CE}$ or $\overline{OE}$ High to Output Float                                 | 0           | 60  | ns    |
| $t_{OH}$          | Output Hold from $\overline{OE}$ , $\overline{CE}$ or Address, whichever occurred first | 0           |     | ns    |

## 10. AC Read Waveforms<sup>(1)(2)(3)(4)</sup>

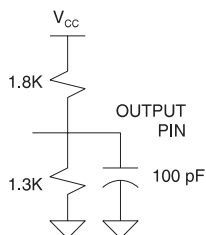


- Notes:
- $\overline{CE}$  may be delayed up to  $t_{ACC} - t_{CE}$  after the address transition without impact on  $t_{ACC}$ .
  - $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$  or by  $t_{ACC} - t_{OE}$  after an address change without impact on  $t_{ACC}$ .
  - $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$  whichever occurs first ( $C_L = 5$  pF).
  - This parameter is characterized and is not 100% tested.

## 11. Input Test Waveforms and Measurement Level



## 12. Output Test Load



## 13. Pin Capacitance

$f = 1 \text{ MHz}$ ,  $T = 25^\circ\text{C}^{(1)}$

| Symbol    | Typ | Max | Units | Conditions     |
|-----------|-----|-----|-------|----------------|
| $C_{IN}$  | 4   | 6   | pF    | $V_{IN} = 0V$  |
| $C_{OUT}$ | 8   | 12  | pF    | $V_{OUT} = 0V$ |

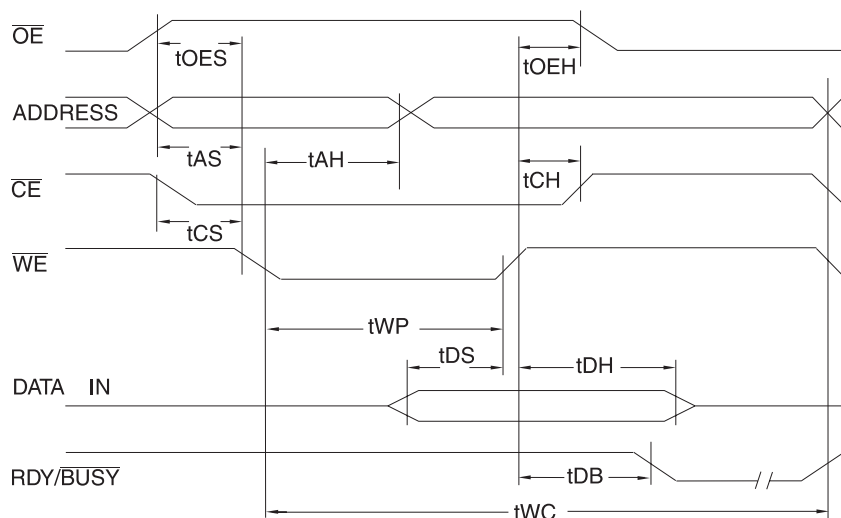
Note: 1. This parameter is characterized and is not 100% tested.

## 14. AC Write Characteristics

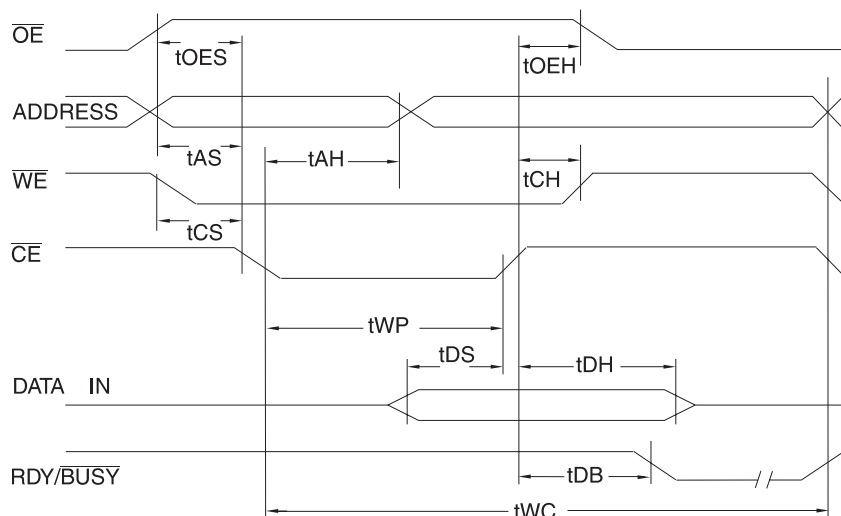
| Symbol            | Parameter                                                | Min | Max  | Units |
|-------------------|----------------------------------------------------------|-----|------|-------|
| $t_{AS}, t_{OES}$ | Address, $\overline{OE}$ Set-up Time                     | 10  |      | ns    |
| $t_{AH}$          | Address Hold Time                                        | 100 |      | ns    |
| $t_{WP}$          | Write Pulse Width ( $\overline{WE}$ or $\overline{CE}$ ) | 150 | 1000 | ns    |
| $t_{DS}$          | Data Set-up Time                                         | 100 |      | ns    |
| $t_{DH}, t_{OEH}$ | Data, $\overline{OE}$ Hold Time                          | 10  |      | ns    |
| $t_{DB}$          | Time to Device Busy                                      |     | 50   | ns    |
| $t_{WC}$          | Write Cycle Time                                         |     | 3    | ms    |

## 15. AC Write Waveforms

### 15.1 $\overline{WE}$ Controlled



### 15.2 $\overline{CE}$ Controlled

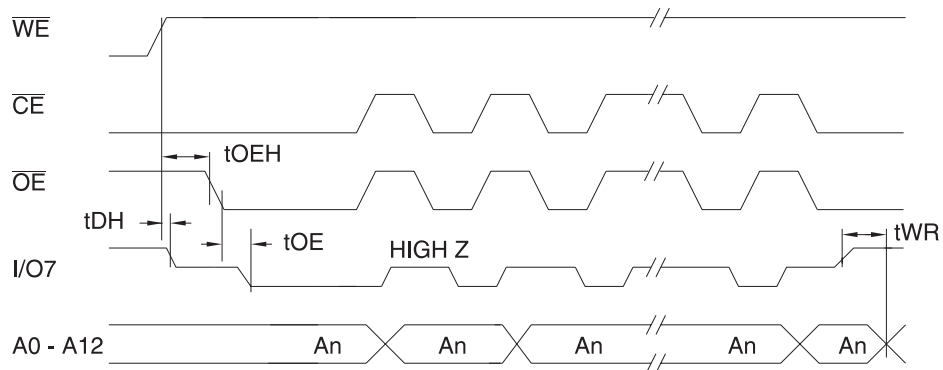


## 16. Data Polling Characteristics<sup>(1)</sup>

| Symbol               | Parameter                                      | Min | Typ | Max | Units |
|----------------------|------------------------------------------------|-----|-----|-----|-------|
| $t_{DH}$             | Data Hold Time                                 | 10  |     |     | ns    |
| $t_{OE\overline{H}}$ | $\overline{OE}$ Hold Time                      | 10  |     |     | ns    |
| $t_{OE}$             | $\overline{OE}$ to Output Delay <sup>(2)</sup> |     |     |     | ns    |
| $t_{WR}$             | Write Recovery Time                            | 0   |     |     | ns    |

Notes: 1. These parameters are characterized and not 100% tested.  
2. See AC Characteristics.

## 17. Data Polling Waveforms



## 18. Ordering Information

### 18.1 Standard Package<sup>(1)</sup>

| t <sub>ACC</sub><br>(ns) | I <sub>CC</sub> (mA) |         | Operating<br>Voltage | Ordering Code                                                    | Package                   | Operation Range                 |
|--------------------------|----------------------|---------|----------------------|------------------------------------------------------------------|---------------------------|---------------------------------|
|                          | Active               | Standby |                      |                                                                  |                           |                                 |
| 300                      | 8                    | 0.05    | 2.7V to 3.6V         | AT28BV64-30JI<br>AT28BV64-30PI<br>AT28BV64-30SI<br>AT28BV64-30TI | 32J<br>28P6<br>28S<br>28T | Industrial<br>(-40° C to 85° C) |

Note: 1. See Valid Part Number table below.

| Package Type |                                                              |
|--------------|--------------------------------------------------------------|
| <b>32J</b>   | 32-lead, Plastic J-leaded Chip Carrier (PLCC)                |
| <b>28P6</b>  | 28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)     |
| <b>28S</b>   | 28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |
| <b>28T</b>   | 28-lead, Plastic Thin Small Outline Package (TSOP)           |

### 18.2 Valid Part Number

The following table lists standard Atmel® products that can be ordered.

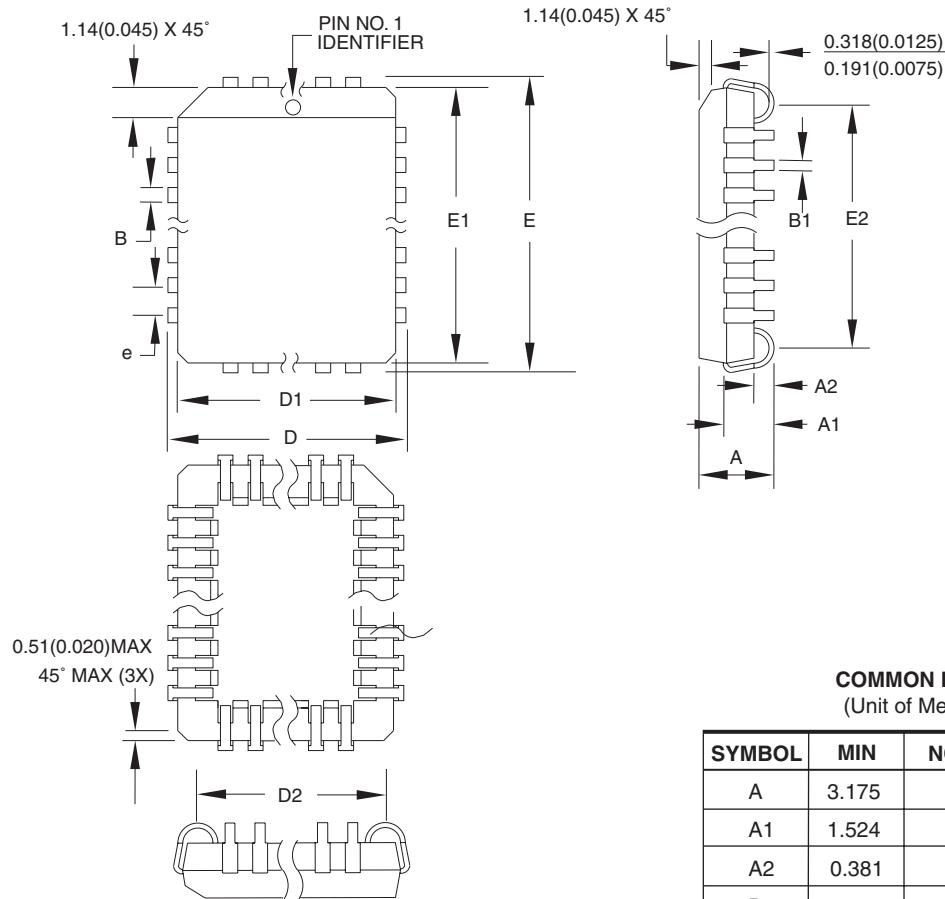
| Device Numbers | Speed | Package and Temperature Combinations |
|----------------|-------|--------------------------------------|
| AT28BV64       | 30    | JI, PI, SI, TI                       |

## 19. Die Products

|                                                 |
|-------------------------------------------------|
| Reference Section: Parallel EEPROM Die Products |
|-------------------------------------------------|

## 20. Packaging Information

### 20.1 32J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 3.175     | –   | 3.556  |        |
| A1     | 1.524     | –   | 2.413  |        |
| A2     | 0.381     | –   | –      |        |
| D      | 12.319    | –   | 12.573 |        |
| D1     | 11.354    | –   | 11.506 | Note 2 |
| D2     | 9.906     | –   | 10.922 |        |
| E      | 14.859    | –   | 15.113 |        |
| E1     | 13.894    | –   | 14.046 | Note 2 |
| E2     | 12.471    | –   | 13.487 |        |
| B      | 0.660     | –   | 0.813  |        |
| B1     | 0.330     | –   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)**

**DRAWING NO.**

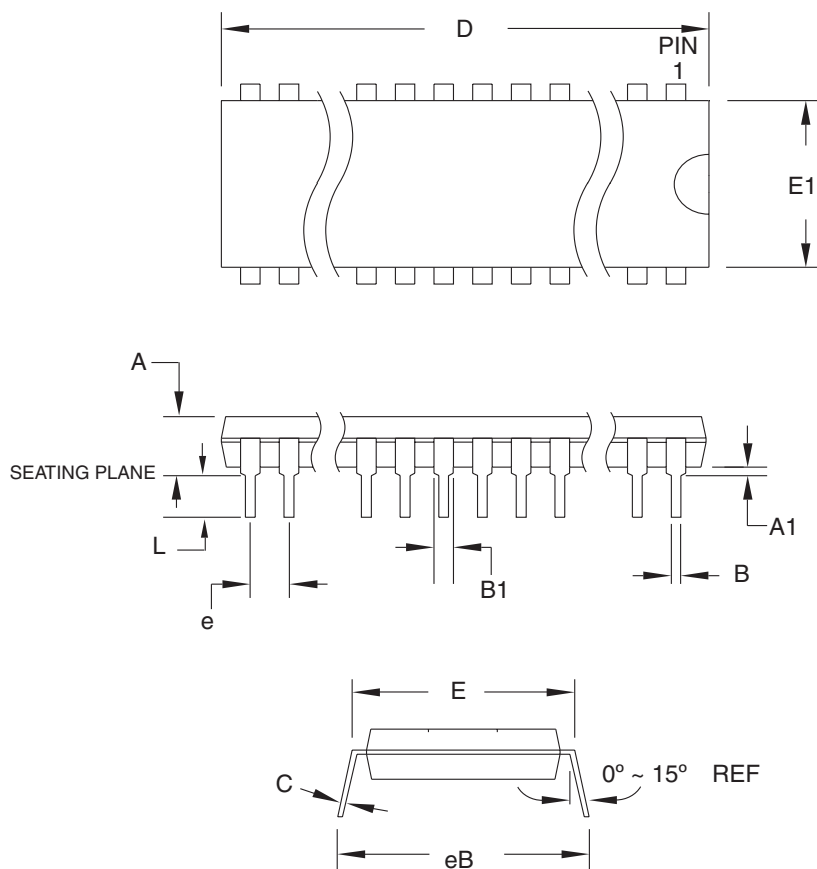
32J

**REV.**

B



## 20.2 28P6 – PDIP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | –         | –   | 4.826  |        |
| A1     | 0.381     | –   | –      |        |
| D      | 36.703    | –   | 37.338 | Note 2 |
| E      | 15.240    | –   | 15.875 |        |
| E1     | 13.462    | –   | 13.970 | Note 2 |
| B      | 0.356     | –   | 0.559  |        |
| B1     | 1.041     | –   | 1.651  |        |
| L      | 3.048     | –   | 3.556  |        |
| C      | 0.203     | –   | 0.381  |        |
| eB     | 15.494    | –   | 17.526 |        |
| e      | 2.540 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AB.
  2. Dimensions D and E1 do not include mold Flash or Protrusion.  
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**28P6**, 28-lead (0.600"/15.24 mm Wide) Plastic Dual  
Inline Package (PDIP)

### DRAWING NO.

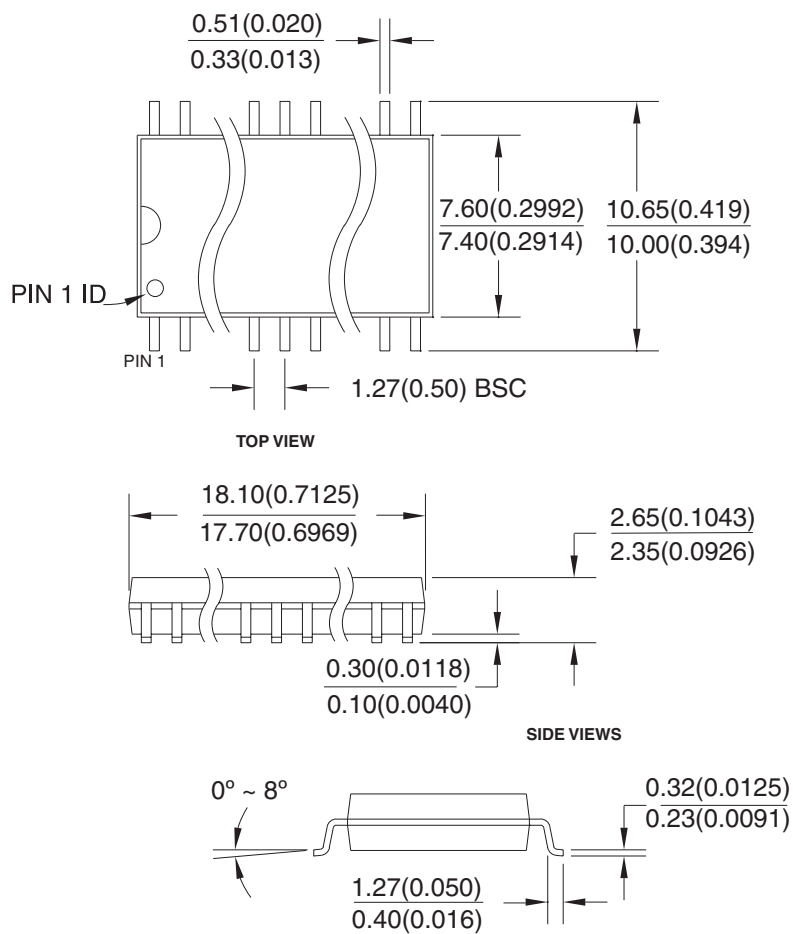
28P6

### REV.

B

## 20.3 28S – SOIC

Dimensions in Millimeters and (Inches).  
Controlling dimension: Millimeters.



8/4/03



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**28S**, 28-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC)  
JEDEC Standard MS-013

**DRAWING NO.**

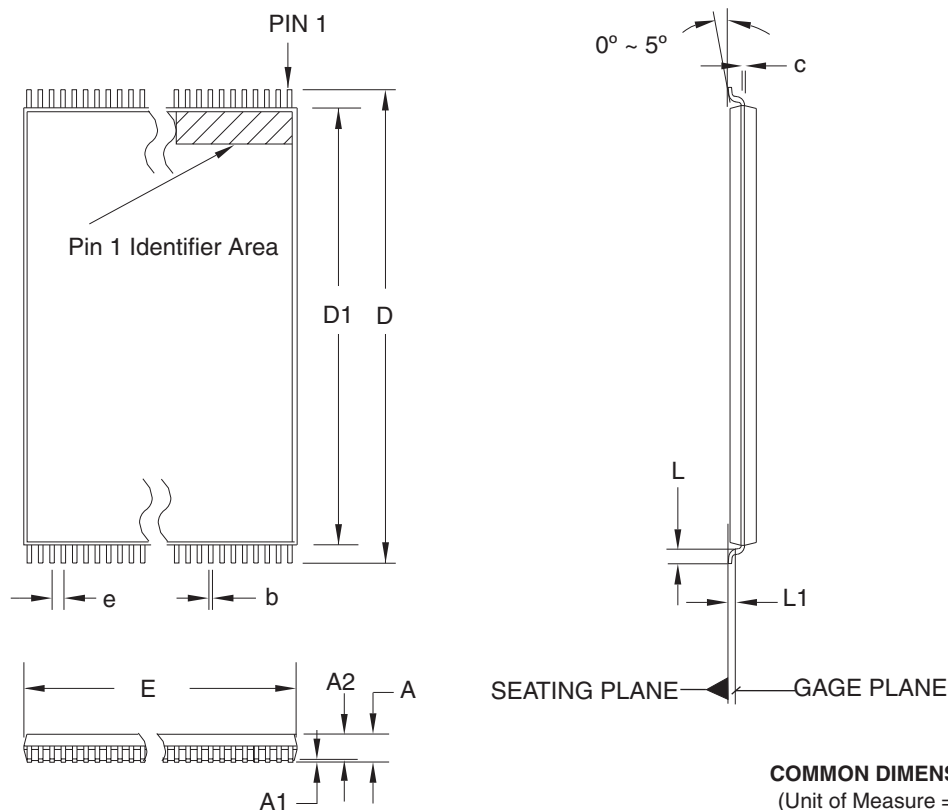
28S

**REV.**

B



## 20.4 28T – TSOP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN        | NOM   | MAX   | NOTE   |
|--------|------------|-------|-------|--------|
| A      | —          | —     | 1.20  |        |
| A1     | 0.05       | —     | 0.15  |        |
| A2     | 0.90       | 1.00  | 1.05  |        |
| D      | 13.20      | 13.40 | 13.60 |        |
| D1     | 11.70      | 11.80 | 11.90 | Note 2 |
| E      | 7.90       | 8.00  | 8.10  | Note 2 |
| L      | 0.50       | 0.60  | 0.70  |        |
| L1     | 0.25 BASIC |       |       |        |
| b      | 0.17       | 0.22  | 0.27  |        |
| c      | 0.10       | —     | 0.21  |        |
| e      | 0.55 BASIC |       |       |        |

- Notes:
1. This package conforms to JEDEC reference MO-183.
  2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
  3. Lead coplanarity is 0.10 mm maximum.

12/06/02



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**28T**, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline  
Package, Type I (TSOP)

### DRAWING NO.

28T

### REV.

C



## Headquarters

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**Atmel Corporation**  
2325 Orchard Parkway  
San Jose, CA 95131  
USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## International

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**Atmel Asia**  
Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

**Atmel Europe**  
Le Krebs  
8, Rue Jean-Pierre Timbaud  
BP 309  
78054 Saint-Quentin-en-  
Yvelines Cedex  
France  
Tel: (33) 1-30-60-70-00  
Fax: (33) 1-30-60-71-11

**Atmel Japan**  
9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Product Contact

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**Web Site**  
[www.atmel.com](http://www.atmel.com)

**Technical Support**  
[eprom@atmel.com](mailto:eprom@atmel.com)

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