GENLINX™ GS9002A
Serial Digital Encoder

DATA SHEET

NOT RECOMMENDED FOR NEW DESIGNS

FEATURES

- **fully compatible with SMPTE-259M serial digital standard**
- **supports up to four serial bit rates to 400 Mb/s**
- **accepts 8 bit and 10 bit TTL and CMOS compatible parallel data inputs**
- **$X^9 + X^4 + 1$ scrambler, NRZI converter and sync detector may be disabled for transparent data transmission**
- **pseudo-ECL serial data and clock outputs**
- **single +5 or -5 volt supply**
- **713 mW typical power dissipation (including ECL pull-down loads).**
- **44 pin PLCC packaging**
- **Pb-free and Green**

APPLICATIONS

- $4f_{SC}$, 4:2:2 and 360 Mb/s serial digital interfaces for Video cameras, VTRs, Signal generators

ORDERING INFORMATION

Part Number	Package	Temperature	Pb-Free and Green
GS9002ACPM	44 Pin PLCC	o°C to 70°C	No
GS9002ACPME3	44 Pin PLCC	o°C to 70°C	Yes

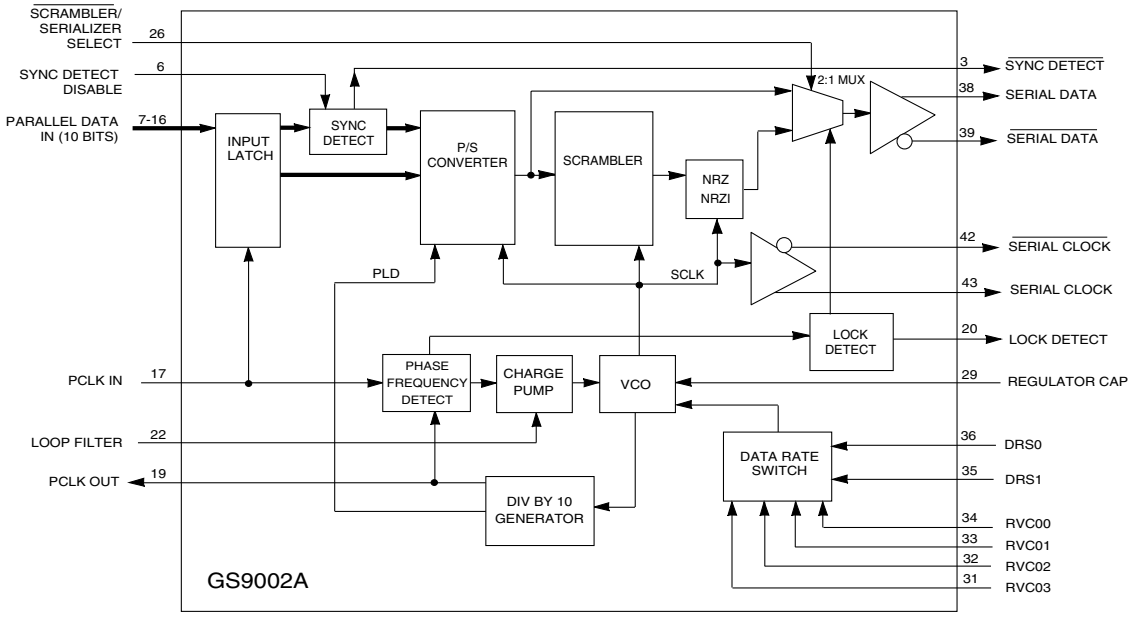
DEVICE DESCRIPTION

The GS9002A is a monolithic bipolar integrated circuit designed to serialize SMPTE 125M and SMPTE 244M bit parallel digital signals as well as other 8 or 10 bit parallel formats. This device performs the functions of sync detection, parallel to serial conversion, data scrambling (using the $X^9 + X^4 + 1$ algorithm), 10x parallel clock multiplication and conversion of NRZ to NRZI serial data. It supports any of four selectable serial data rates from 100 Mb/s to over 360 Mb/s. The data rates are set by resistors and are selected by an on-board 2:4 decoder having two TTL level input address lines.

Other features such as a sync detector output, a sync detector disable input, and a lock detect output are also provided. The $X^9 + X^4 + 1$ scrambler and NRZ to NRZI converter may be bypassed to allow the output of the parallel to serial converter to be directly routed to the output drivers.

The GS9002A provides pseudo-ECL outputs for the serial data and serial clock as well as a single-ended pseudo-ECL output of the regenerated parallel clock.

The GS9002A directly interfaces with cable drivers GS9007A, GS9008A and GS9009A. The device requires a single +5 volt or -5 volt supply and typically consumes 713 mW of power while driving 100 Ω loads. The 44 pin PLCC packaging assures a small footprint for the complete encoder function.



Patent No.5,357,220

FUNCTIONAL BLOCK DIAGRAM

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GS9002A - ENCODER DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 70°C unless otherwise shown

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage		V_S	Operating Range	4.75	5.0	5.25	V	
Power Consumption		P_D	SDO/$\overline{SDO}$ connected to (V_{CC}-2V) thru 100ý resistors, PCK OUT connected to V_{EE} via 1kΩ	-	690	870	mW	
			Same as above with SCK/$\overline{SCK}$ also connected to (V_{CC}-2V) thru 100Ω resistors.	-	710	900	mW	
Supply Current		I_S	SDO/$\overline{SDO}$ connected to (V_{CC}-2V) thru 100ý resistors, PCK OUT connected to V_{EE} via 1kΩ	-	155	190	mA	
			Same as above with SCK/$\overline{SCK}$ to (V_{CC}-2V) V thru 100Ω resistors.	-	170	205	mA	see Figure 15
TTL Inputs-HIGH		V_{IHmin}	T_A = 25°C	2.0	-	-	V	
TTL Inputs-LOW		V_{ILmax}	T_A = 25°C	-	-	0.8	V	
Logic Input Current		I_{INmax}		-	2.5	10	µA	
TTL Outputs-HIGH		V_{OHmin}	T_A = 25°C	2.4	-	-	V	
TTL Outputs-LOW		V_{OLmax}	T_A = 25°C	-	-	0.5	V	
Sync Detect O/P		I_{OSYNC}		-	-	4.0	mA	SINK & SOURCE
Serial Outputs	High	V_{OH}	T_A=25°C, R_L=100Ω to V_{CC}-2V	-0.875	-	-0.7	V	with respect to V_{CC}
(SDO & SCK)	Low	V_{OL}	(V_{CC}-2V)	-1.8	-	-1.5	V	

GS9002A - ENCODER AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 70°C, $V_{LOOP\ FILTER}$ =2.6 V unless otherwise shown,

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Serial Data Outputs (SDO and $\overline{SDO}$)	bit rates	BR_{SDO}	R_L = 100Ω to (V_{CC}-2 volts) T_A = 25°C	100	-	400	Mb/s	
	signal swing	V_{SDO}		700	850	1000	mV p-p	
	rise/fall times	t_R, t_F		-	500	-	ps	20% - 80%
	jitter	$t_{J(SDO)}$	143 Mb/s	-	400	-	ps p-p	see Note 1
			270 Mb/s	-	300	-	ps p-p	see Fig. 16
Serial Clock Outputs (SCK and $\overline{SCK}$)	frequency	f_{SCK}	R_L = 100Ω to (V_{CC}-2 volts)	100	-	400	MHz	see Fig. 12, 13
	signal swing	V_{SCK}		-	800	-	mV p-p	see Fig. 14
Serial Data to Clock Timing		t_D	See Figure 9	-	1.4	-	ns	Data lags Clock
Lock Time		t_{LOCK}	$C_{LOOP\ FILT}$ = 0.1µF $R_{LOOP\ FILT}$ = 3.9kΩ	-	1	1.2	ms	
Parallel Clock Output (PCK OUT)	frequency	f_{PCKO}	R_L = 1kΩ to V_{EE}	10	-	40	MHz	$f_{PCKO} = f_{SCK}/10$
	signal swing	V_{PCKO}		-	800	-	mV p-p	
	rise/fall times	t_R, t_F		-	700	-	ps	20% - 80%
	jitter	t_{JPCKO}		-	400	-	ps p-p	
Parallel Data & Clock Inputs	risetime	t_R	T_A = 25°C	500	-	-	ps	
	setup	t_{SU}		3	-	-	ns	
	hold	t_{HOLD}		3	-	-	ns	

NOTE 1: Measured using PCK-IN as trigger source on 1GHz analog oscilloscope.

NOT RECOMMENDED FOR NEW DESIGNS

≤

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage	5.5 V
Input Voltage Range (any input)	$-V_{EE} < V_I < V_{CC}$
DC Input Current (any one input)	10 mA
Power Dissipation (V_S = 5.25 V)	1 W
Operating Temperature Range	$0^{\circ}C \le T_A \le 70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C \le T_S \le 150^{\circ}C$
Lead Temperature (soldering 10 seconds)	260°C

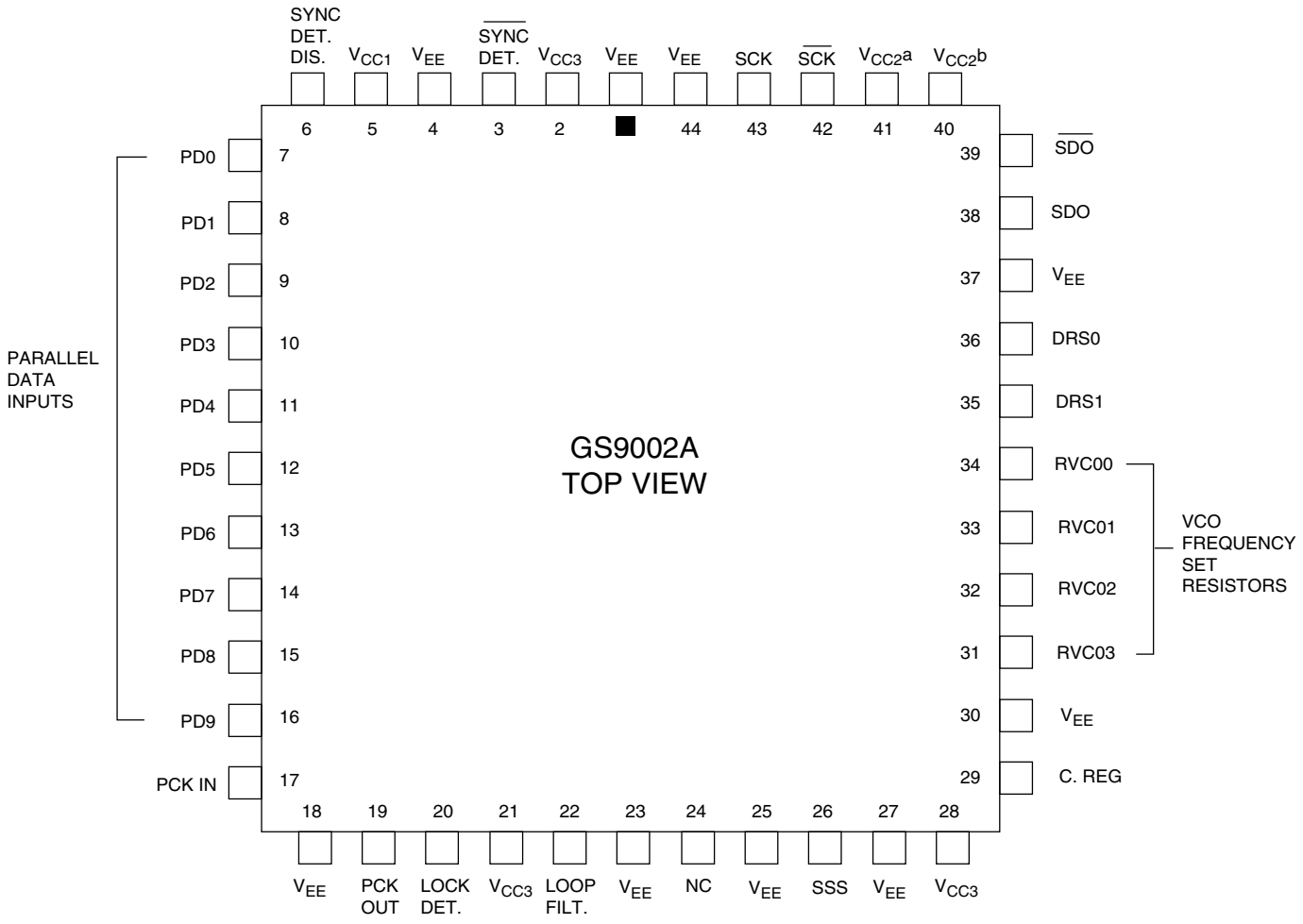


Fig. 1 GS9002A Encoder Pin Connections

NOT RECOMMENDED FOR NEW DESIGNS

GS9002A Serial Digital Encoder - Detailed Device Description

The GS9002A Encoder is a bipolar integrated circuit used to convert parallel data into a serial format according to the SMPTE 259M standard. The device encodes both eight and ten bit TTL-compatible parallel signals producing serial data rates up to 400 Mb/s. It operates from a single five volt supply and is packaged in a 44 pin PLCC.

Functional blocks within the device include the input latches, sync detector, parallel to serial converter, scrambler, NRZ to NRZI converter, ECL output buffers for data and clock, PLL for 10x parallel clock multiplication and lock detect.

The parallel data (PD0-PD9) and parallel clock (PCK-IN) are applied via pins 7 through 17 respectively.

Sync Detector

The Sync Detector looks for the reserved words 000-003 and 3FC-3FF, in ten bit Hex, or 00 and FF in eight bit Hex, used in the TRS-ID sync word. When the occurrence of either all zeros or ones at inputs PD2-PD9 is detected, the lower two bits PD0 and PD1 are forced to zeros or ones, respectively. This makes the system compatible with eight or ten bit data. For non - SMPTE standard parallel data, a logic input, Sync Disable (6) is available to disable this feature.

Scrambler

The Scrambler is a linear feedback shift register used to pseudo-randomize the incoming serial data according to the fixed polynomial (X^9+X^4+1). This minimizes the DC component in the output serial data stream. The NRZ to NRZI converter uses another polynomial (X+1) to convert a long sequence of ones to a series of transitions, minimizing polarity effects.

Phase Locked Loop

The PLL performs parallel clock multiplication and provides the timing signal for the serializer. It is composed of a phase/frequency detector, charge pump, VCO and a divide-by-ten counter.

The phase/frequency detector allows a wider capture range and faster lock time than that which can be achieved with a phase discriminator alone. The discrimination of frequency also eliminates harmonic locking. With this type of discriminator, the PLL can be over-damped for good stability without sacrificing lock time.

The charge pump delivers a 'charge packet' to the loop filter which is proportional to the system phase error. Internal voltage clamps are used to constrain the loop filter voltage between approximately 1.8 and 3.4 volts.

The VCO, constructed from a current-controlled multivibrator, features operation in excess of 400 Mb/s and a wide pull range (≈±40% of centre frequency).

VCO Centre Frequency Selection

The wide VCO pull range allows the PLL to compensate for variations in device processing, temperature variations and changes in power supply voltage, without external adjustment. A single external resistor is used to set the VCO current for each of four centre frequencies as selected by a two bit code through a 2:4 decoder.

The current setting resistors are connected to the RVCO0 through RVCO3 inputs (34, 33, 32 and 31). The decoder inputs DRS0 and DRS1 (36, 35) are TTL compatible inputs and select the four resistors according to the following truth table.

DRS1	DRS0	Resistor Selected
0	0	RVCO0 (34)
0	1	RVCO1 (33)
1	0	RVCO2 (32)
1	1	RVCO3 (31)

A 2:1 multiplexer (MUX) selects either the direct data from the P/S Converter (Serializer) or the NRZI data from the Scrambler. This MUX is controlled by the Scrambler/Serializer Select (SSS) input pin 26. When this input is LOW the MUX selects the Scrambler output. (This is the mode used for SMPTE 259M data). When this input is HIGH the MUX directly routes the serialized data to the output buffer with no scrambling or NRZ to NRZI conversion.

The lock detect circuit disables the serial data output when the loop is not locked by turning off the 2:1 MUX. The Lock Detect output is available from pin 20 and is HIGH when the loop is locked.

The true and complement serial data, SDO and $\overline{SDO}$ are available from pins 38 and 39 while the true and complement serial clock, SCK and $\overline{SCK}$ are available from pins 43 and 42 respectively. If the serial clock is not used pins 43 and 42 can be connected to V_{CC}.

The regenerated parallel clock (PCK OUT) is available at pin 19. This output is a single ended pseudo-ECL output requiring a pull down resistor. If regenerated parallel clock is not used pin 19 can be connected to V_{CC}.

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GS9002A PIN DESCRIPTIONS

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1	V_{EE}		Power Supply: Most negative power supply connection.
2	V_{CC3}		Power Supply: Most positive power supply connection for the PLL and scrambler.
3	SYNC DET.	O	TTL output level that detects the occurrence of all zero's or all one's at inputs PD2-PD9 and pulses LOW for three PCK-IN durations. Used to detect SMPTE 259M reserved words (000-003 and 3FC-3FF) in TRS sync word. Parallel data bits PD0 and PD1 are set Low or High when PD2 - PD9 are Low or High respectively.
4	V_{EE}		Power Supply: Most negative power supply connection.
5	V_{CC1}		Power Supply: Most positive power supply connection for the input data latches and serializer.
6	SYNC DET. DISABLE	I	TTL level input that disables the internal Sync Detector when HIGH. This allows the GS9002 to serialize 8 or 10 bit non - SMPTE Standard parallel data.
7-16	PD0-PD9	I	TTL level inputs of the parallel data words. PD0 is the LSB and PD9 is the MSB.
17	PCK-IN	I	TTL level input of the Parallel Clock.
18	V_{EE}		Power Supply: Most negative power supply connection.
19	PCK OUT	O	Pseudo-ECL output representing the re-clocked Parallel Clock and is derived from the internal VCO. The VCO is divided by 10 in order to produce this output.
20	LOCK DET.	O	TTL level output which goes HIGH when the internal PLL is locked.
21	V_{CC3}		Power Supply: Most positive power supply connection for the PLL and scrambler.
22	LOOP FILT.	I	Connection for the R-C loop filter components. The loop filter sets the PLL loop parameters.
23	V_{EE}		Power Supply: Most negative power supply connection.
24	NC		
25	V_{EE}		Power Supply: Most negative power supply connection.
26	SSS	I	Scrambler/Serializer Select. TTL level input that selects scrambled NZRI output when logic LOW or direct serializer output when logic HIGH.
27	V_{EE}		Power Supply: Most negative power supply connection.
28	V_{CC3}		Power Supply: Most positive power supply connection for the PLL and scrambler.
29	C_{REG}	I	Compensation RC network for internal voltage regulator that requires decoupling with a series 0.1µF capacitor and 820Ω resistor. Components should be located as close as possible to the pin.
30	V_{EE}		Power Supply: Most negative power supply connection.
31	R_{VCO3}	I	VCO Resistor 3: Analog current input used to set the centre frequency of the VCO when the two Data Rate Select bits (pins 35 and 36) are both set to logic 1. A resistor is connected from this pin to V_{EE}.
32	R_{VCO2}	I	VCO Resistor 2: Analog current input used to set the centre frequency of the VCO when the Data Rate Select Bit 0 (pin 36) is set to logic 0 and the Data Rate Select Bit 1 (pin 35) is set to logic 1. A resistor is connected from this pin to V_{EE}.
33	R_{VCO1}	I	VCO Resistor 1: Analog current input used to set the centre frequency of the VCO when the Data Rate Select Bit 0 (pin 36) is set to logic 1 and the Data Rate Select Bit 1 (pin 35) is set to logic 0. A resistor is connected from this pin to V_{EE}.
34	R_{VCO0}	I	VCO Resistor 0: Analog current input used to set the centre frequency of the VCO when the two Data Rate Select bits (pins 35 and 36) are both set to logic 0. A resistor is connected from this pin to V_{EE}.
35,36	DRS0, 1	I	TTL level inputs to the internal 2:4 demultiplexer used to select one of four VCO frequency setting resistors (R_{VCO0} - R_{VCO3}). (See above)

NOT RECOMMENDED FOR NEW DESIGNS

GS9002A PIN DESCRIPTIONS (Continued)

PIN NO	SYMBOL	TYPE	DESCRIPTION
37	V_{EE}		Power Supply: Most negative power supply connection.
38,39	SDO/$\overline{SDO}$	O	Serial Data Outputs (true and inverse). Pseudo-ECL differential outputs representing the serialized data. These outputs require 390Ω pull down resistors.
40	V_{CC2b}		Power Supply: Most positive power supply connection for the Serial Data ECL output buffers.
41	V_{CC2a}		Power Supply: Most positive power supply connection for the Serial Clock ECL output buffers.
42,43	$\overline{SCK}$/SCK	O	Serial Clock Outputs (inverse and true). Pseudo-ECL differential outputs of the Serial Clock (10x Parallel Clock). These outputs require 390Ω pull-down resistors.
44	V_{EE}		Power Supply: Most negative power supply connection.

INPUT / OUTPUT CIRCUITS

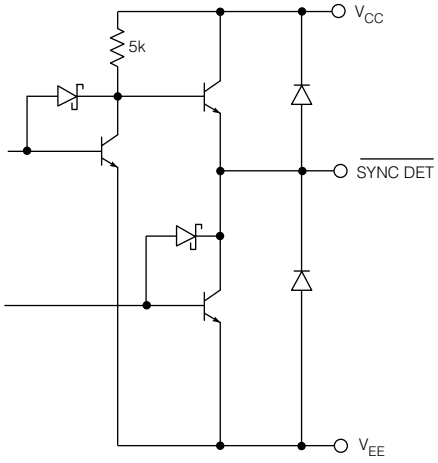


Fig. 2 Pin No. 3
Sync Detect

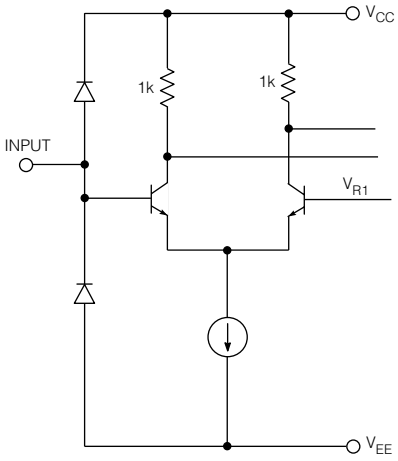


Fig. 3 Pins No. 6, 7 - 16, 17,26
Sync Disable, Parallel Data, Parallel Clock,
Scrambler/Serializer Select

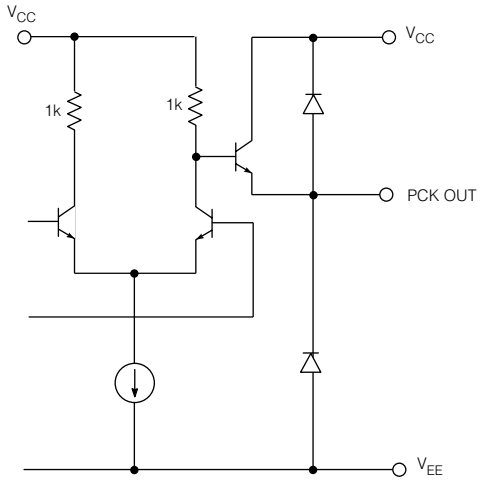


Fig. 4 Pin No. 19
Parallel Clock Out

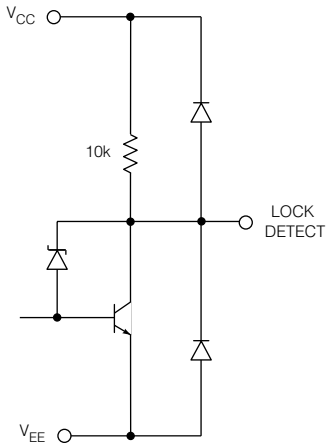


Fig. 5 Pin No. 20
Lock Detect

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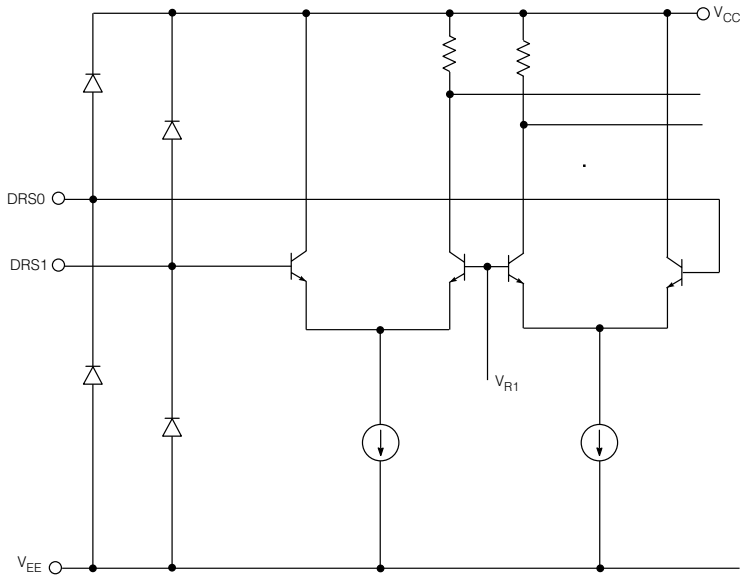


Fig. 6 Pins No. 35, 36
Data Rate Select

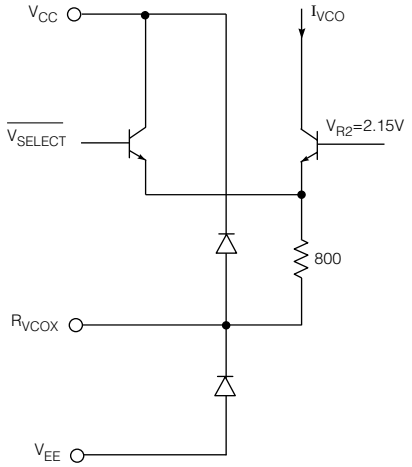


Fig. 7 Pins No. 31 - 34
Frequency Setting Registors R_{VCO0}-R_{VCO3}

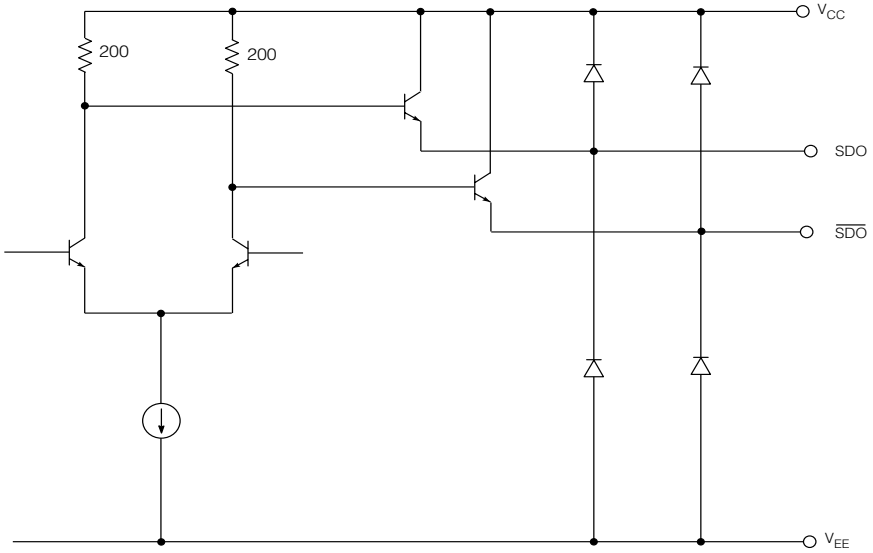


Fig. 8 Pins No. 38, 39, 42, 43
Serial Outputs (Data & Clock)

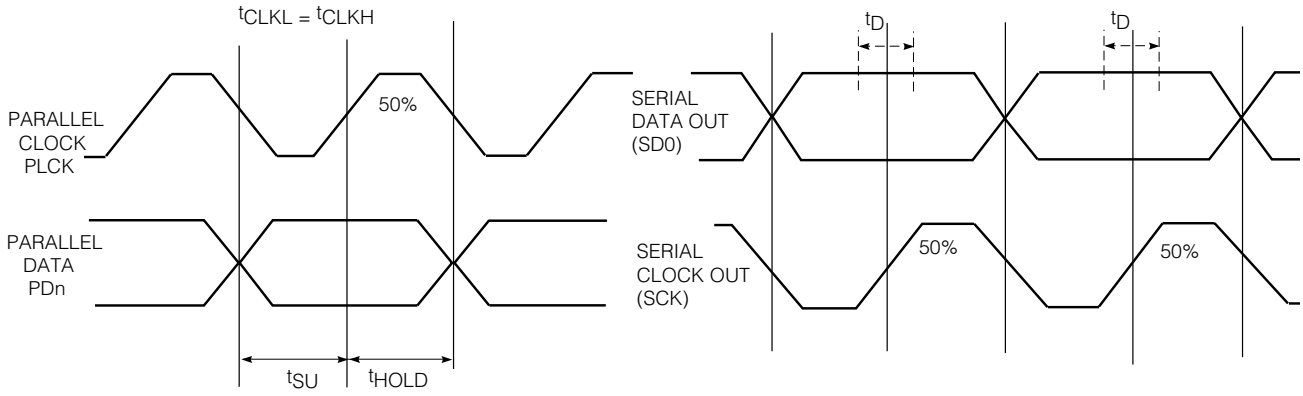


Fig. 9 Waveforms

NOT RECOMMENDED FOR NEW DESIGNS

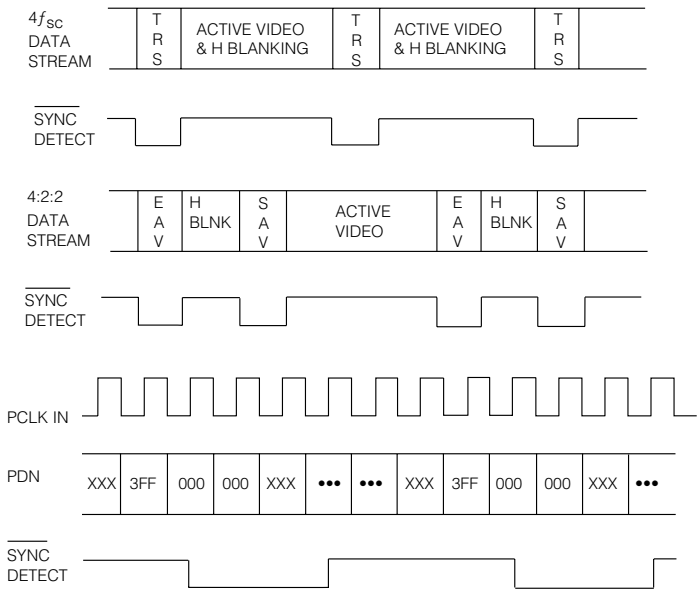
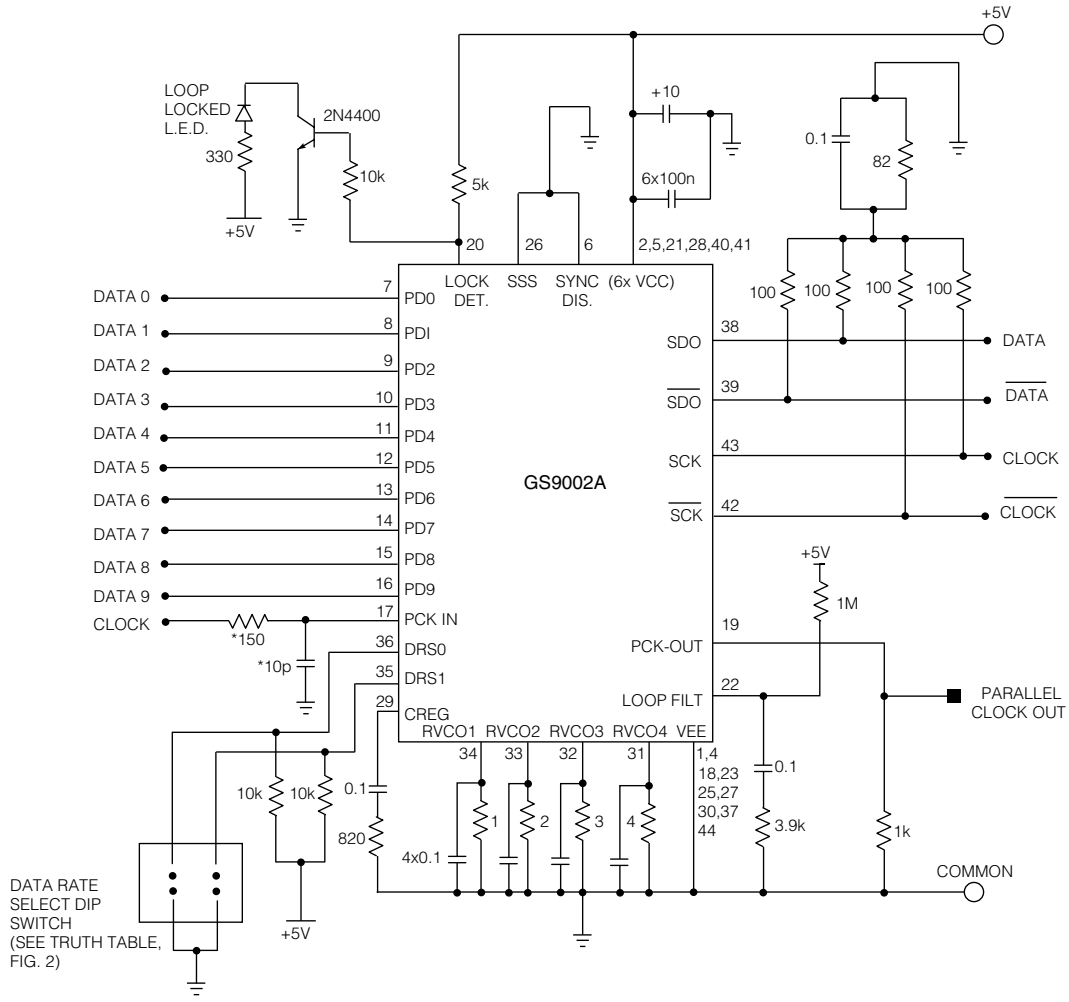


Fig. 10 Timing Diagram



NOTES: Resistors 1, 2, 3 and 4 are used to set the VCO centre frequency. For 143/177 Mb/s ≈ 6kΩ, 270 Mb/s ≈ 2.7kΩ, 360 Mb/s ≈ 1.8kΩ
All resistors in ohms, all capacitors in microfarads unless otherwise stated. ■— represent test points.

* This RC network is used to slow down fast PCLK risetimes (≤ 500ps). It is not required if risetimes exceed 500ps.

Fig. 11 GS9002A Test Circuit

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TYPICAL PERFORMANCE CURVES (V_S = 5V, T_A = 25° C unless otherwise shown)

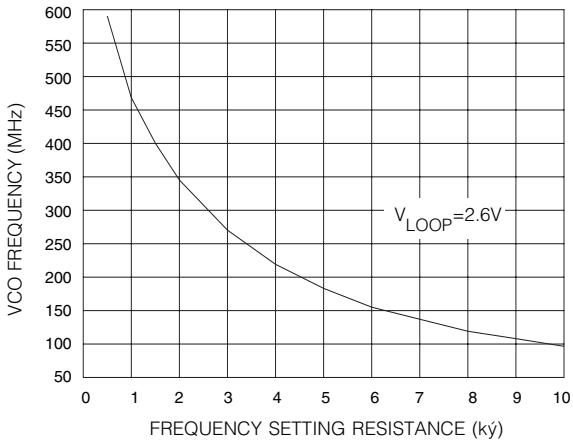


Fig. 12 VCO Frequency

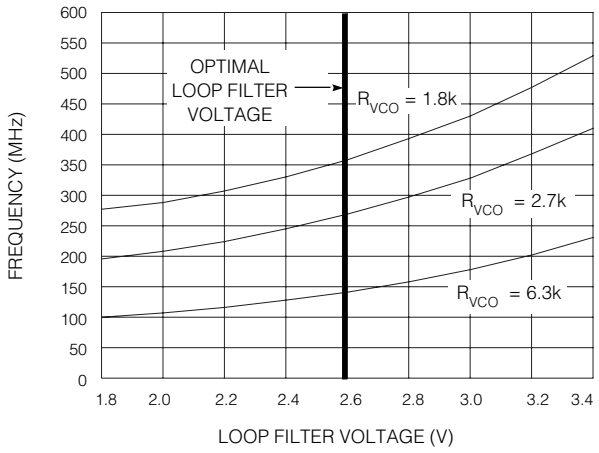


Fig. 13 VCO Frequency vs Loop Filter Voltage

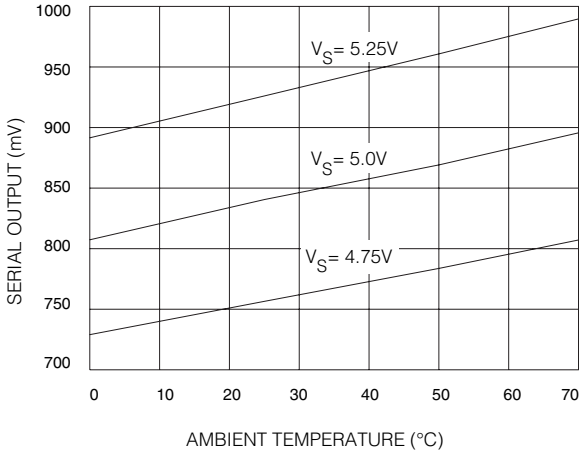


Fig. 14 Serial Output Level (Data & Clock)

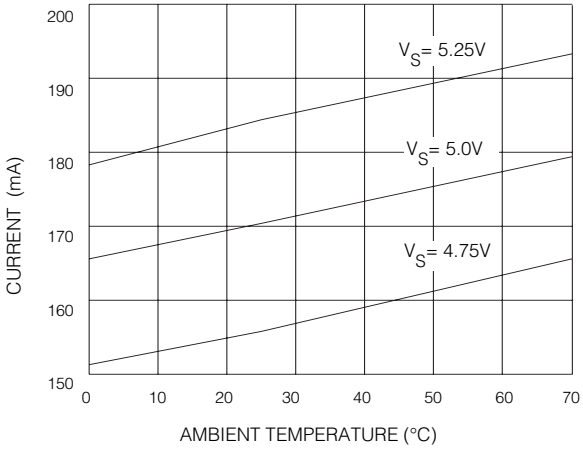


Fig. 15 Supply Current

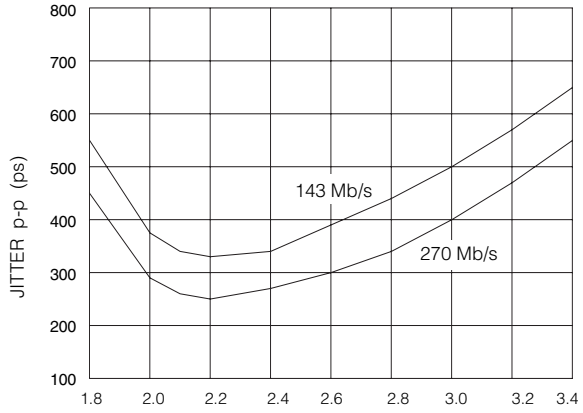
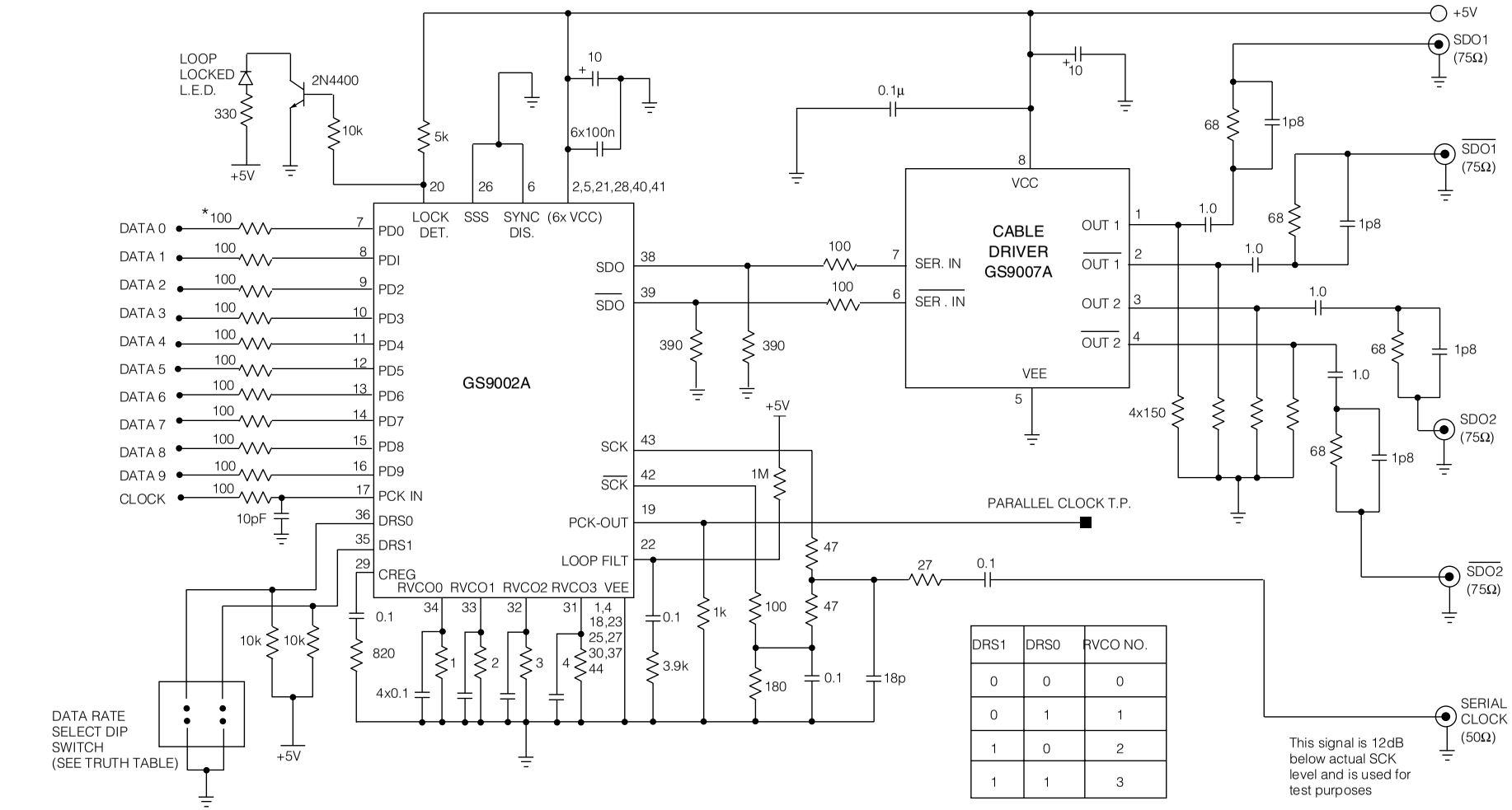


Fig. 16 Output Jitter

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DRS1	DRS0	RVCO NO.
0	0	0
0	1	1
1	0	2
1	1	3

DATA RATE SELECT TRUTH TABLE

NOTES: Resistors 1, 2, 3 and 4 are used to set the VCO centre frequency. See Figures 12 and 13.
All resistors in ohms, all capacitors in microfarads unless otherwise stated. ■— represent test points.
* These resistors are used to slow down fast INPUT edges (≤500ps) and prevent the input signals from ringing below the V_{EE} rail.

Fig. 17 ***GENLINX***™ Serial Digital Chipset
GS9002/7A Application Circuit

NOT RECOMMENDED FOR NEW DESIGNS

APPLICATION CIRCUIT

Figure 17 shows a typical application circuit of the GS9002A driving a GS9007A cable driver.

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REVISION NOTES

Added lead-free and green information.

For latest product information, visit www.gennum.com

CAUTION

ELECTROSTATIC

SENSITIVE DEVICES

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