2.5 V/3.3 V PECL/ECL 1:2 Fanout Buffer

FEATURES

- 1:2 PECL/ECL Fanout Buffer
- Operating Range
  - PECL: V_{CC} = 2.375 V to 3.8V With V_{EE} = 0 V
  - NECL: V_{CC} = 0 V With V_{EE} = –2.375V to –3.8 V
- Open Input Default State
- Support for Clock Frequencies > 3.0 GHz
- 240 ps Typical Propagation Delay
- Deterministic Output Value for Open Input Conditions
- Q Output Will Default Low When Input Open or at V_{EE}
- Built-in Temperature Compensation
- Drop in Compatible to MC10LVEP11, MC100LVEP11
- LVDS Input Compatible

DESCRIPTION

The SN65LVEP11 is a differential 1:2 PECL/ECL fanout buffer. The device includes circuitry to maintain known logic levels when the inputs are in an open condition. Single-ended clock input operation is limited to V_{CC} ≥ 3 V in PECL mode, or V_{EE} ≤ 3 V in NECL mode. The device is housed in an industry-standard SOIC-8 package and is also available in TSSOP-8 package option.

PINOUT ASSIGNMENT

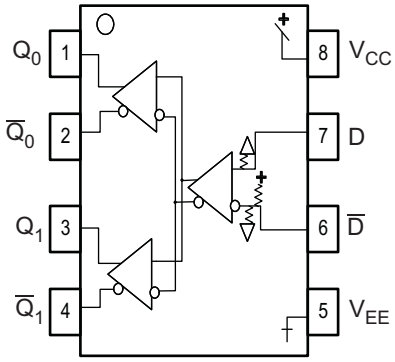


Table 1. PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	PECL/ECL data inputs
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	PECL/ECL outputs
V_{CC}	Positive supply
V_{EE}	Negative supply

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65LVEP11D	SN65LVEP11	SOIC	NiPdAu
SN65LVEP11DGK	SN65LVEP11	SOIC-TSSOP	NiPdAu

(1) Leaded device option not initially available; contact TI sales representative for further information.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITION	VALUE	UNIT
Absolute PECL mode supply voltage VCC	V_{EE} = 0 V	6	V
Absolute NECL mode supply voltage, V_{EE}	V_{CC} = 0 V	–6	V
PECL mode input voltage	V_{EE} = 0 V; $V_I \le V_{CC}$	6	V
NECL mode input voltage	V_{CC} = 0 V; $V_I \ge V_{EE}$	–6	V
Output current	Continuous	50	mA
	Surge	100	mA
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to Board Thermal Resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
θ_{JC}	Junction-to Case Thermal Resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Internal input pull down resistor	75 kΩ
Internal input pull up resistor	37.5 kΩ
Moisture sensitivity level	Level 1
Flammability rating (Oxygen Index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD-HBM	4 kV
ESD-machine model	200 V
ESD-charged device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

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PECL DC CHARACTERISTICS(1) (V_{CC} = 2.5 V; V_{EE} = 0.0 V)(2)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current		28	45		31	45		35	45	mA
V_{OH}	Output HIGH voltage(3)	1355		1605	1355	1425	1605	1335		1605	mV
V_{OL}	Output LOW voltage(3)	555		900	555	759	900	555		900	mV
V_{IH}	Input high voltage (Single-Ended)	1335		1620	1335		1620	1335		1620	mV
V_{IL}	Input low voltage (Single-Ended)	555		900	555		900	555		900	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential)(4)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH current			150			150			150	µA
I_{IL}	Input LOW current (D)	0.5			0.5			0.5			µA
	nput LOW current (–D)	–150			–150			–150			

(1) The device will meet the specifications after the thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to – 1.3 V.
(3) All loading with 50 Ω to V_{CC} –2 V.
(4) $V_{IHCMR\ min}$ varies 1:1 with V_{EE}, $V_{IHCMR\ max}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single ended input clock pin operation is limited to $V_{CC} \geq 3.0$ V in PECL mode.

PECL DC CHARACTERISTICS(1) (V_{CC} = 3.3 V; V_{EE} = 0.0 V)(2)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current		28	45		32	45		36	45	mA
V_{OH}	Output HIGH voltage(3)	2155		2405	2155	2221	2405	2155		2405	mV
V_{OL}	Output LOW voltage(3)	1355		1700	1355	1543	1700	1355		1700	mV
V_{IH}	Input high voltage (Single-Ended)(4)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input low voltage (Single-Ended)(4)	1355		1700	1355		1700	1355		1700	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential)(5)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH current			150			150			150	µA
I_{IL}	Input LOW current (D)	0.5			0.5			0.5			µA
	nput LOW current (–D)	–150			–150			–150			

(1) The device will meet the specifications after the thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are specified only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously
(2) Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.5 V.
(3) All loading with 50 Ω to V_{CC} – 2 V.
(4) Single Ended input clock pin operation is limited to VCC ≥ 3 V in PECL mode.
(5) $V_{IHCMR\ min}$ varies 1:1 with V_{EE}, $V_{IHCMR\ max}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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NECL DC CHARACTERISTICS(1) (V_{CC} = 0.0 V; V_{EE} = –3.8V to –2.375 V)(2)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current		28	45		32	45		36	45	mA
V_{OH}	Output HIGH voltage(3)	–1145		–895	–1145	–1065	–895	–1145		–895	mV
V_{OL}	Output LOW voltage(3)	–1945		–1600	–1945	–1777	–1600	–1945		–1600	mV
V_{IH}	Input high voltage (Single-Ended)(4)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input low voltage (Single-Ended)(4)	–1945		–1600	–1945		–1600	–1945		–1600	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential)(5)	V_{EE}+1.2	V_{EE}+1.2	0.0	V_{EE}+1.2	V_{EE}+1.2	0.0	V_{EE}+1.2	V_{EE}+1.2	0.0	V
I_{IH}	Input HIGH current			150			150			150	µA
I_{IL}	Input LOW current (D)	0.5			0.5			0.5			µA
	nput LOW current (–D)	–150			–150			–150			

(1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously
(2) Input and output parameters vary 1:1 with V_{CC}.
(3) All loading with 50 Ω to V_{CC} – 2 V.
(4) Single Ended input clock pin operation is limited to VCC ≤ –3 V in NECL mode.
(5) $V_{IHCMR\ min}$ varies 1:1 with V_{EE}, $V_{IHCMR\ max}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS(1) (V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = –3.8 V to –2.375 V(2)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency(3) (see Figure 6)		3.8			3.5			3.1		GHz
t_{PLH}/t_{PHL}	Propagation delay to output differential (CLK, Q, –Q)	200		300	200		300	200		300	ps
t_{SKEW}	Device skew (Q, –Q)		8			8	15		8	15	ps
	Device to Device Skew (Q, –Q) (4)			25			25			25	
t_{JITTER}	Random clock jitter (RMS) ≤ 1.0 GHz			0.3			0.3			0.3	ps
	Random Clock Jitter (RMS) ≤ 1.5 GHz			0.2			0.2			0.2	
	Random Clock Jitter (RMS) ≤ 2.0 GHz			0.2			0.2			0.2	
	Random Clock Jitter (RMS) ≤ 2.5 GHz			0.2			0.2			0.2	
	Random Clock Jitter (RMS) ≤ 3.0 GHz			0.2			0.2			0.2	
V_{PP}	Input swing Differential Config.	150	800	1200	150		1200	150		1200	mV
t_r/t_f	Output rise/fall times Q, –Q (20%–80%)	100		200	100		200	100		200	ps

(1) The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} –2 V.
(3) The maximum switching frequency measured at the output amplitude of 300 mVpp.
(4) Skew is measured between outputs under identical transitions

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Typical Termination for Output Driver

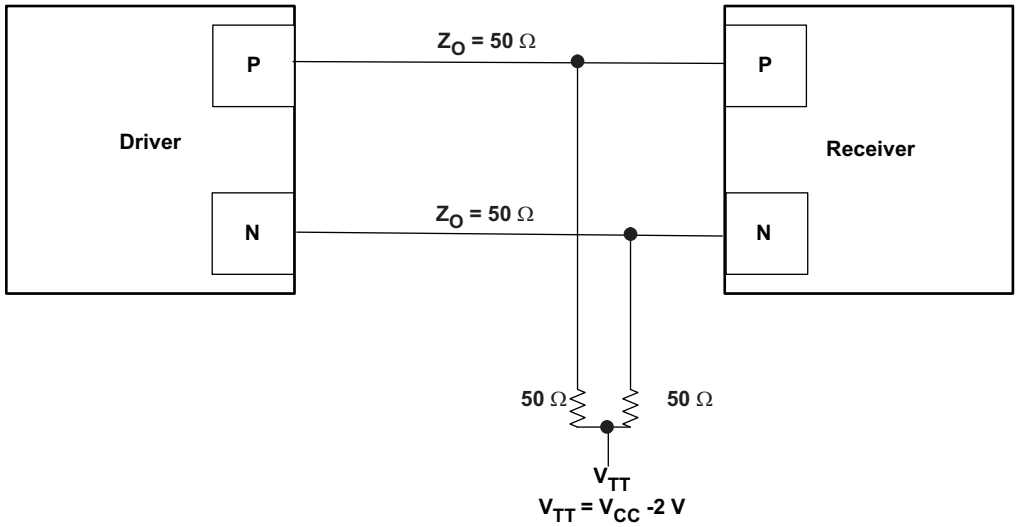


Figure 1. Typical Termination for Output Driver

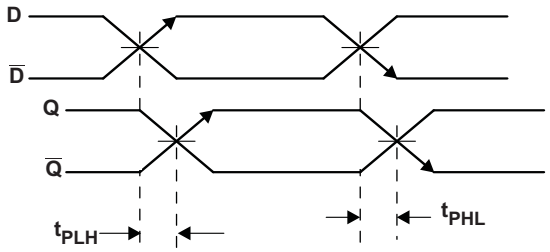


Figure 2. Propagation Delay

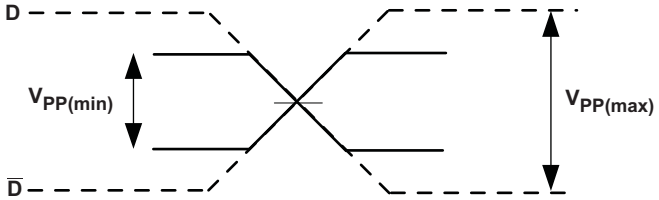


Figure 3. Input Voltage Swing

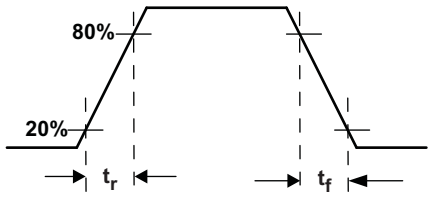


Figure 4. Output Rise and Fall Times

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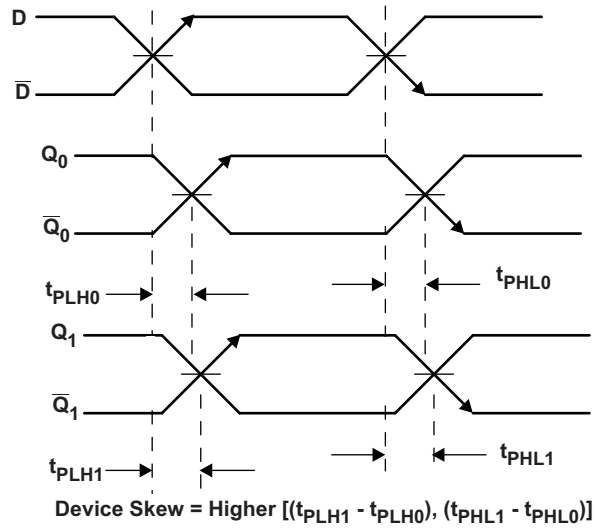


Figure 5. Device Skew

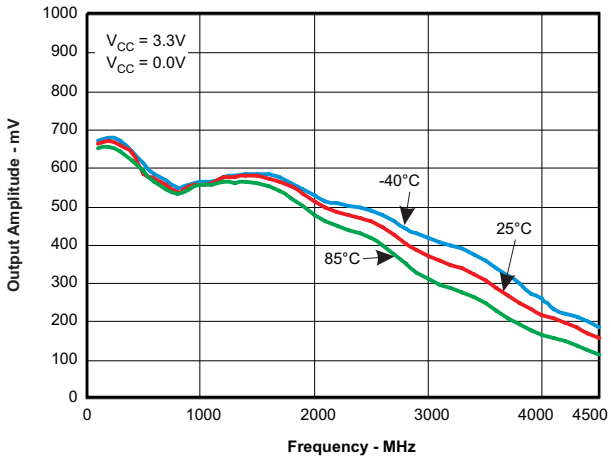


Figure 6. Output Amplitude vs Frequency

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVEP11D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVEP11DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVEP11DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVEP11DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

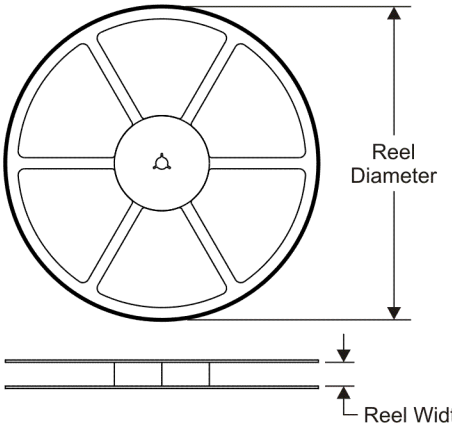
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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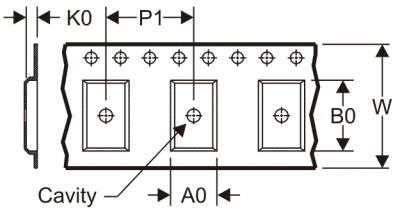
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

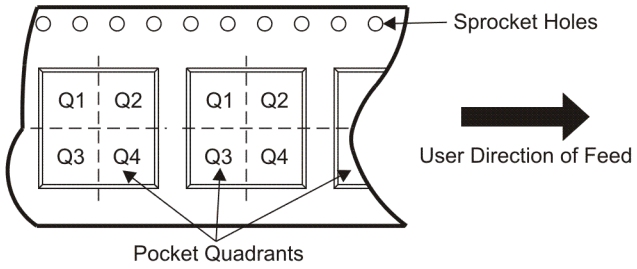


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

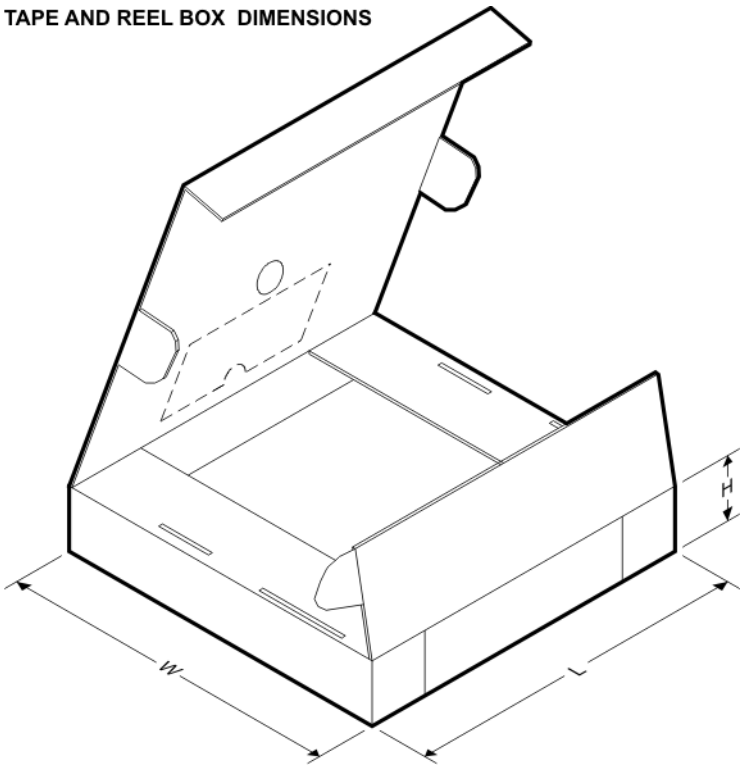
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVEP11DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVEP11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

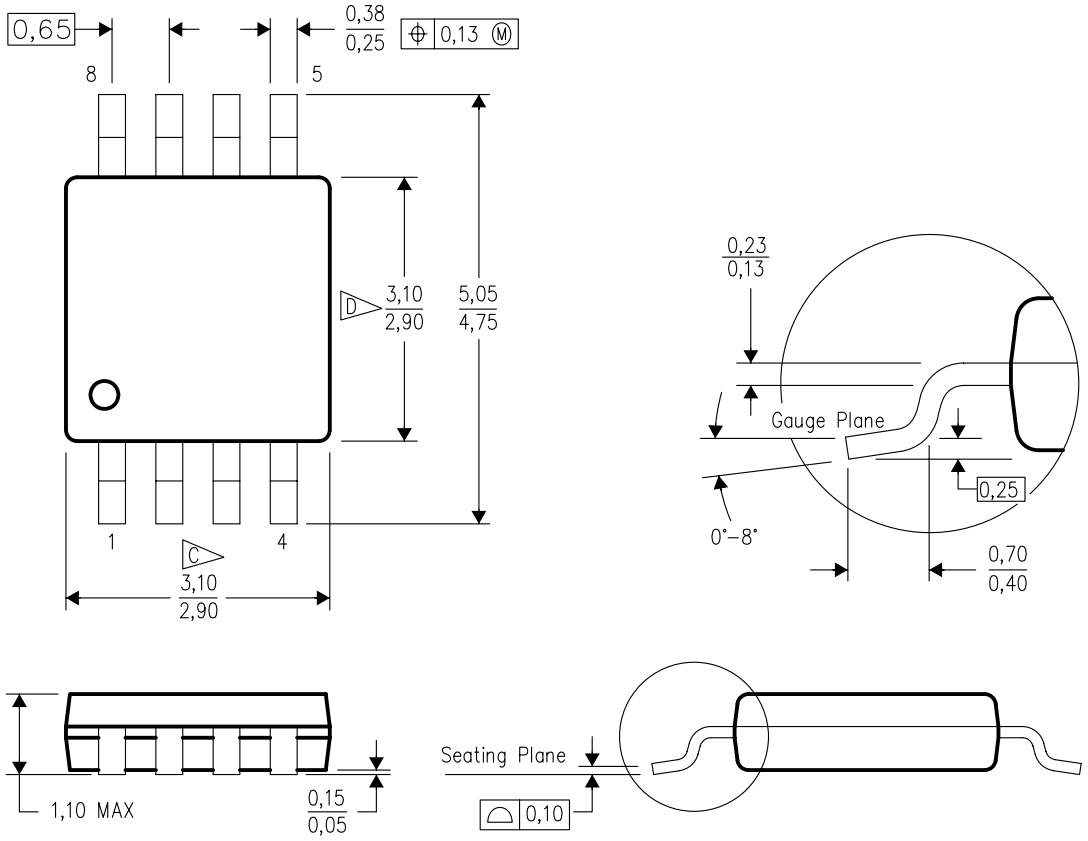
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVEP11DGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
SN65LVEP11DR	SOIC	D	8	2500	346.0	346.0	29.0

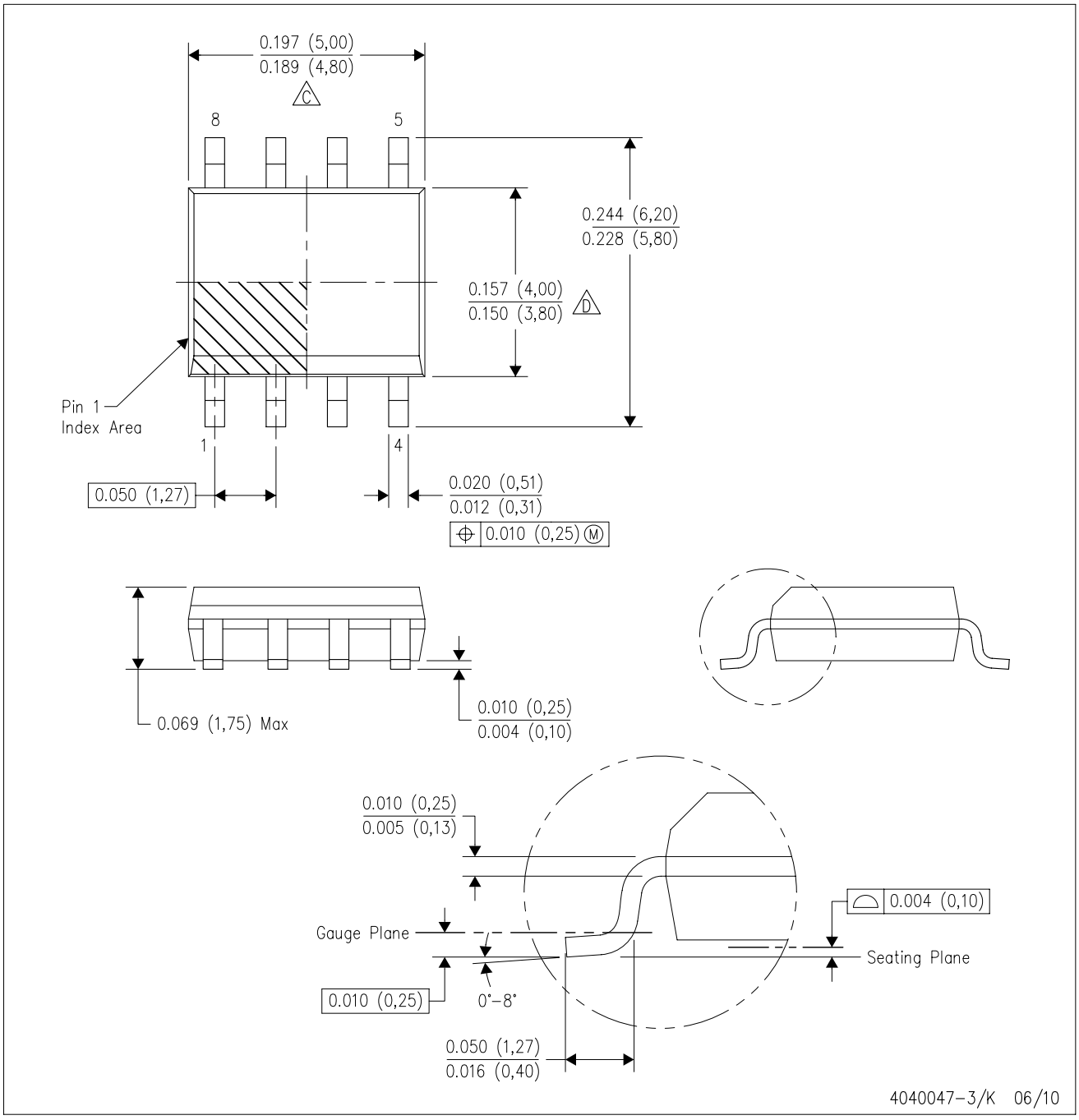
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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