Data Sheet April 3, 2007 FN7362.3

Triple 16x5 Differential Crosspoint Switch Capable of Operation in Single-Ended or Differential Input Modes

The EL4544 is a high bandwidth 16-channel differential RGB to 5-channel RGB single-ended RGB-HV video crosspoint switch with embedded sync extraction. Four 16-channel input muxes, each capable of receiving a complete RGB video signal, and five output muxes, each capable of "seeing" any one of the four RGB inputs. Additionally, the fifth input mux has an overlay "screen on screen" function that can be displayed in conjunction with any of the stacked RGB inputs.

The EL4544 has a fast disable feature to reduce power consumption. The device also provides a presence of signal indicator by looking for syncs on a designated channel.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL4544IGZ (Note)	EL4544IGZ	356 Pin (27x27mm) BGA (Pb-Free)	V356.27x27

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Serial programming of switch array
- Parallel or serial modes
- High Z output disable
- Drives 150Ω loads
- 60MHz 0.1dB gain flatness
- -3dB bandwidth of 300MHz
- Crosstalk rejection: 75dB @ 100MHz
- Channels settle to 5% within 10ns after overlay switching
- 356 pin BGA packaging
- Pb-free plus anneal available (RoHS compliant)

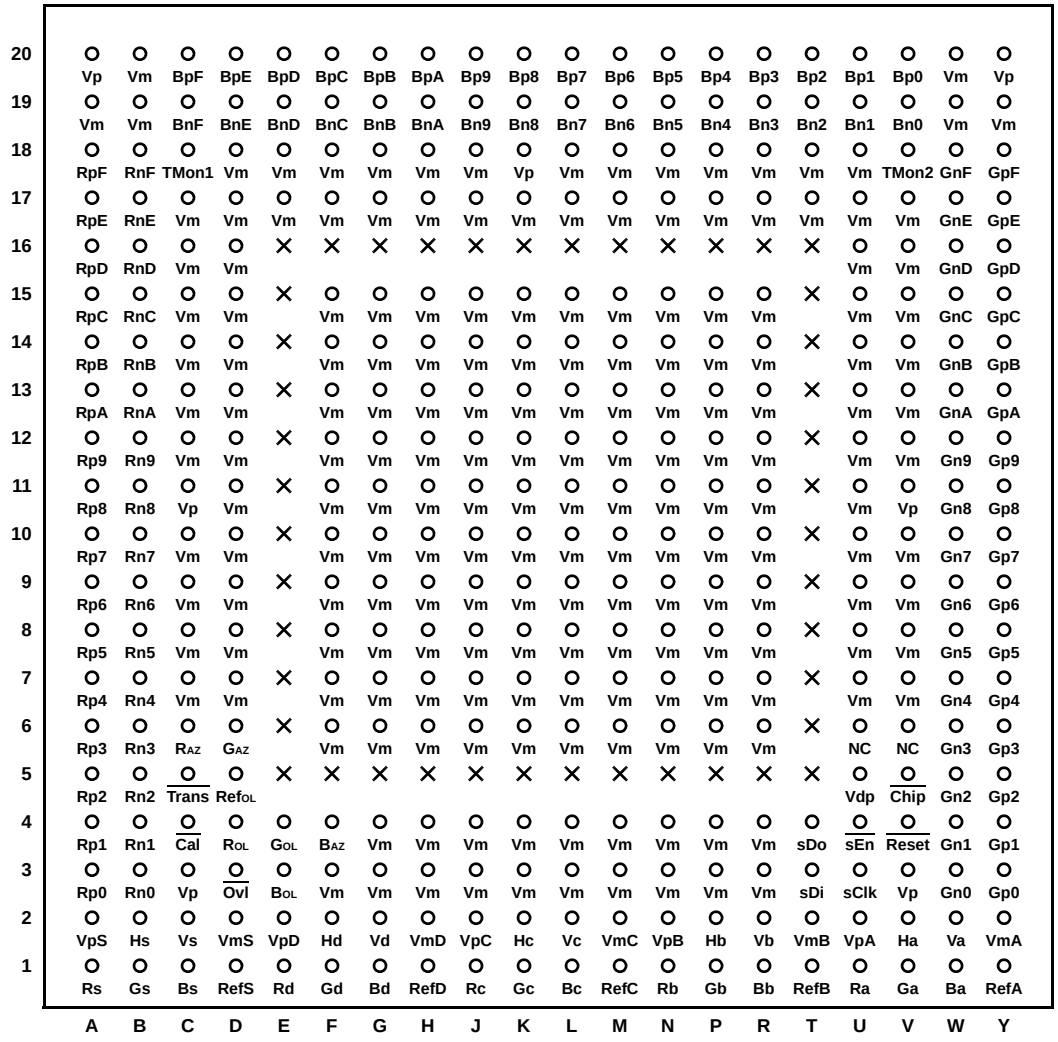
Applications

- Video switching

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright Intersil Americas Inc. 2005-2007. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

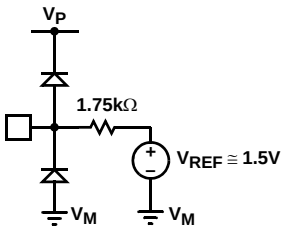
Pinout

EL4544
(356 PIN BGA)
TOP VIEW

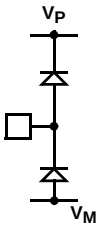


× = EMPTY LOCATION (UNPOPULATED)
O = BALLGRID

Pin Descriptions

PIN NAME	SOLDER BALL	DESCRIPTION	EQUIVALENT CIRCUIT
Rp0	A3	Red plus input 0	 CIRCUIT 1
Rn0	B3	Red minus input 0	Reference Circuit 1
Rp1	A4	Red plus input 1	Reference Circuit 1
Rn1	B4	Red minus input 1	Reference Circuit 1
Rp2	A5	Red plus input 2	Reference Circuit 1
Rn2	B5	Red minus input 2	Reference Circuit 1
Rp3	A6	Red plus input 3	Reference Circuit 1
Rn3	B6	Red minus input 3	Reference Circuit 1
Rp4	A7	Red plus input 4	Reference Circuit 1
Rn4	B7	Red minus input 4	Reference Circuit 1
Rp5	A8	Red plus input 5	Reference Circuit 1
Rn5	B8	Red minus input 5	Reference Circuit 1
Rp6	A9	Red plus input 6	Reference Circuit 1
Rn6	B9	Red minus input 6	Reference Circuit 1
Rp7	A10	Red plus input 7	Reference Circuit 1
Rn7	B10	Red minus input 7	
Vm	MultipleBalls	Analog minus supply	
Vp	C11	Analog plus supply	Reference Circuit 1
Rp8	A11	Red plus input 8	Reference Circuit 1
Rn8	B11	Red minus input 8	Reference Circuit 1
Rp9	A12	Red plus input 9	Reference Circuit 1
Rn9	B12	Red minus input 9	Reference Circuit 1
RpA	A13	Red plus input 10	Reference Circuit 1
RnA	B13	Red minus input 10	Reference Circuit 1
RpB	A14	Red plus input 11	Reference Circuit 1
RnB	B14	Red minus input 11	Reference Circuit 1
RpC	A15	Red plus input 12	Reference Circuit 1
RnC	B15	Red minus input 12	Reference Circuit 1
RpD	A16	Red plus input 13	Reference Circuit 1
RnD	B16	Red minus input 13	Reference Circuit 1
RpE	A17	Red plus input 14	Reference Circuit 1
RnE	B17	Red minus input 14	Reference Circuit 1
RpF	A18	Red plus input 15	Reference Circuit 1
RnF	B18	Red minus input 15	Reference Circuit 1

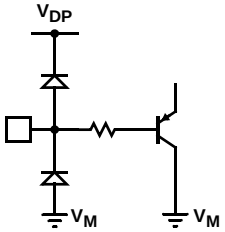
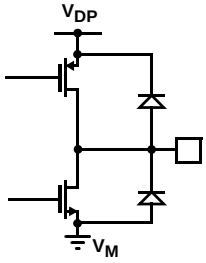
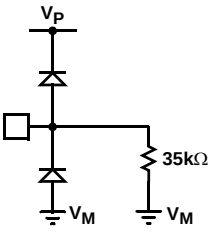
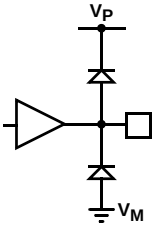
Pin Descriptions (Continued)

PIN NAME	SOLDER BALL	DESCRIPTION	EQUIVALENT CIRCUIT
TMon1	C18	Thermal Monitor 1 has diodes to measure die temperature	 CIRCUIT 6
Vp	A20	Analog plus supply	
Vm	MultipleBalls	Analog minus supply	
BnF	C19	Blue minus input 15	Reference Circuit 1
BpF	C20	Blue plus input 15	Reference Circuit 1
BnE	D19	Blue minus input 14	Reference Circuit 1
BpE	D20	Blue plus input 14	Reference Circuit 1
BnD	E19	Blue minus input 13	Reference Circuit 1
BpD	E20	Blue plus input 13	Reference Circuit 1
BnC	F19	Blue minus input 12	Reference Circuit 1
BpC	F20	Blue plus input 12	Reference Circuit 1
BnB	G19	Blue minus input 11	Reference Circuit 1
BpB	G20	Blue plus input 11	Reference Circuit 1
BnA	H19	Blue minus input 10	Reference Circuit 1
BpA	H20	Blue plus input 10	Reference Circuit 1
Bn9	J19	Blue minus input 9	Reference Circuit 1
Bp9	J20	Blue plus input 9	Reference Circuit 1
Bn8	K19	Blue minus input 8	Reference Circuit 1
Bp8	K20	Blue plus input 8	Reference Circuit 1
Vp	K18	Analog plus supply	
Vm	MultipleBalls	Analog minus supply	
Bn7	L19	Blue minus input 7	Reference Circuit 1
Bp7	L20	Blue plus input 7	Reference Circuit 1
Bn6	M19	Blue minus input 6	Reference Circuit 1
Bp6	M20	Blue plus input 6	Reference Circuit 1
Bn5	N19	Blue minus input 5	Reference Circuit 1
Bp5	N20	Blue plus input 5	Reference Circuit 1
Bn4	P19	Blue minus input 4	Reference Circuit 1
Bp4	P20	Blue plus input 4	Reference Circuit 1
Bn3	R19	Blue minus input 3	Reference Circuit 1
Bp3	R20	Blue plus input 3	Reference Circuit 1
Bn2	T19	Blue minus input 2	Reference Circuit 1
Bp2	T20	Blue plus input 2	Reference Circuit 1
Bn1	U19	Blue minus input 1	Reference Circuit 1

Pin Descriptions (Continued)

PIN NAME	SOLDER BALL	DESCRIPTION	EQUIVALENT CIRCUIT
Bp1	U20	Blue plus input 1	Reference Circuit 1
Bn0	V19	Blue minus input 0	Reference Circuit 1
Bp0	V20	Blue plus input 0	Reference Circuit 1
Vm	Vm	Analog minus supply	
Vp	Y20	Analog plus supply	
TMon2	V18	Thermal Monitor 2 has diodes to measure die temperature	Reference Circuit 6
GnF	W18	Green minus input 15	Reference Circuit 1
GpF	Y18	Green plus input 15	Reference Circuit 1
GnE	W17	Green minus input 14	Reference Circuit 1
GpE	Y17	Green plus input 14	Reference Circuit 1
GnD	W16	Green minus input 13	Reference Circuit 1
GpD	Y16	Green plus input 13	Reference Circuit 1
GnC	W15	Green minus input 12	Reference Circuit 1
GpC	Y15	Green plus input 12	Reference Circuit 1
GnB	W14	Green minus input 11	Reference Circuit 1
GpB	Y14	Green plus input 11	Reference Circuit 1
GnA	W13	Green minus input 10	Reference Circuit 1
GpA	Y13	Green plus input 10	Reference Circuit 1
Gn9	W12	Green minus input 9	Reference Circuit 1
Gp9	Y12	Green plus input 9	Reference Circuit 1
Gn8	W11	Green minus input 8	Reference Circuit 1
Gp8	Y11	Green plus input 8	Reference Circuit 1
Vp	V11	Analog plus supply	
Vm	MultipleBalls	Analog minus supply	
Gn7	W10	Green minus input 7	Reference Circuit 1
Gp7	Y10	Green plus input 7	Reference Circuit 1
Gn6	W9	Green minus input 6	Reference Circuit 1
Gp6	Y9	Green plus input 6	Reference Circuit 1
Gn5	W8	Green minus input 5	Reference Circuit 1
Gp5	Y8	Green plus input 5	Reference Circuit 1
Gn4	W7	Green minus input 4	Reference Circuit 1
Gp4	Y7	Green plus input 4	Reference Circuit 1
Gn3	W6	Green minus input 3	Reference Circuit 1
Gp3	Y6	Green plus input 3	Reference Circuit 1
Gn2	W5	Green minus input 2	Reference Circuit 1
Gp2	Y5	Green plus input 2	Reference Circuit 1
Gn1	W4	Green minus input 1	Reference Circuit 1
Gp1	Y4	Green plus input 1	Reference Circuit 1
Gn0	W3	Green minus input 0	Reference Circuit 1
Gp0	Y3	Green plus input 0	Reference Circuit 1

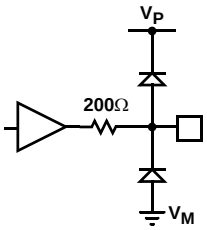
Pin Descriptions (Continued)

PIN NAME	SOLDER BALL	DESCRIPTION	EQUIVALENT CIRCUIT
Vm	Vm	Analog minus supply	
Vp	V3	Analog plus supply	
$\overline{\text{Chip}}$	V5	Chip enable (active low): when "HI" disables all analog except references; all analog or digital video outputs are in a high impedance state; all registers hold their data but remain programmable since the serial interface is left active	 CIRCUIT 4
Vdp	U5	Digital logic power supply: nominally at 3V	
$\overline{\text{Reset}}$	V4	Reset (active low): clears all registers in interface and calibration sections; this causes the chip to standby with all outputs in a high impedance state	Reference Circuit 4
$\overline{\text{sEn}}$	U4	Serial bus enable (active low): enables the serial bus when "LO"; latches the current value when transitioning to "HI"	Reference Circuit 4
Vp	V3	Analog plus supply	
Vm	MultipleBalls	Analog minus supply	
sClk	U3	Serial bus clock	Reference Circuit 4
sDo	T4	Serial bus data output	Reference Circuit 4
sDi	T3	Serial bus data input	 CIRCUIT 5
RefA	Y1	Output stage reference level (input) A	Reference Circuit 6
VmA	Y2	RGB video output stages' minus supply A	 CIRCUIT 7
Ba	W1	Blue output A	 CIRCUIT 2

Pin Descriptions (Continued)

PIN NAME	SOLDER BALL	DESCRIPTION	EQUIVALENT CIRCUIT
Va	W2	Vertical sync output A	Reference Circuit 5
Ga	V1	Green output A	Reference Circuit 2
Ha	V2	Horizontal sync output A	Reference Circuit 5
Ra	U1	Red output A	Reference Circuit 2
VpA	U2	RGB video output stages' plus supply A	Reference Circuit 7
RefB	T1	Output stage reference level (input) B	Reference Circuit 6
VmB	T2	RGB video output stages' minus supply B	Reference Circuit 7
Bb	R1	Blue output B	Reference Circuit 2
Vb	R2	Vertical sync output B	Reference Circuit 5
Gb	P1	Green output B	Reference Circuit 2
Hb	P2	Horizontal sync output B	Reference Circuit 5
Rb	N1	Red output B	Reference Circuit 2
VpB	N2	RGB video output stages' plus supply B	Reference Circuit 7
RefC	M1	Output stage reference level (input) C	Reference Circuit 6
VmC	M2	RGB video output stages' minus supply C	Reference Circuit 7
Bc	L1	Blue output C	Reference Circuit 2
Vc	L2	Vertical sync output C	Reference Circuit 5
Gc	K1	Green output C	Reference Circuit 2
Hc	K2	Horizontal sync output C	Reference Circuit 5
Rc	J1	Red output C	Reference Circuit 2
VpC	J2	RGB video output stages' plus supply C	Reference Circuit 7
RefD	H1	Output stage reference level (input) D	Reference Circuit 6
VmD	H2	RGB video output stages' minus supply D	Reference Circuit 7
Bd	G1	Blue output D	Reference Circuit 2
Vd	G2	Vertical sync output D	Reference Circuit 5
Gd	F1	Green output D	Reference Circuit 2
Hd	F2	Horizontal sync output D	Reference Circuit 5
Rd	E1	Red output D	Reference Circuit 2
VpD	E2	RGB video output stages' plus supply D	Reference Circuit 7
RefS	D1	Output stage reference level (input) S	Reference Circuit 6
VmS	D2	RGB video output stages' minus supply S	Reference Circuit 7
Bs	C1	Blue output S	Reference Circuit 2
Vs	C2	Vertical sync output S	Reference Circuit 5
Gs	B1	Green output S	Reference Circuit 2
Hs	B2	Horizontal sync output S	Reference Circuit 5
Rs	A1	Red output S	Reference Circuit 2
VpS	A2	RGB video output stages' plus supply S	Reference Circuit 7
BOL	E3	Blue overlay input for output group S	Reference Circuit 6
GOL	E4	Green overlay input for output group S	Reference Circuit 6
ROL	D4	Red overlay input for output group S	Reference Circuit 6

Pin Descriptions (Continued)

PIN NAME	SOLDER BALL	DESCRIPTION	EQUIVALENT CIRCUIT
RefOL	D5	Overlay inputs' reference level for output group S	Reference Circuit 6
Vm	MultipleBalls	Analog minus supply	
BAZ	F4	Blue auto-zero internal calibration level monitor for output group S	 CIRCUIT 3
GAZ	D6	Green auto-zero internal calibration level monitor for output group S	Reference Circuit 3
Vp	C3	Analog plus supply	
RAZ	C6	Red auto zero internal calibration level monitor for output group S	Reference Circuit 3
Vdp	U5	Digital logic power supply: nominally at 3V	
$\overline{\text{Ovl}}$	D3	Digital input to select whether overlay is active for output group S	Reference Circuit 4
Cal	C4	Digital input to calibrate S output group	Reference Circuit 4
$\overline{\text{Trans}}$	C5	Digital input to select a transparent overlay for output group S	Reference Circuit 4
Vp	C3	Analog plus supply	
Vm	MultipleBalls	Analog minus supply	
Vm	A19	Analog minus supply	
Vm	B19, B20, C7, C8, C9, C10, C12, C13, C14, C15, C16, C17, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, E17, E18, F3, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F17, F18, G3, G4, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G17, G18, H3, H4, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H17, H18, J3, J4, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J17, J18, K3, K4, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, K17, L3, L4, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L17, L18, M3, M4, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M17, M18, N3, N4, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, N17, N18, P3, P4, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P17, P18, R3, R4, R6, R7, R8, R9, R10, R11, R12, R13, R1, R15, R17, R18, T17, T18, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, V7, V8, V9, V10, V12, V13, V14, V15, V16, V17, W19, W20, Y19		
N/C	U6, V6	Not connected; may be grounded	

Absolute Maximum Ratings (T_A = +25°C)

V_{SA} 5.5V
Input Voltage . . . . . V_S
V_{SD} 3.3V
Output Current 80mA

Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +135°C
Recommended Operating Temperature . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

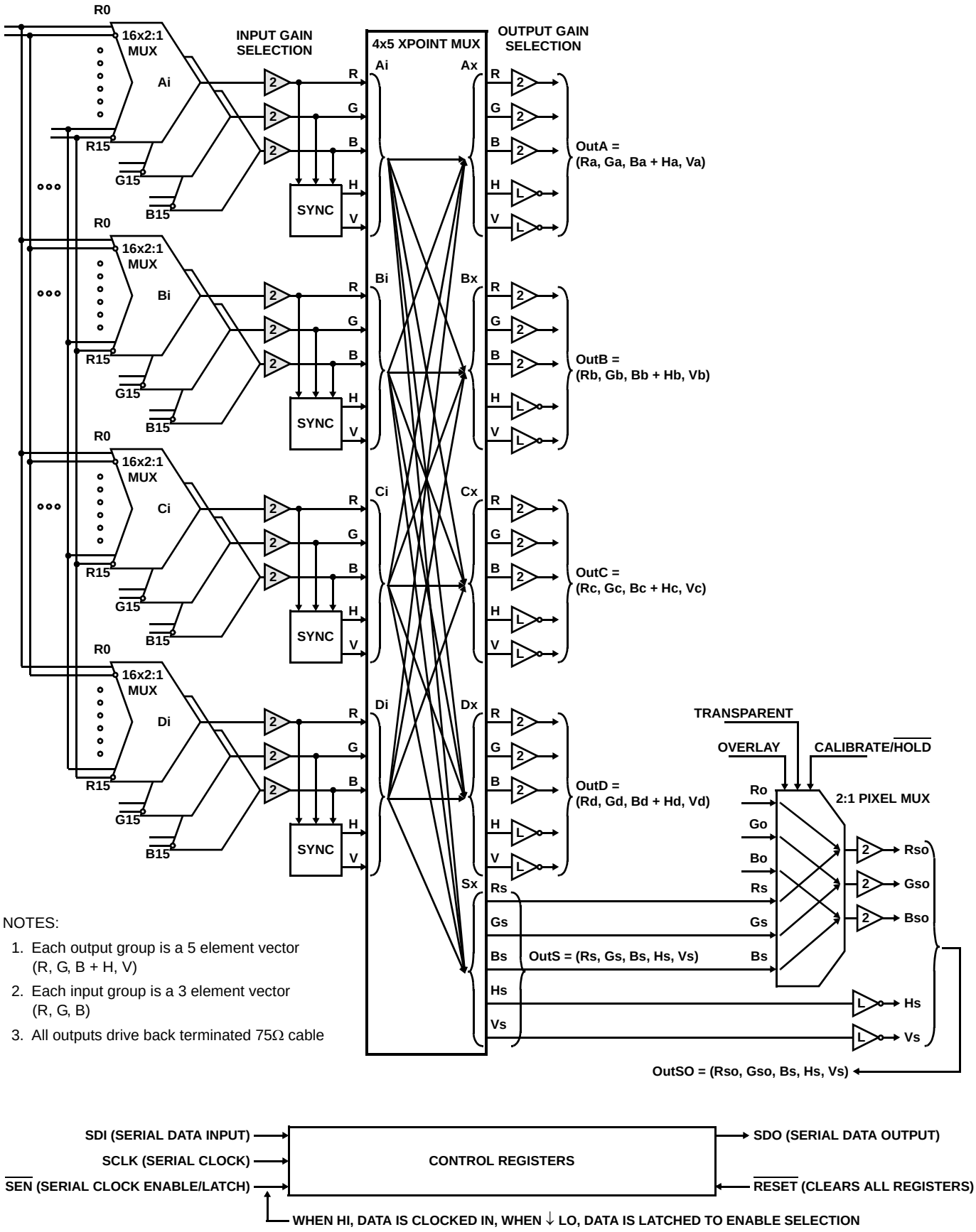
V_{SA} = 5V, V_{SD} = 3.3V, Gain = 2, R_L = 150Ω, C_L = 2.7pF, T_A = +25°C.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
V_{SA}	Recommended Analog Supply Voltage		4.75	5.0	5.25	V
V_{SD}	Recommended Digital Supply Voltage		2.4	3.3	3.6	V
I_{SD}	Digital Supply Current			3	10	mA
I_{SA}	Analog Supply Current	Enabled - no load, all amplifiers enabled		685	790	mA
		Disabled		33	50	mA
PSRR	Power Supply Rejection Ratio	4.75V to 5.25V		40		dB
CHARACTERISTICS OF DIFFERENTIAL INPUTS						
CMRR	Input Common Mode Rejection Ratio	0V to 1.5V	45	66		dB
A_V	Gain Accuracy for A, B, C, D, S Channels	Range of Deviation from gain of 2 (excluding overlay)	1.85	2.0	2.15	
V_N	Input Referred Voltage Noise	A_V = +2		40		nV/$\sqrt{Hz}$
V_{OS}	Input Referred Offset Voltage	Includes muxes and output amps; A, B, C, D channels	-80	0	80	mV
		S channel in auto-calibration mode	-10	5	12	mV
V_{IN}	Maximum Recommended Input Range				V_{SA}	V
C_{IN}	Input Capacitance			2		pF
R_{IN}	Input Resistance, Single-ended		1100	1320	1550	Ω
V_{INSET}	Input Biasing Voltage		1.49	1.53	1.57	V
OVERLAY INPUT CHARACTERISTICS						
V_{OS}	Input Referred Offset Voltage	S channel overlay inputs at A_V = 2	-10	5	12	mV
OVERLAY SWITCHING CHARACTERISTICS						
$P_{APERTURE}$	Pixel Mux Aperture of Uncertainty	5% setting for max signal charge		10		ns
A_V	Gain Accuracy for S Channel	S channel overlay input				
OUTPUT CHARACTERISTICS						
Output Impedance		Enabled		100		mΩ
		Disabled		10		MΩ
V_{OUT}	Maximum Recommended Output Range		0		3.3	V
I_{OUT}	Output Current	Short-circuit (5Ω)		60		mA

Electrical Specifications V_{SA} = 5V, V_{SD} = 3.3V, Gain = 2, R_L = 150Ω, C_L = 2.7pF, T_A = +25°C. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SR	Slew Rate	$2V_{P-P}$ symmetrical, R_L = 150Ω, A_V = 2, guaranteed by design		800		V/µs
BW	-3dB Bandwidth	-3dB, 200mV_{P-P}, load of 150Ω		300		MHz
	0.1dB Bandwidth	0.1dB, 200mV_{P-P}, load of 150Ω		60		MHz
Settling Time	1% Settling Time	$2V_O$ step, load of 150Ω		10		ns
Crosstalk	Hostile Crosstalk Between any 2 Channels	100MHz		-70		dB
	Worst Case Hostile Crosstalk One Channel Affected by all Other Channels Running the Same Signal	100MHz		-50		dB

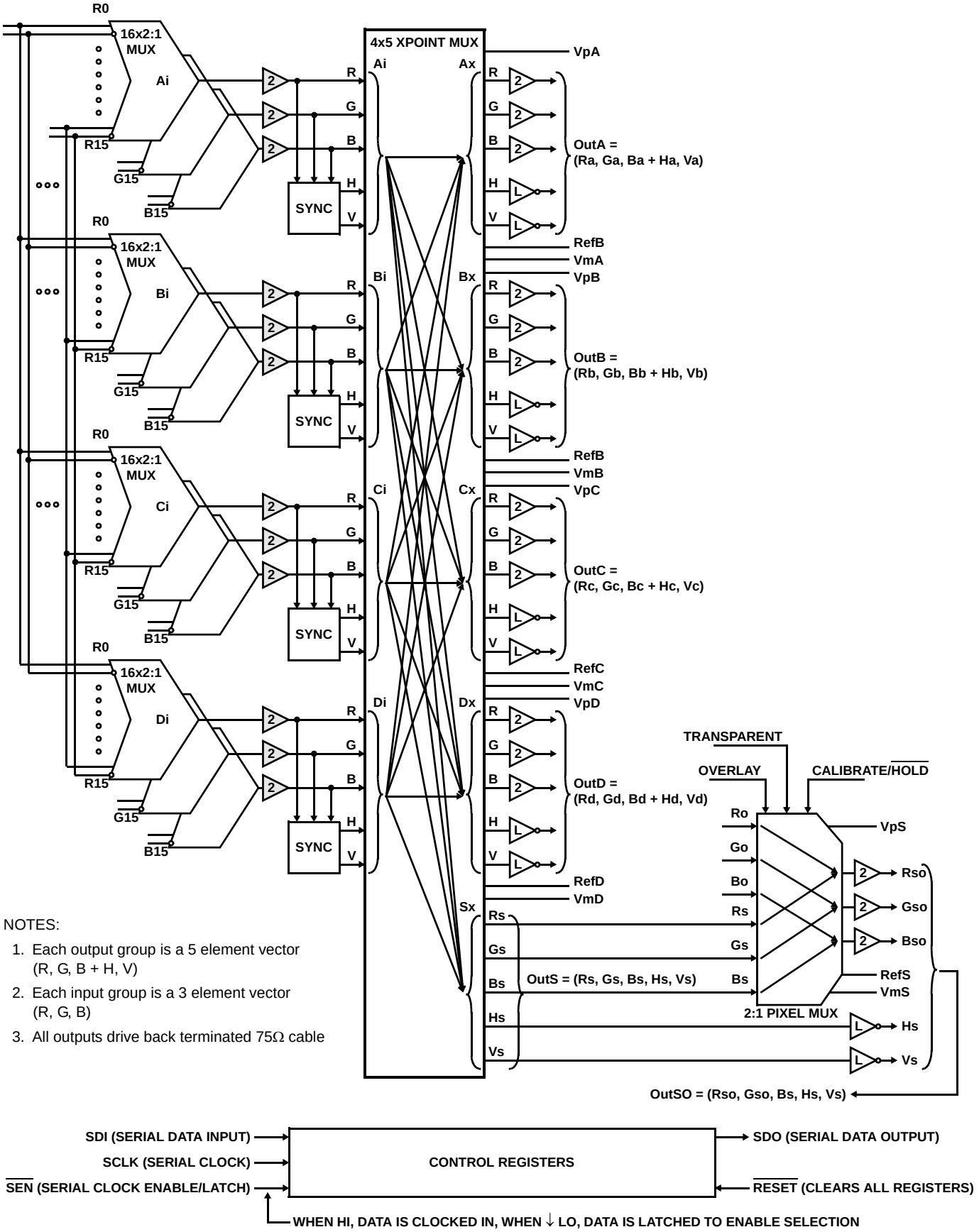
I/O Block Diagram of Video Signals



NOTES:

1. Each output group is a 5 element vector (R, G, B + H, V)
2. Each input group is a 3 element vector (R, G, B)
3. All outputs drive back terminated 75Ω cable

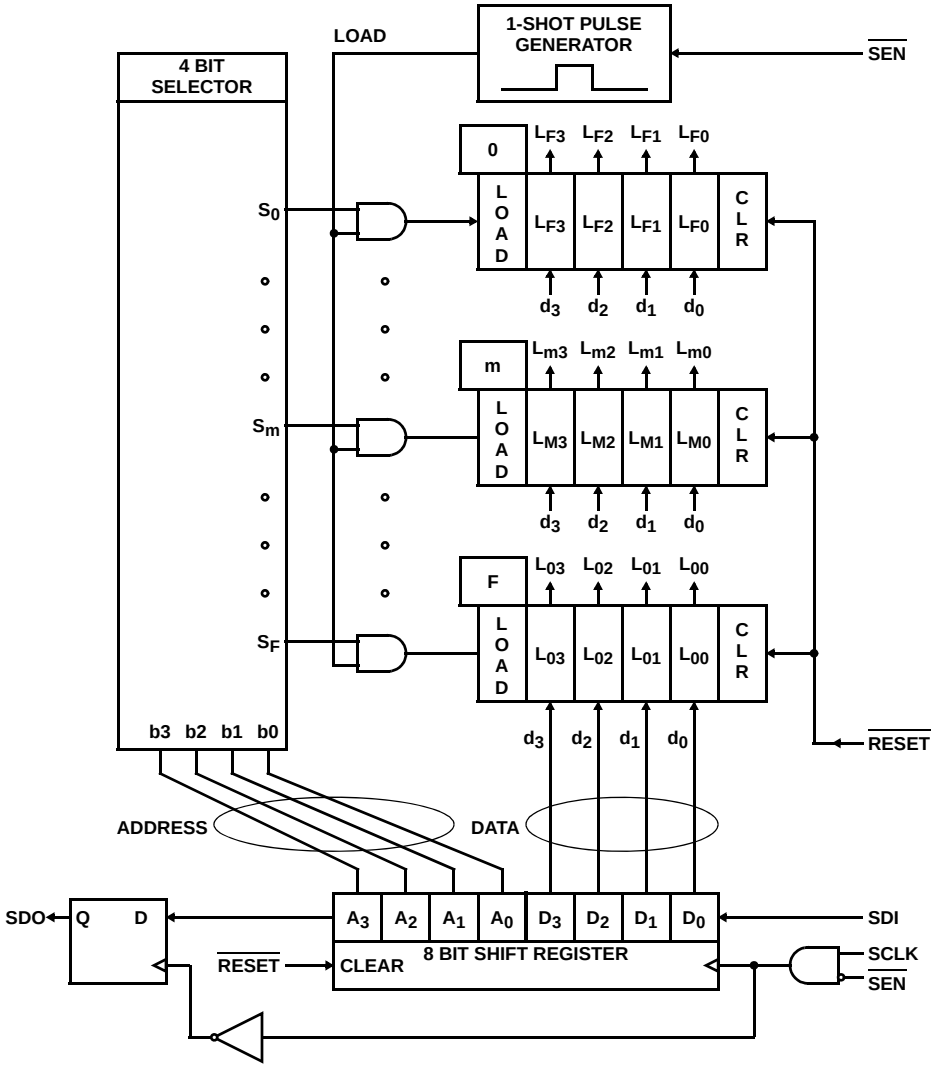
I/O Block Diagram of Video Signals with Power Supplies and References



NOTES:

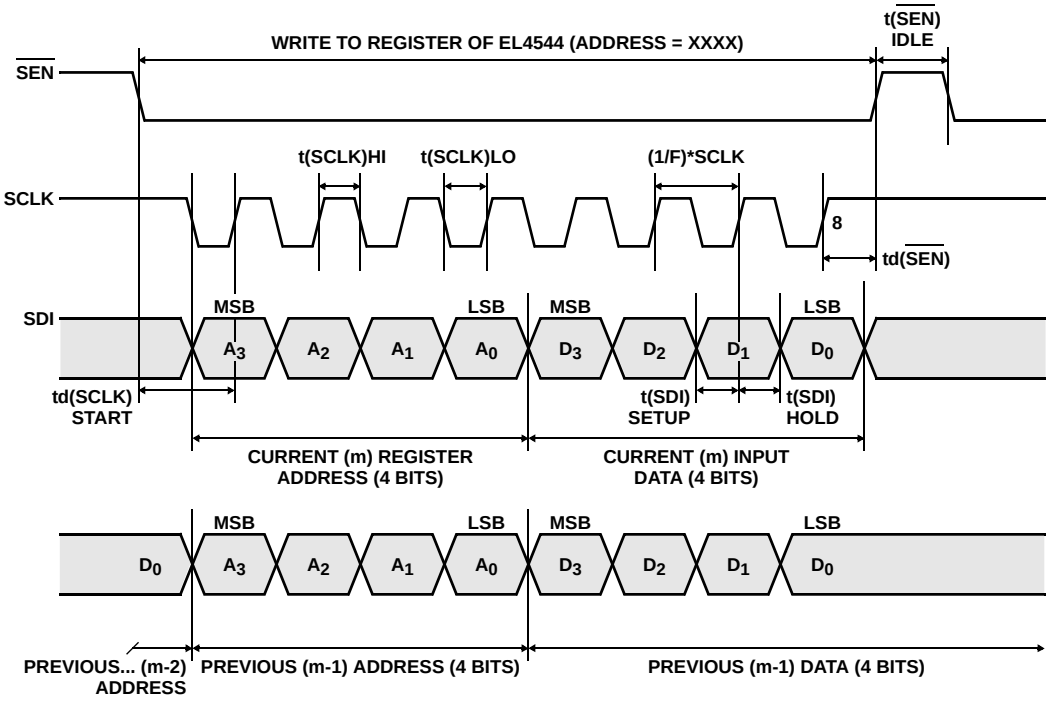
1. Each output group is a 5 element vector (R, G, B + H, V)
2. Each input group is a 3 element vector (R, G, B)
3. All outputs drive back terminated 75Ω cable

Serial Bus Interface Architecture



NOTE: The selector has 16 outputs, connected to 16 AND gates, connected to 16 4-bit latches. Rising edge of SEN triggers the load one-shot.

Serial Bus Interface Timing Diagram



NOTE: Readback of the serial bus register can be done as follows: After $\overline{SEN}$ is taken low, latching data, and before writing the next word, the data in the register can be read back by clocking out 8 bits before writing in the next word.

Serial Bus Interface Control Table

HEX ADDRESS CODE	FUNCTION	ADDRESS				DATA			
		A3	A2	A1	A0	D3	D2	D1	D0
0	**Ai** Input Mux: Select Input of Input Mux **Ai**	0	0	0	0	S3	S2	S1	S0
1	**Bi** Input Mux: Select Input of Input Mux **Bi**	0	0	0	1	S3	S2	S1	S0
2	**Ci** Input Mux: Select Input of Input Mux **Ci**	0	0	1	0	S3	S2	S1	S0
3	**Di** Input Mux: Select Input of Input Mux **Di**	0	0	1	1	S3	S2	S1	S0
4	Enable Any of the 4 Input Muxes: **Di/Ci/Bi/Ai**	0	1	0	0	EnDi	EnCi	EnBi	EnAi
5	**Ti** Input Test Mux: Select Which Input Group is Connected to Input Test Mux	0	1	0	1	TiS3	TiS2	TiS1	TiS0
6	Enable Test Muxes: Input and Output	0	1	1	0	EnTi	ToS2	ToS1	ToS0
7	Enable Sync Detectors for **Di/Ci/Bi/Ai**	0	1	1	1	EnDSync	EnCSync	EnBSync	EnASync
8	**Ax** Crosspoint Mux: Enable/Gain = 2or1/Select Input (2Bits)	1	0	0	0	En	A_V=2/ not1	S1	S0
9	**Bx** Crosspoint Mux: Enable/Gain = 2or1/ Select Input (2Bits)	1	0	0	1	En	A_V=2/ not1	S1	S0
A	**Cx** Crosspoint Mux: Enable/Gain = 2or1/ Select Input (2Bits)	1	0	1	0	En	A_V=2/ not1	S1	S0
B	**Dx** Crosspoint Mux: Enable/Gain = 2or1/ Select Input (2Bits)	1	0	1	1	En	A_V=2/ not1	S1	S0
C	**Sx** Crosspoint Mux: Enable/Gain = 2or1/ Select Input (2Bits)	1	1	0	0	En	A_V=2/ not1	S1	S0
D	Sync, Overlay, and Calibration Modes	1	1	0	1	X	Trans	Toggle	Autocal
E	Gain for: **Di/Ci/Bi/Ai** Set to HI for gain of 2 Set to LO for gain of 1	1	1	1	0	AvDi=2	AvCi=2	AvBi=2	AvDi=2
F	No Operation	1	1	1	1	X	X	X	X

Order bits are loaded		1	2	3	4	5	6	7	8

Typical Performance Curves

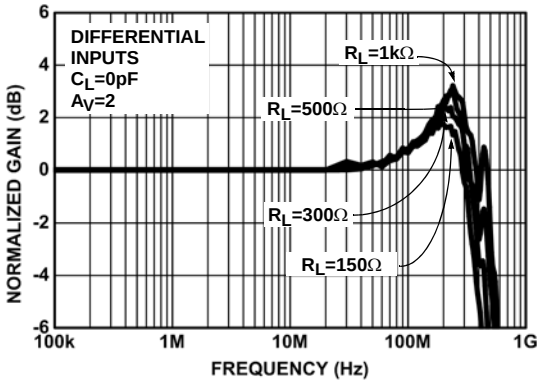


FIGURE 1. FREQUENCY FOR VARIOUS R_{LOAD}

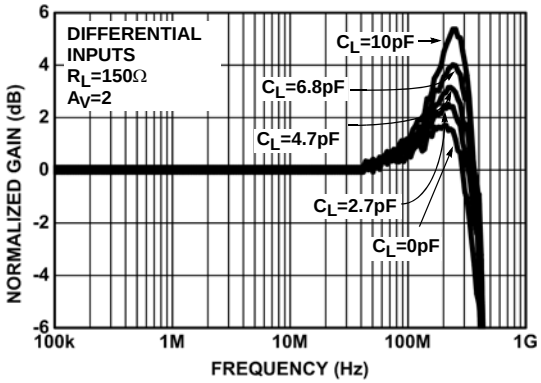


FIGURE 2. FREQUENCY FOR VARIOUS C_{LOAD}

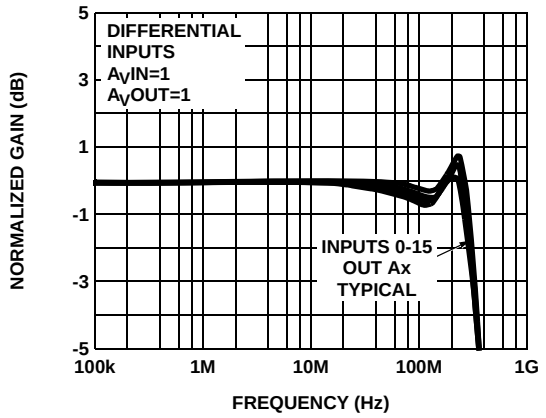


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS INPUT CHANNELS

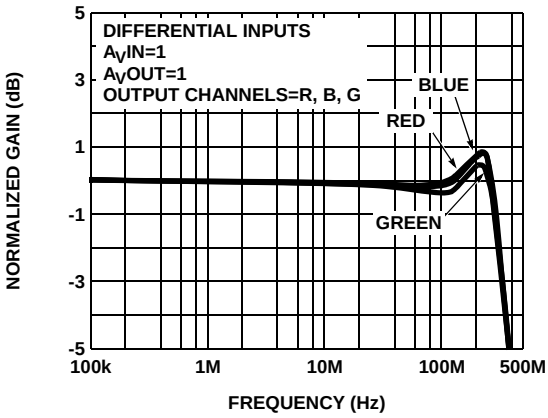


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS OUTPUT COLOR CHANNELS

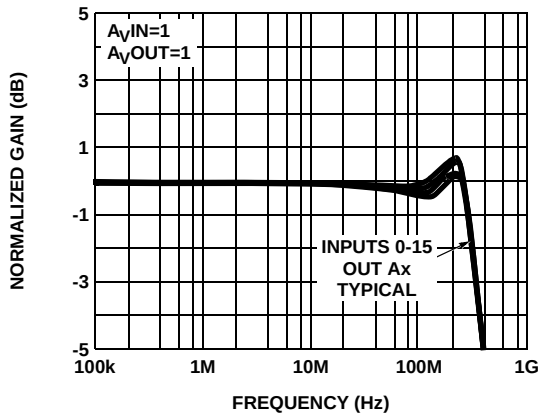


FIGURE 5. GAIN vs FREQUENCY FOR VARIOUS NON INVERTING INPUTS

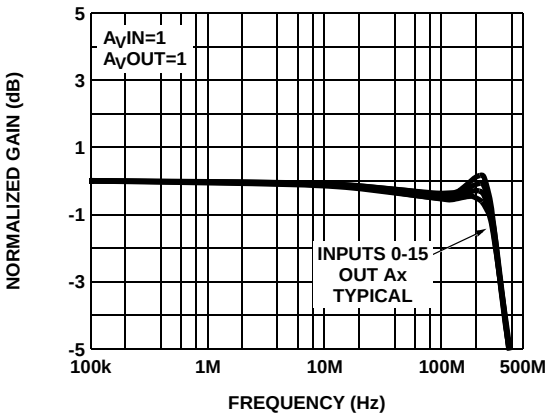


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS INVERTING INPUTS

Typical Performance Curves (Continued)

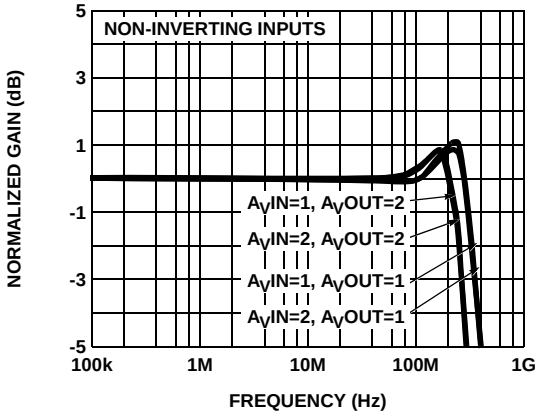


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS GAINS

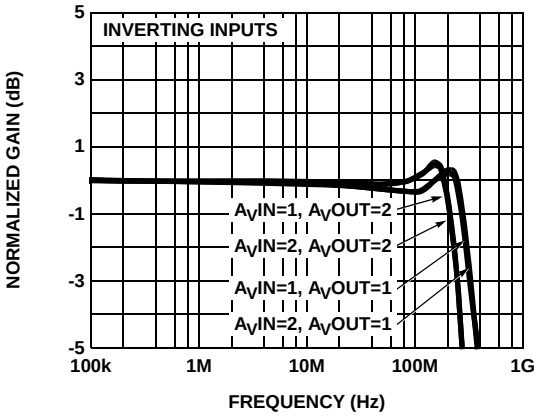


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS GAINS

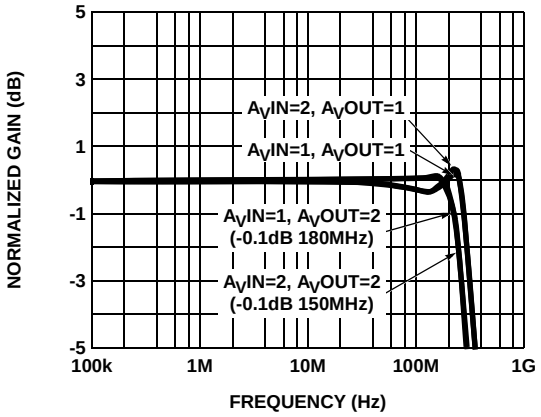


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS GAIN COMBINATIONS

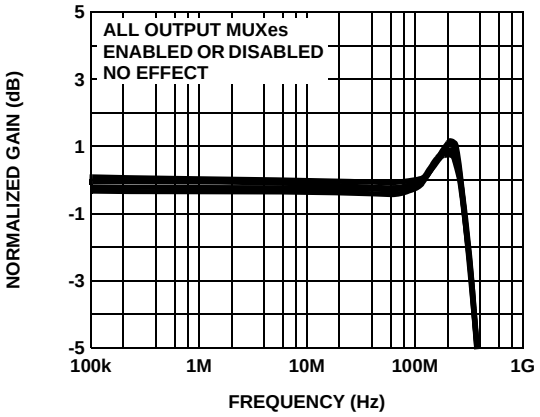


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS INPUT MUX LOADING

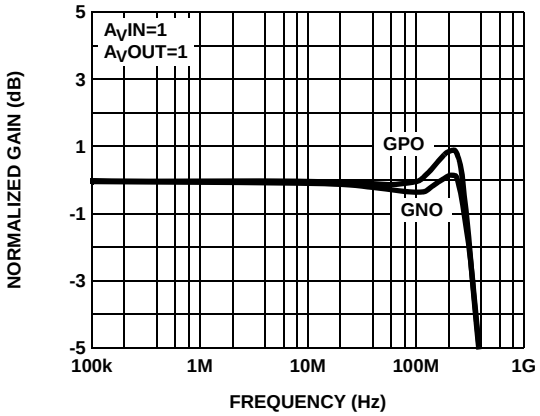


FIGURE 11. GAIN vs FREQUENCY DIFFERENTIAL INPUT COMPARISON

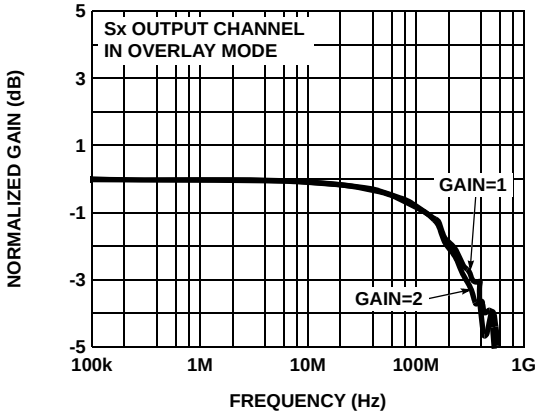


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS GAINS

Typical Performance Curves (Continued)

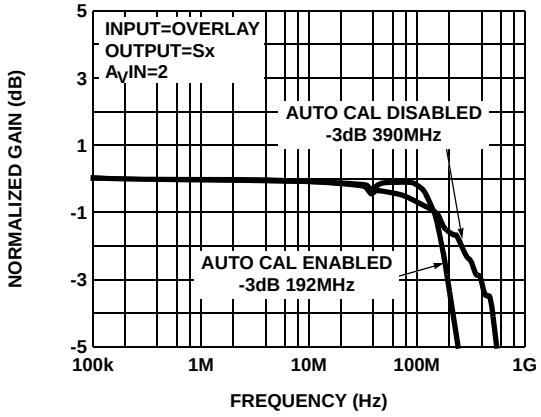


FIGURE 13. GAIN vs FREQUENCY FOR Sx CHANNEL FUNCTIONS

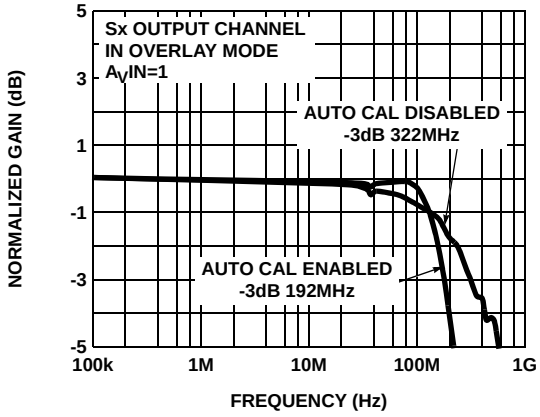


FIGURE 14. GAIN vs FREQUENCY FOR Sx CHANNEL FUNCTIONS

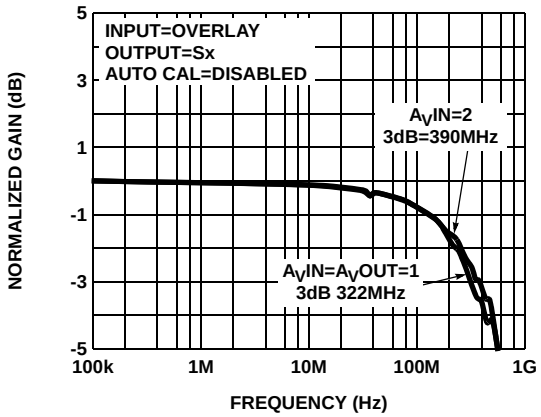


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS GAINS

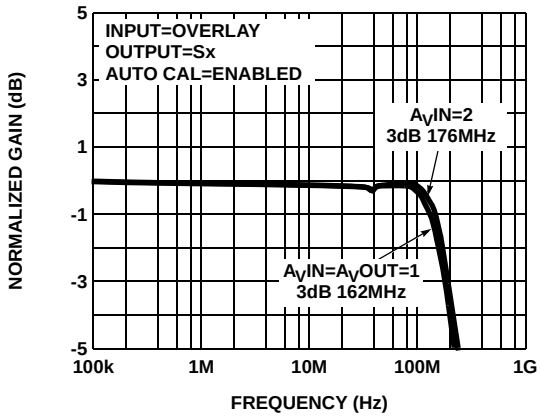


FIGURE 16. GAIN vs FREQUENCY FOR VARIOUS GAINS

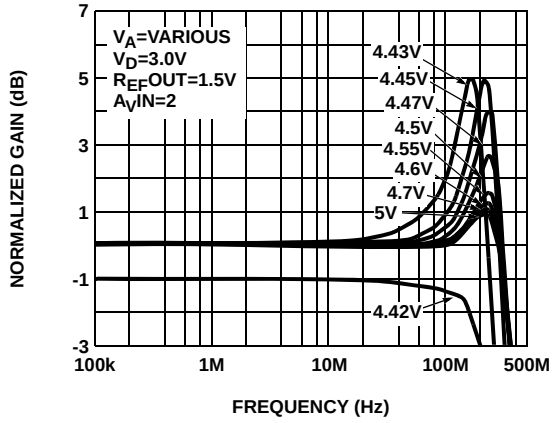


FIGURE 17. PEAKING FOR VARIOUS POWER SUPPLY SETTINGS

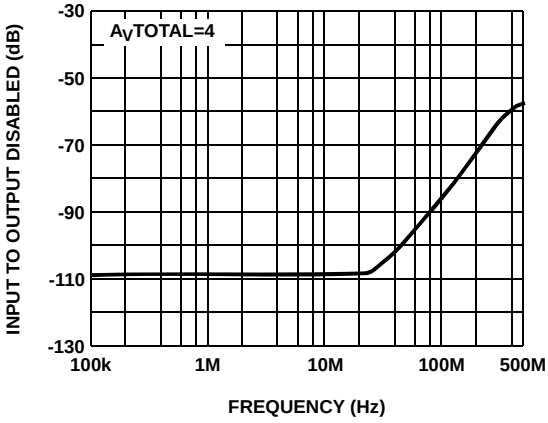


FIGURE 18. INPUT TO OUTPUT ISOLATION (DISABLED)

Typical Performance Curves (Continued)

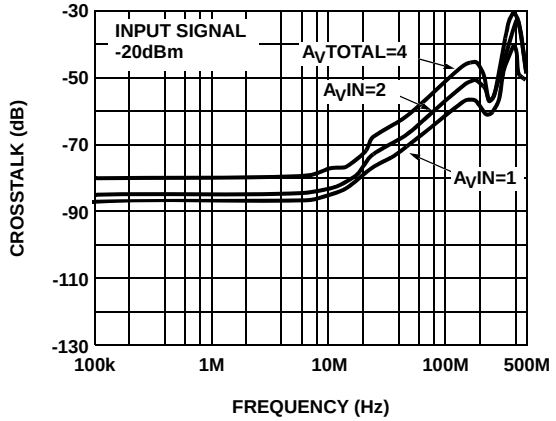


FIGURE 19. CROSSTALK FOR VARIOUS GAINS

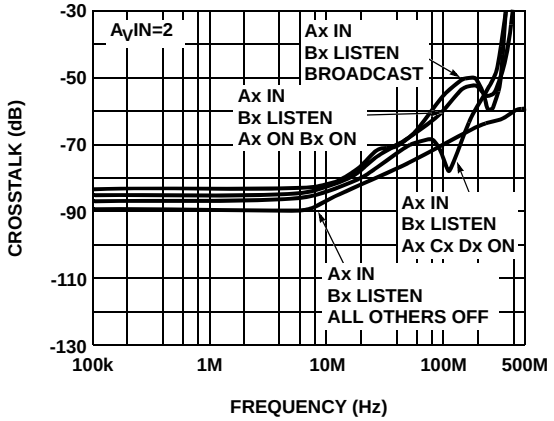


FIGURE 20. CROSSTALK FOR VARIOUS BROADCAST MODES

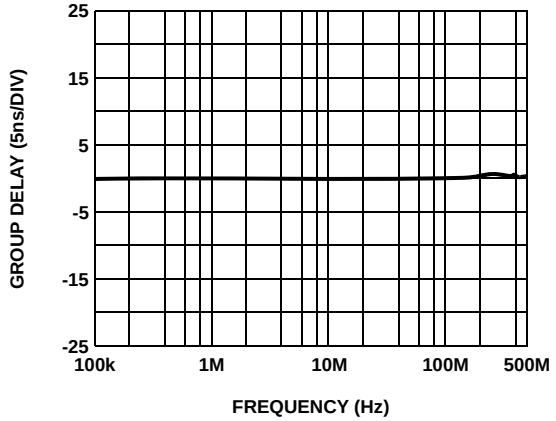


FIGURE 21. GROUP DELAY FOR OUTPUT CHANNELS A, B, C, D, S

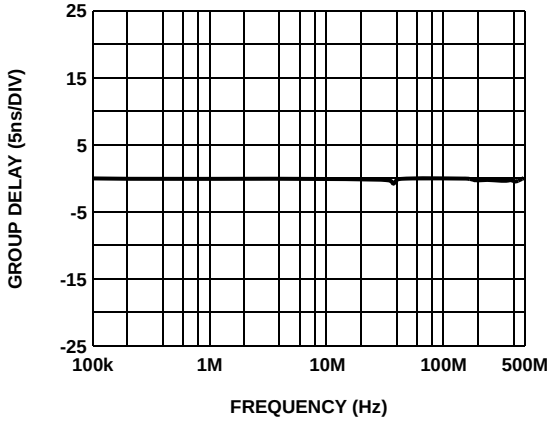


FIGURE 22. GROUP DELAY FOR OVERLAY MODE

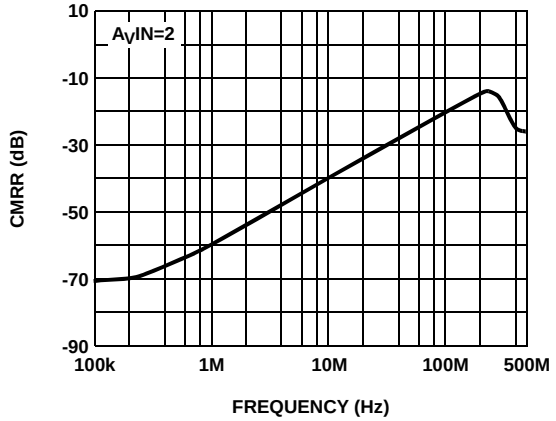


FIGURE 23. CMRR

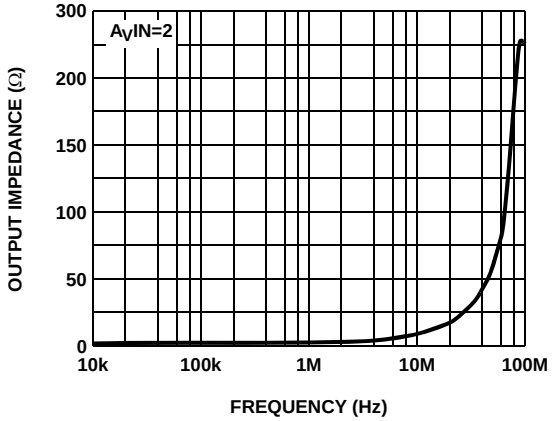


FIGURE 24. OUTPUT IMPEDANCE

Typical Performance Curves (Continued)

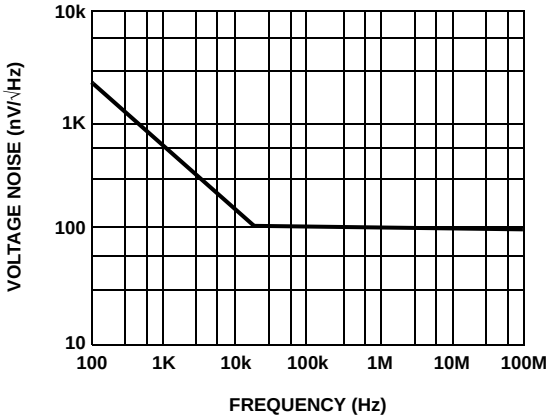


FIGURE 25. VOLTAGE NOISE vs FREQUENCY

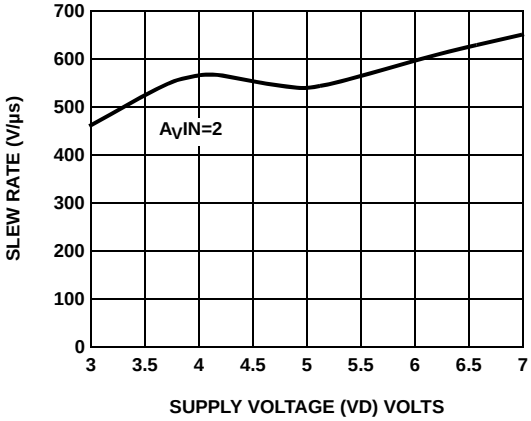


FIGURE 26. SLEW RATE vs SUPPLY (VD)

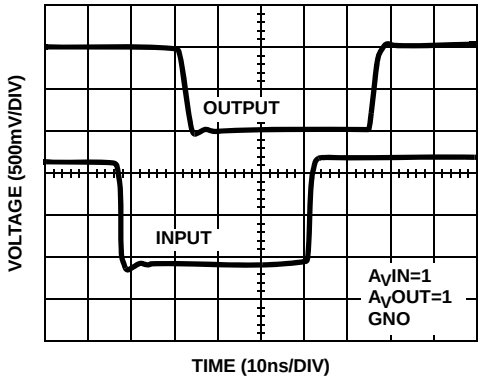


FIGURE 27. SMALL SIGNAL NEGATIVE PULSE RESPONSE

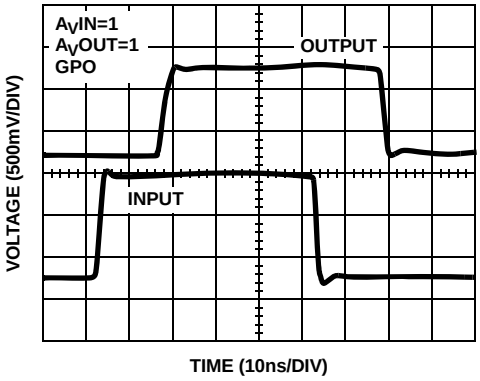


FIGURE 28. SMALL SIGNAL POSITIVE PULSE RESPONSE

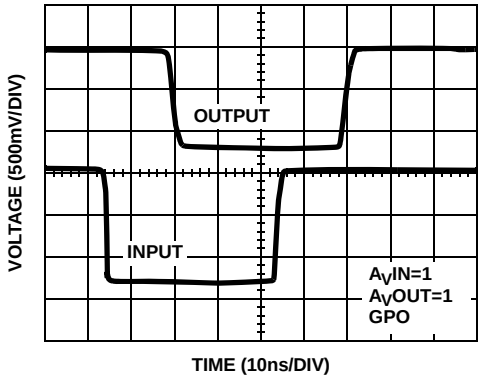


FIGURE 29. LARGE SIGNAL NEGATIVE PULSE RESPONSE

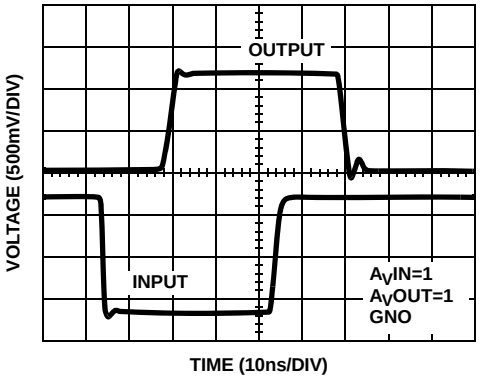


FIGURE 30. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves (Continued)

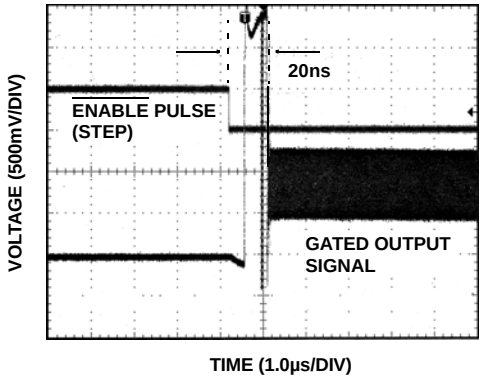


FIGURE 31. ENABLE TIME

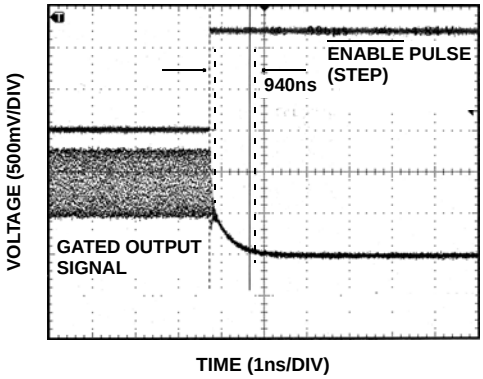


FIGURE 32. DISABLE TIME

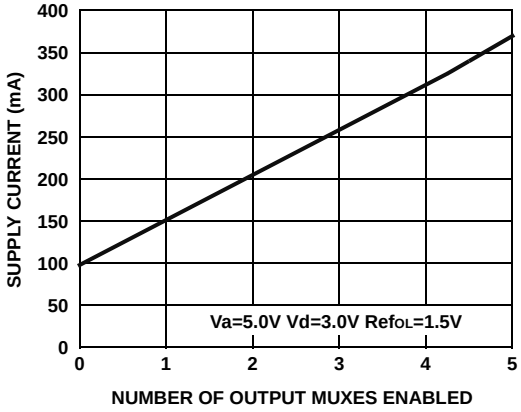


FIGURE 33. POWER SUPPLY CURRENT AS FUNCTION OF OUTPUT MUXES ENABLED - ALL INPUT MUXES DISABLED

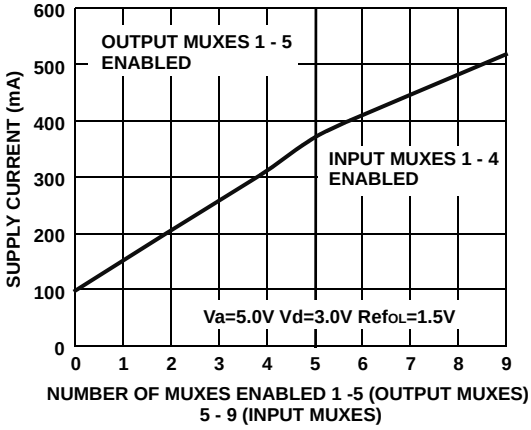


FIGURE 34. POWER SUPPLY CURRENT AS FUNCTION OF INPUT AND OUTPUT MUXES ENABLED

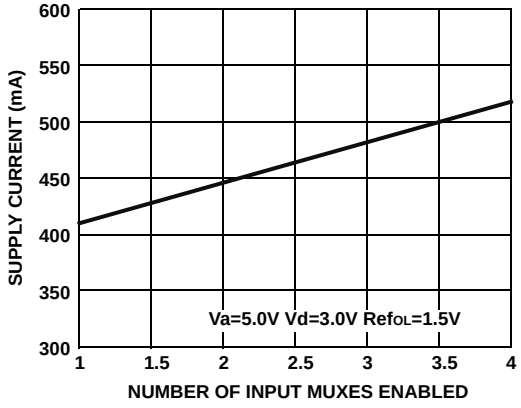


FIGURE 35. POWER SUPPLY CURRENT AS FUNCTION OF INPUT MUXES ENABLED - ALL OUTPUT MUXES ENABLED

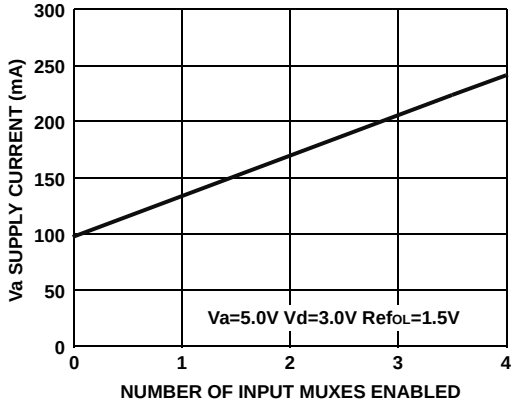


FIGURE 36. POWER SUPPLY CURRENT AS FUNCTION OF INPUT MUXES ENABLED - ALL OUTPUT MUXES DISABLED

Typical Performance Curves (Continued)

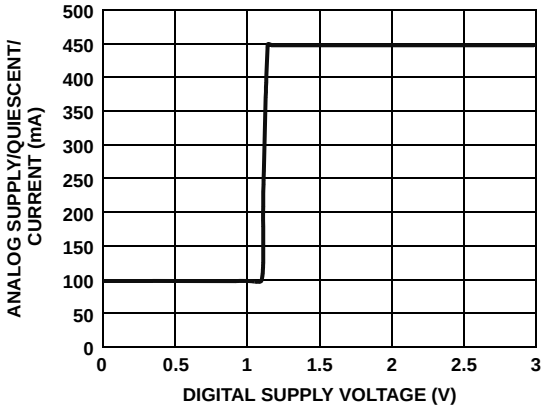


FIGURE 37. ANALOG CURRENT vs DIGITAL SUPPLY VOLTAGE

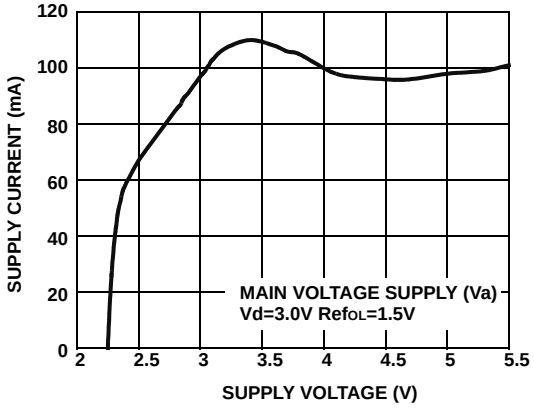


FIGURE 38. SUPPLY CURRENT VERSUS SUPPLY VOLTAGE BASE LINE IDLE - ALL INPUTS AND OUTPUTS DISABLED

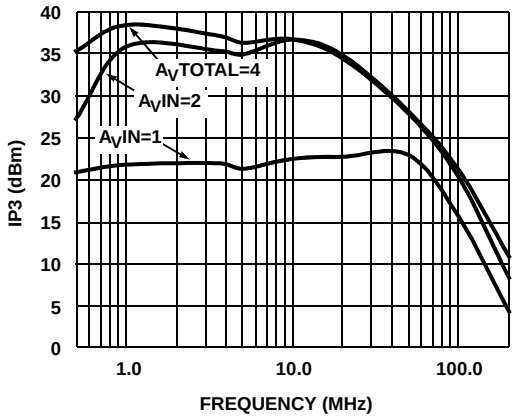


FIGURE 39. THIRD-ORDER INTERCEPT POINT vs FREQUENCY GREEN CHANNEL

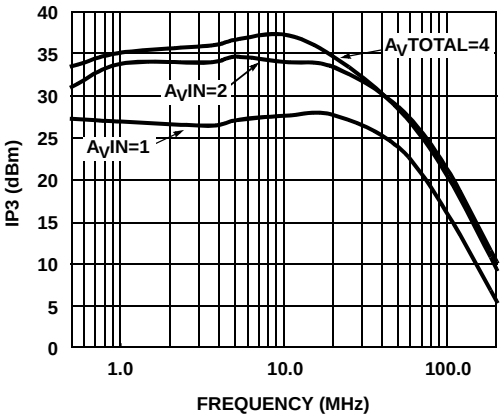


FIGURE 40. THIRD-ORDER INTERCEPT POINT vs FREQUENCY BLUE CHANNEL

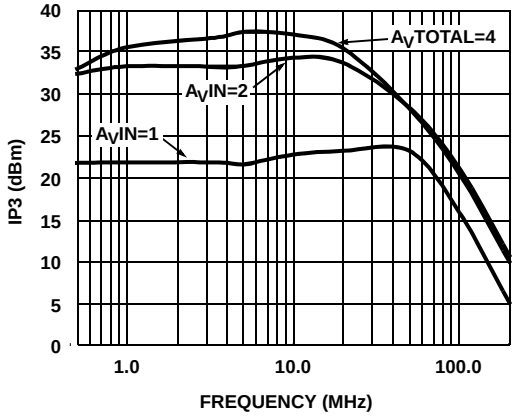


FIGURE 41. THIRD-ORDER INTERCEPT POINT vs FREQUENCY RED CHANNEL

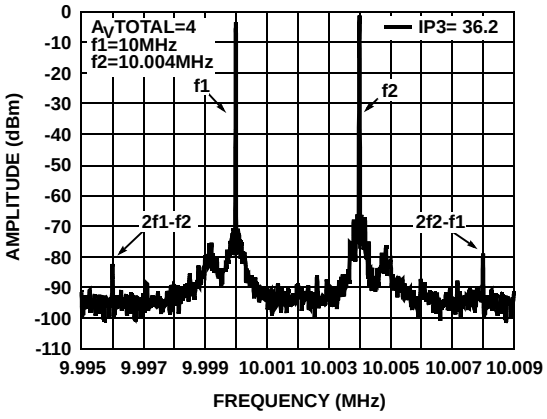


FIGURE 42. IP3 A_VTOTAL = 4 BLUE CHANNEL

Typical Performance Curves (Continued)

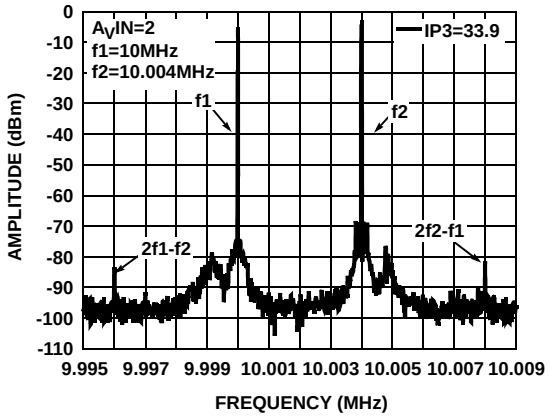


FIGURE 43. IP3 A_VIN = 2 BLUE CHANNEL

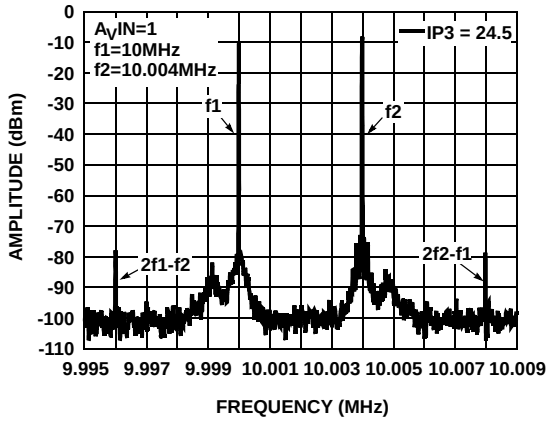


FIGURE 44. IP3 A_VIN = 1 BLUE CHANNEL

Functional Overview

Overall Functionality

The EL4544 is a video crosspoint switch that has 16 (RGB differential) input channels (with H and V sync embedded in their common-modes) which connect via an internal crosspoint mux to 5 (RGB + HV) single-ended output channels. The 5th output group has enhanced features that include: a pixel-by-pixel overlay mux and auto-calibrated offset cancellation. All analog and digital outputs have a high-impedance state, allowing several EL4544 to share the same output connections.

16 RGB Differential Video Inputs with Encoded Sync

For each of the 16 RGB groups of differential video inputs, horizontal and vertical sync are encoded as a combination of the common modes for each RGB group. Each of these differential input pins has a single-ended signal range that spans the entire 0V to 5V supply range. The embedded sync signals are provided by the EL4543 Triple Differential Twisted Pair Driver IC.

Overall Analog Signal Flow

There are four independent internal input multiplexors represented as **Ai**, **Bi**, **Ci**, and **Di** in the block diagram and serial bus interface control table (hexa-decimal addresses 0h, 1h, 2h, 3h). These muxes convert the selected RGB differential input signal to single-ended RGB and extract H and V sync. The five output crosspoint multiplexors represented as **Ax**, **Bx**, **Cx**, **Dx**, and **Sx**, can independently select from the four internal (RGBHV) signal groups **Ai**, **Bi**, **Ci**, and **Di** by programming the hexadecimal serial bus addresses 8h, 9h, Ah, Bh, and Ch. There are five RGBHV single-ended output signal groups labelled A, B, C, D, and S which buffer signals from the corresponding crosspoint outputs **Ax**, **Bx**, **Cx**, **Dx**, and **Sx**. Each of these output groups has an independent reference pin (**RefA**, **RefB**, **RefC**, **RefD**, and **RefS**) that allows the user to program the reference level that corresponds to a zero voltage differential input.

Analog and Digital Video Outputs

All analog outputs (A, B, C, D, and S) have a signal range from 0V to 3.5V and are capable of driving the 150Ω load presented by a terminated video cable. The H and V sync outputs and all other digital I/O are compatible with 3V operation; their signal swings are determined by connecting the digital supply pin **Vdp** to a 3V source.

How to Configure the Analog Video Outputs to Swing to 0V

The RGB analog outputs of the A, B, C, D, and S output groups are all capable of a range of swing that reaches the negative supply pin **Vm** = 0V. However, since the EL4544 has no internal supply connections, its single-ended outputs run out of bandwidth, slew rate, and linearity below 0.5V. If accurate wide band performance below 0.5V is required, add external pulldown resistors between each analog output and an external -5V supply.

This will keep the output stage biased. Values between 3kΩ to 1kΩ are suggested. The lower the selected resistance, the wider the bandwidth will be at 0V, but lower external resistance will increase overall IC power dissipation significantly since these resistors are loading their respective output stages.

Operating the S Output Group Near Ground

The S output group has one additional consideration to cover configurations where the output signals and the output reference pin **RefS** are operated below 0.5V. Under these circumstances, each of the three auto-zero monitoring pins **RAZ**, **GAZ**, and **BAZ**, require an external 10kΩ resistor

connecting each to an external -5V supply. This keeps the auto-zero circuitry active all the way down to ground.

Switchable Video Output Group Has Overlay Capability and Offset Cancellation

The S group of output signals have an overlay switch that allows single-ended inputs **ROL**, **GOL**, and **BOL**, to be inserted on a pixel-by-pixel basis. The pin **RefoL** allows the user to program the overlay input (reference) level that produces an output voltage equal to the output reference pin **RefS**. The S group of video outputs has an Auto-Calibration mode which can null out offsets through the entire selected signal path from its inputs to its outputs. (It is usually triggered during the front or back porch of video when the input signal is known to be at Black Level.)

Transparent vs Opaque Overlays

The overlay input for the S group is directly selected by the Overlay control pin **Ovl**. Two types of overlay are possible. The simplest overlay alternates between the dedicated overlay input and the "thru" input (that has been selected by the cross-point multiplexor). The "transparent" overlay mode is different from the standard overlay mode in that it presents the average of the overlay input and the "thru" input signal during overlay. The transparent mode is selected either by driving the Trans pin low or by programming bit D2 in Register D of the Serial Interface to a logical "1".

Serial Interface Control of the Auto-Calibration Feature

Programming bit D0 in Register D of the Serial Interface to a logical "1" activates the "Auto-Calibration" Mode which allows offsets from all inputs to the S group to be nulled-out via a calibration sequence. The programming Bit D1 in Register D of the Serial Interface is called **Toggle**. It allows for two modes of auto-calibration. If Toggle is programmed to a logical "0", Toggle mode is inactive. The auto-calibration cycle must be executed separately for both input groups (the overlay and the through signal groups).

What Happens During an Auto-Calibration Cycle

The auto-calibration (auto-zero) feature only applies to the S group of outputs. An auto-calibration cycle works as follows for either the overlay input or a selected "thru" input from the cross-point: During any time when the input signal is known to be at a "zero-level" ("zero-level" is a differential-zero input signal for any of the 16-RGB differential inputs or when the pin voltages to the overlay inputs **ROL** = **GOL** = **BOL** are all equal to **RefoL**), setting the calibration pin **Cal** to a logical "LO" activates the sample phase of auto-calibration and forces the analog outputs to be equal to the reference voltage of pin **RefS**. When pin **Cal** is brought back to a logical "HI", the calibration is held until the next calibration cycle, and the S group will accurately convey the video signal with low offsets. A small hold-step (≤1mV) can be observed whenever the calibration signal is released. Each subsequent activation of the sampling phase refreshes the calibration. If Toggle mode is inactive, the user must individually calibrate both the overlay and non-overlay ("thru") output states by selecting the between them and running calibration separately for both of the input conditions. Changing the input selections by re-programming the crosspoint to another input path or by changing the overlay mode (transparent/opaque), requires refreshing of this calibration. Ideally, the calibration is refreshed once per line of video. The drift during a line of video is negligible. (On the lab bench, using manual control, a drift rate on the order of 0.2mV/sec will be observed.)

Toggle Mode Automatically Supervises the Calibration Cycles

The purpose of Toggle mode is to automatically alternate between calibrating the overlay and calibrating the "thru" paths to the S Output group. The Toggle mode assumes that overlays never exist outside of the video screen (that overlay only occurs during active video). When using the Toggle mode, the overlay function must be inactive during and around sync. When Toggle mode is active and the overlay switch is disabled, the EL4544 will automatically toggle between "thru" and overlay selections for alternate pulsing of the calibrate signal. Thus, every alternate calibrate pulse will override the selected "thru" state of the overlay switch, perform an auto-zero function, and then return the overlay switch back to its original "thru" position. This is true if the programming Bit D1 in Register D (labelled **Toggle**) of the Serial Interface is programmed to a logical "1". Whenever the IC is reset by momentarily pulling the Reset pin "LO", the Toggle mode is initialized such that the first path calibrated is the overlay path. The next calibration cycle will automatically calibrate the "thru" path.

Incorrect Use of the Toggle Mode

If the overlay is selected during auto-calibration with the Toggle mode active, the "thru" path will never be calibrated. Only the overlay gets calibrated in this configuration.

Integrated Die Temperature Probes

Thermal monitoring pins **TMon1** and **TMon2** allow the user to effectively monitor the die temperature by lightly forward biasing internal diodes and measuring their forward voltage drop. Since these diodes will have a -2mV/°C tempco, they can be an effective means of evaluating the thermal management of the user's application board and may even be configured to provide a thermally-triggered shutdown. To implement this feature, pull either of these pins below the negative supply with precision current source of 10µA to 100µA. Measure the forward drop at room temperature with the chip disabled. During operation, every 1°C rise in temperature will produce a 2mV drop in the forward voltage.

Some Tips on the Most Effective Programming of the EL4544

The video inputs present a 1.75kΩ single ended and a 3.5kΩ differential load to an incoming video signal. Since this load

is in parallel with the external termination network, it has a consistent effect on the system gain. To maintain this consistency, it is inadvisable to program more than one input stage (**Ai**, **Bi**, **Ci**, or **Di**) to "look" at any given video input (RGB0, RGB1, …, RGBF) since each activated input stage puts an additional parallel load of 3.5kΩ onto the selected input. When programming the serial interface this is simply expressed as: Avoid programming the same value into the four data registers (for **Ai**, **Bi**, **Ci**, and **Di**) at hex addresses 0H, 1H, 2H, and 3H. They should all have unique values. This is important since if any inputs are selected more than once, their gains will mismatch an input that has only been selected once.

If one wishes to broadcast the same signal to multiple output channels, this can easily be accomplished without violating the advice of the previous paragraph. Select the input that needs to be broadcast using any one of the four input selectors (**Ai**, **Bi**, **Ci**, or **Di**), then have any of up to five of the output stages (**Ax**, **Bx**, **Cx**, **Dx**, **Sx**) point to the input stage that is pointing to the desired input signal. These are selected using hex 8H, 9H, AH, BH, and CH. Now the EL4544 is broadcasting a single video source to multiple outputs without excessively loading down the selected input.

Sync Decoding of EL4544

The EL4544 is designed to receive and decode Horizontal and Vertical Sync signals that have been encoded as common-mode signals of the Red, Green, and Blue Video inputs. The EL4543 provides this encoding as shown in Table 1.

TABLE 1. SYNC SIGNAL ENCODING

H	V	COMMON MODE A (RED)	COMMON MODE B (GREEN)	COMMON MODE C (BLUE)
Low	High	3.0	2.0	2.5
Low	Low	2.5	3.0	2.0
High	Low	2.0	3.0	2.5
High	High	2.5	2.0	3.0

The EL4544 decodes the common-mode signals into H and V syncs as follows: Horizontal Sync is TRUE when the Blue_Common_Mode voltage is greater than the Average_of_Red_and_Green_Common_Mode voltage. Vertical Sync is TRUE when the Average_of_Red_and_Blue_Common_Mode voltage is greater than the Green_Common_Mode voltage. The sync comparators have an internal symmetrical hysteresis that is less than ±50mV. Timing skews between comparators under all conditions are less than one pixel. The comparators have an input common mode that allows for operation at least 1V from the negative supplies and at least 1.5V from the positive supplies.

Logic Levels for Serial Interface and Control Logic

TABLE 2. INPUT LOGIC THRESHOLD (+5V SUPPLY)

V_{LO}, max	0.8V
V_{HI}, min	2V

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

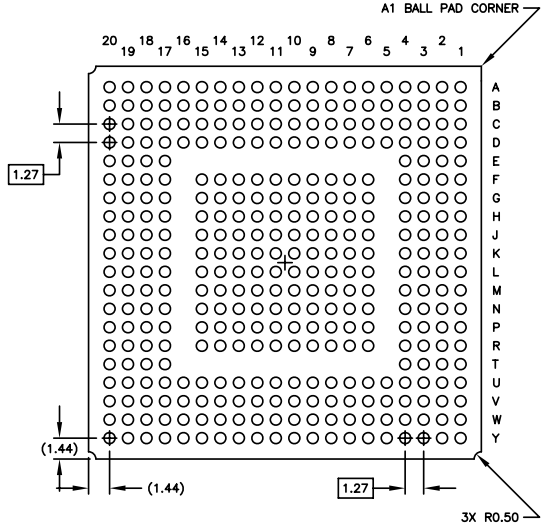
Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

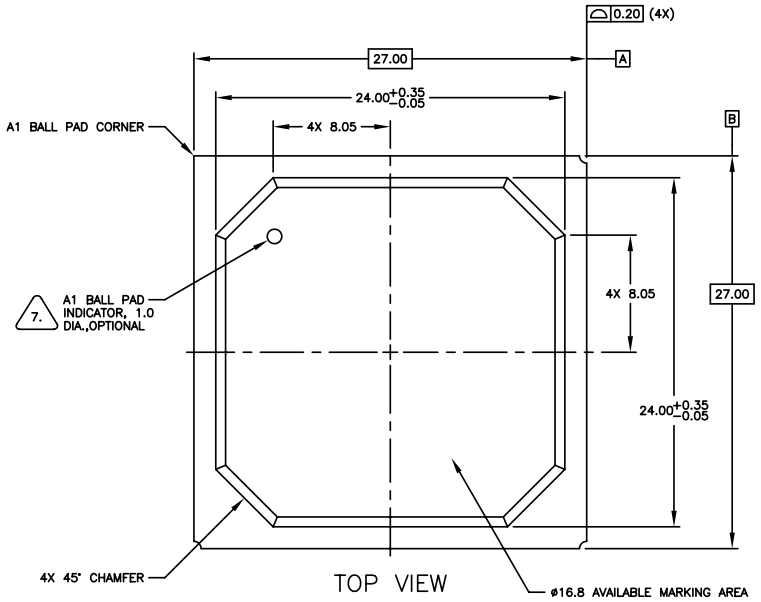
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.27mm.
3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 20 X 20.
4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 400.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. A1 BALL PAD CORNER I.D. FOR PLATE MOLD: TO BE MARKED BY INK. AUTO MOLD: DIMPLE TO BE FORMED BY MOLD CAP.
8. REFERENCE SPECIFICATIONS:
   A. THIS DRAWING CONFORMS TO THE JEDEC REGISTERED OUTLINE MS–034/A VARIATION BAL–2.

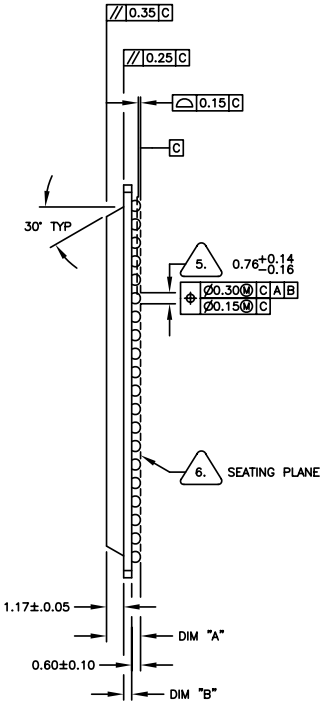


BOTTOM VIEW

356 SOLDER BALLS



TOP VIEW



SIDE VIEW

Drawing #: V356.27x27	PACKAGE OUTLINE DRAWING– 356 PBGA 27 x 27 mm x 1.17 mm MOLD CAP, 1.27 mm PITCH SUBSTRATE
Rev: 0	
Date: 2/28/06	
Units: mm	

NO. LAYERS	DIM "A"	DIM "B"	NOTES
4	2.38±0.21	0.61±0.06	STANDARD
PBGA THICKNESS SCHEDULE			