Low Power, Precision Analog Microcontroller with Dual Sigma-Delta ADC, ARM Cortex-M3

Enhanced Product

ADuCM362-EP

FEATURES

- Analog input/output: dual 24-bit ADCs
  - Programmable ADC conversion rate (3.5 Hz to 3.906 kHz)
  - Simultaneous 50 Hz/60 Hz noise rejection
    - At 50 Hz continuous conversion mode
    - At 16.67 Hz single conversion mode
- Flexible input mux for input channel selection to both ADCs
- Two 24-bit multichannel ADCs (ADC0 and ADC1)
  - 6 differential or 12 single-ended input channels
  - 4 internal channels for monitoring DAC, temperature sensor, IOVDD/4, and AVDD/4 (ADC1 only)
  - Programmable gain (1 to 128)
  - Gain of 1 with input buffer on/off supported
  - RMS noise: 0.052 µV at 3.53 Hz and 0.2 µV at 50 Hz
- Programmable sensor excitation current sources
- On-chip precision voltage reference
  - Two external reference options supported by both ADCs
- Single 12-bit voltage output DAC
  - NPN mode for 4 mA to 20 mA loop applications
- Microcontroller
  - ARM Cortex-M3 32-bit processor
  - Serial wire download and debug
  - Internal watch crystal for wake-up timer
  - 16 MHz oscillator frequency with 8-way programmable divider
- Memory
  - 256 kB Flash/EE memory, 24 kB SRAM
  - In-circuit debug/download via serial wire and UART
- Power supply voltage range: 1.8 V to 3.6 V
- Power consumption, MCU active mode
  - Core consumes 290 µA/MHz
  - Overall system current consumption of 1 mA with core operating at 500 kHz (both ADCs on, input buffers off, PGA gain of 4, 1 × SPI port on, and all timers on)
- Power consumption, power-down mode: 4 µA (wake-up timer active)
- On-chip peripherals
  - 2× UART, I^2C, and 2 × SPI serial input/output (I/O)
  - 16-bit pulse-width modulation (PWM) controller
  - 19-pin multifunction GPIO port
  - 2 general-purpose timers
  - Wake-up timer and watchdog timer
  - Multichannel DMA and interrupt controller
    - DMA support for both SPI channels
- Package and temperature range
  - 48-lead, 7 mm × 7 mm LFCSP
  - Specified for −55°C to +125°C operation
- Multiple diagnostic functions that support safety integrity level (SIL) certification

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Weapons and munitions
- Avionics
- Unmanned systems
- Intelligent precision sensing systems

Rev. 0 Document Feedback

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REVISION HISTORY

1/2021—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADuCM362-EP is a fully integrated, 3.906 kHz, 24-bit data acquisition (DAQ) system that incorporates dual, high performance, multichannel Σ-Δ analog-to-digital converters (ADCs), a 32-bit ARM Cortex™-M3 processor, and Flash/EE memory on a single chip. The ADuCM362-EP is designed for direct interfacing to external precision sensors in both wired and battery-powered applications.

The ADuCM362-EP contains an on-chip 32 kHz oscillator and an internal 16 MHz high frequency oscillator. The high frequency oscillator is routed through a programmable clock divider from which the operating frequency of the processor core clock is generated. The maximum core clock speed is 16 MHz. This clock speed is not limited by operating voltage or temperature.

The microcontroller core is a low power ARM Cortex-M3 processor, 32-bit RISC machine that offers up to 20 MIPS peak performance. The Cortex-M3 processor incorporates a flexible, 11-channel direct memory access (DMA) controller that supports all wired communication peripherals (both serial peripheral interfaces (SPIs), both universal asynchronous receivers/transmitters (UARTs), and I^2C). Also integrated on chip is 256 kB of nonvolatile Flash/EE memory and 24 kB of SRAM.

The analog subsystem consists of dual ADCs, each connected to a flexible input mux. Both ADCs can operate in fully differential and single-ended modes. Other on-chip ADC features include dual programmable excitation current sources, diagnostic current sources, and a bias voltage generator of AVDD_REG/2 (900 mV) to set the common-mode voltage of an input channel. A low-side internal ground switch is provided to allow power-down of an external circuit (for example, a bridge circuit) between conversions. Optional input buffers are provided for the analog inputs and the external reference inputs. These buffers can be enabled for all programmable gain amplifier (PGA) gain settings.

The ADCs contain two parallel filters: a sinc3 or sinc4 filter in parallel with a sinc2 filter. The sinc3 or sinc4 filter is used for precision measurements. The sinc2 filter is used for fast measurements and for the detection of step changes in the input signal.

The ADuCM362-EP contains a low noise, low drift internal band gap reference, but the device can be configured to accept one or two external reference sources in ratiometric measurement configurations. An option to buffer the external reference inputs is provided on chip. A single-channel buffered voltage output DAC is also provided on chip.

The ADuCM362-EP integrates a range of on-chip peripherals that can be configured under microcontroller software control as required in the application. The peripherals include two UARTs, an I^2C, and dual SPI serial I/O communication controllers, a 19-pin general-purpose input/output (GPIO) port, two general-purpose timers, a wake-up timer, and a system watchdog timer. A 16-bit PWM controller with six output channels is also provided.

The ADuCM362-EP is specifically designed to operate in battery-powered applications where low power operation is critical. The microcontroller core can be configured in a normal operating mode that consumes 290 μA/MHz (including flash/SRAM I_{DD}). An overall system current consumption of 1 mA can be achieved with both ADCs on (input buffers off), a PGA gain of 4, one SPI port on, and all timers on.

The ADuCM362-EP can be configured in a number of low power operating modes under direct program control, including a hibernate mode (internal wake-up timer active) that consumes only 4 μA. In hibernate mode, peripherals, such as external interrupts or the internal wake-up timer, can wake up the devices. This mode allows the devices to operate with ultralow power while still responding to asynchronous external or periodic events.

On-chip factory firmware supports in-circuit serial download via a serial wire interface (2-pin JTAG system) and UART. Nonintrusive emulation is also supported via the serial wire interface. These features are incorporated into a low cost QuickStart™ Development System that supports this precision analog microcontroller family.

The device operates from an external 1.8 V to 3.6 V voltage supply and is specified over the −55°C to +125°C temperature range.

Additional application and technical information can be found in the ADuCM362 data sheet.

FUNCTIONAL BLOCK DIAGRAM

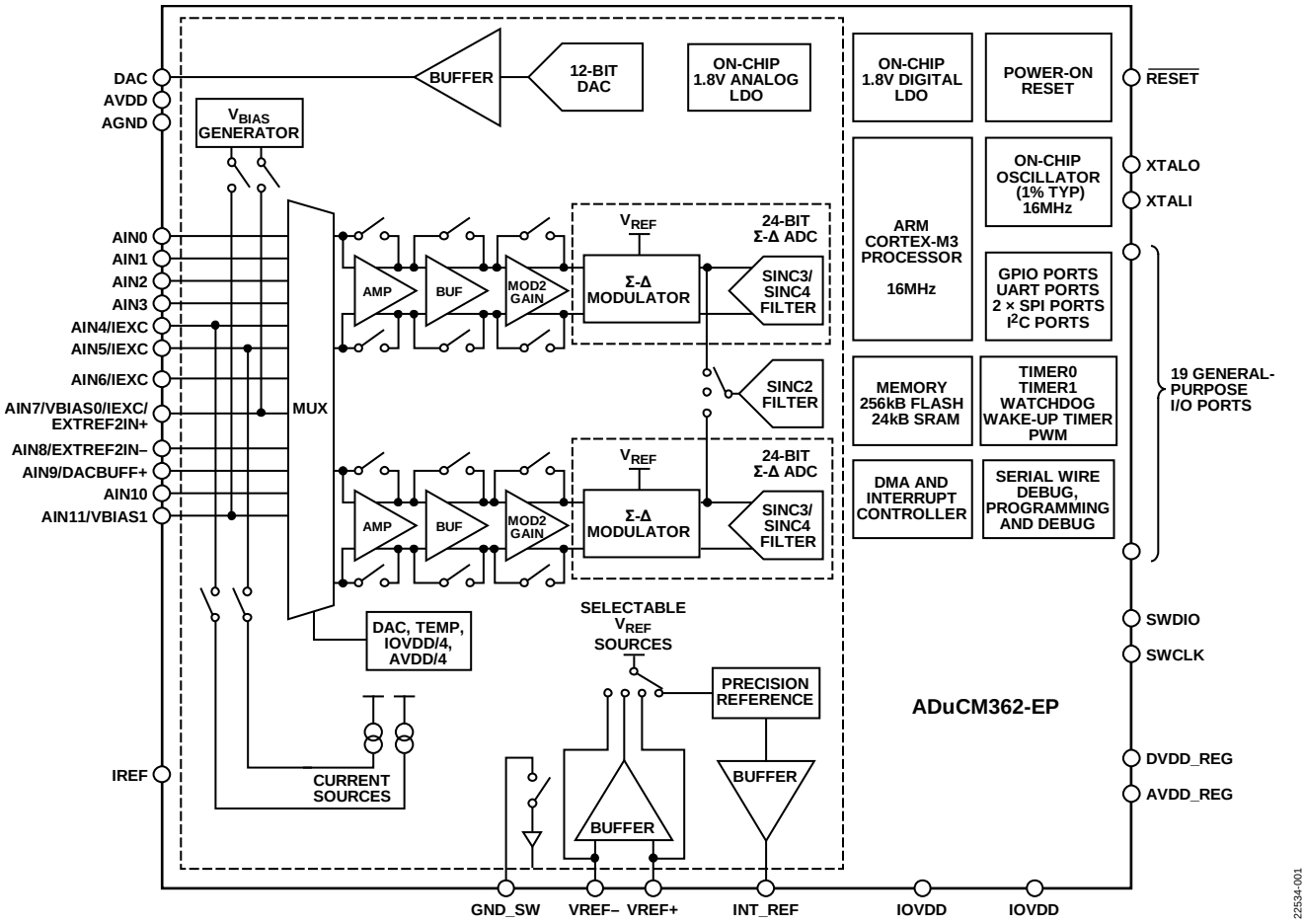


Figure 1.

SPECIFICATIONS

MICROCONTROLLER ELECTRICAL SPECIFICATIONS

AVDD/IOVDD = 1.8 V to 3.6 V, internal 1.2 V reference, core frequency (f_{CORE}) = 16 MHz, and all specifications at T_A = −55°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPECIFICATIONS	ADC0 and ADC1				
Conversion Rate[1]	Chop off	3.5		3906	Hz
	Chop on	3.5		1302	Hz
No Missing Codes[1]	Chop off, ADC frequency (f_{ADC}) ≤ 500 Hz	24			Bits
	Chop on, f_{ADC} ≤ 250 Hz	24			Bits
Integral Nonlinearity[1]	Gain = 1, input buffer off		±10		ppm of FSR
	Gain = 2, 4, 8, or 16		±15		ppm of FSR
	Gain = 32, 64, or 128		±20		ppm of FSR
Offset Error[2, 3, 4, 5, 6]	Chop off, and the offset error is in the order of the noise for the programmed gain and update rate following calibration		±230/gain		µV
	Chop on[1]		±1.0		µV
Offset Error Drift vs. Temperature[1, 4, 5]	Chop off, gain ≤ 4		1/gain		µV/°C
	Chop off, gain ≥ 8		230		nV/°C
	Chop on		10		nV/°C
Offset Error Lifetime Stability[7]	Gain = 128		1		µV/1000 Hr
Full-Scale Error[1, 4, 5, 6, 8]			±0.5/gain		mV
Full-Scale Error Lifetime Stability[7]	Gain = 128		70		µV/1000 Hr
Gain Error Drift vs. Temperature[1, 4, 5]	External reference				
	Gain = 1, 2, 4, 8, or 16		±3		ppm/°C
	Gain = 32, 64, or 128		±6		ppm/°C
PGA Gain Mismatch Error			±0.15		%
Power Supply Rejection[1]	External reference				
	Chop on, ADC input = 0.25 V, gain = 4	95			dB
	Chop off, ADC input = 7.8 mV, gain = 128	80			dB
	Chop off, ADC input = 1 V, gain = 1	90			dB
Absolute Input Voltage Range					
Unbuffered Mode		AGND		AVDD	V
Buffered Mode	Available for all gain settings, G = 1 to 128	AGND + 0.1		AVDD − 0.1	V
Differential Input Voltage Ranges[1]					
	Gain = 1			±V_{REF}	V
	Gain = 2			±500	mV
	Gain = 4			±250	mV
	Gain = 8			±125	mV
	Gain = 16			±62.5	mV
Common-Mode Voltage, V_{CM}[1]	Ideally, V_{CM} = ((AIN+) + (AIN−))/2 and gain = 2 to 128, where AIN+ or AIN− refers to any ADC input pin in which the sign indicates a positive or negative voltage input, respectively	AGND		AVDD	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Current[9]					
Buffered Mode	Gain > 1 (excluding AIN4, AIN5, AIN6, and AIN7 pins)		1		nA
	Gain > 1 (AIN4, AIN5, AIN6, and AIN7 pins)		2		nA
Unbuffered Mode	Input current varies with input voltage		860		nA/V
Average Input Current Drift[1]					
Buffered Mode	AIN1, AIN3, AIN5, AIN7, and AIN11		±5		pA/°C
	AIN0, AIN4, AIN9, and AIN10		±9		pA/°C
	AIN2, AIN6, and AIN8		±15		pA/°C
Unbuffered Mode			±250		pA/V/°C
Common-Mode Rejection, DC[1]	On ADC input				
	ADC gain = 1, AVDD < 2 V	65	100		dB
	ADC gain = 1, AVDD > 2 V	80	100		dB
	ADC gain = 2 to 128	80			dB
Common-Mode Rejection, 50 Hz/60 Hz[1]	50 Hz/60 Hz ± 1 Hz, f_{ADC} = 16.67 Hz with chop on, and f_{ADC} = 50 Hz with chop off				
	ADC gain = 1	97			dB
	ADC gain = 2 to 128	90			dB
Normal Mode Rejection, 50 Hz/60 Hz[1]	On ADC input				
	50 Hz/60 Hz ± 1 Hz, f_{ADC} = 16.67 Hz with chop on and f_{ADC} = 50 Hz with chop off	60	80		dB
TEMPERATURE SENSOR[1]	After user calibration				
Voltage Output at 25°C	Processor powered down or in standby mode before measurement		82.1		mV
Voltage Temperature Coefficient			250		µV/°C
Accuracy			6		°C
GROUND SWITCH					
On Resistance (R_{ON})		3.7	10	19	Ω
Allowable Current[1]	20 kΩ resistor off, direct short to ground			20	mA
VOLTAGE REFERENCE	ADC internal reference				
Internal Reference Voltage (V_{REF})			1.2		V
Initial Accuracy	Measured at T_A = 25°C	−0.1		+0.1	%
Reference Temperature Coefficient[1, 10]		−15	±5	+15	ppm/°C
Power Supply Rejection[1]		82	90		dB
EXTERNAL REFERENCE INPUTS					
Input Range					
Buffered Mode		AGND + 0.1		AVDD − 0.1	V
Unbuffered Mode	Minimum differential voltage between VREF+ and VREF− pins is 400 mV	0		AVDD	V
Input Current					
Buffered Mode		−20	+10	+27	nA
Unbuffered Mode			500		nA/V
Normal Mode Rejection[1]			80		dB
Common-Mode Rejection[1]		85	100		dB
Reference Detect Levels[1]			400		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
EXCITATION CURRENT SOURCES					
Output Current	Available from each current source, value programmable from 10 µA to 1 mA	10		1000	µA
Initial Tolerance at 25°C[1]	Output current (I_{OUT}) ≥ 50 µA		±5		%
Drift[1]	Using internal reference resistor		100	400	ppm/°C
	Using external 150 kΩ reference resistor between IREF pin and AGND, and the resistor must have a drift specification of 5 ppm/°C		75	400	ppm/°C
Initial Current Matching at 25°C[1]	Matching between both current sources		±0.5		%
Drift Matching[1]			50		ppm/°C
Load Regulation, AVDD[1]	AVDD = 3.3 V		0.2		%/V
Output Compliance[1]	I_{OUT} = 10 µA to 210 µA	AGND – 0.03		AVDD – 0.85	V
	I_{OUT} > 210 µA	AGND – 0.03		AVDD – 1.1	V
DAC CHANNEL SPECIFICATIONS	Load resistance (R_L) = 5 kΩ and load capacitance (C_L) = 100 pF				
Voltage Range	Internal reference	0		V_{REF}	V
	External reference	0		1.8	V
DC Specifications[11]					
Resolution		12			Bits
Relative Accuracy			±3		LSB
Differential Nonlinearity	Guaranteed monotonic		±0.5	±1	LSB
Offset Error	1.2 V internal reference		±2	±10	mV
Gain Error	V_{REF} range (reference = 1.2 V)			±0.5	%
NPN Mode[1]					
Resolution		12			Bits
Relative Accuracy			±3		LSB
Differential Nonlinearity			±0.5		LSB
Offset Error			±0.35		mA
Gain Error			±0.75		mA
Output Current Range		0.008		23.6	mA
Interpolation Mode[1, 12]	Only monotonic to 14 bits				
Resolution			14		Bits
Relative Accuracy	For 14-bit resolution		±6		LSB
Differential Nonlinearity	Monotonic (14 bits)		±0.6		LSB
Offset Error	1.2 V internal reference		±2		mV
Gain Error	V_{REF} range (reference = 1.2 V)		±1		%
	AVDD range		±1		%
DAC AC CHARACTERISTICS[1]					
Voltage Output Settling Time			10		µs
Digital-to-Analog Glitch Energy	1 LSB change at major carry (maximum number of bits changes simultaneously in the DACDAT register)		±20		nV-sec
POWER-ON RESET (POR)					
POR Trip Level	Voltage at IOVDD pin				
	Power-on level		1.65		V
	Power-down level		1.65		V
Timeout from POR[1]			50		ms
WATCHDOG TIMER (WDT)[1]					
Timeout Period		0.00003		8192	sec
Timeout Step Size	Register T3CON, Bits[3:2] (PRE) = 10		7.8125		ms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FLASH/EE MEMORY[1]					
Endurance[13]	T_A = −40°C to +125°C	10,000			Cycles
Read	T_A = −55°C to +125°C	10,000			Cycles
Write	T_A = −55°C to −40°C	1000			Cycles
Data Retention[14]	T_J = 85°C	10			Years
DIGITAL INPUTS	All digital inputs				
Input Leakage Current	Digital inputs except for the $\overline{\text{RESET}}$, SWCLK, and SWDIO pins				
Logic 1	High input voltage (V_{INH}) = IOVDD or V_{INH} = 1.8 V		140		µA
	Internal pull-up disabled		1		nA
Logic 0	Low input voltage (V_{INL}) = 0 V		160		µA
	Internal pull-up disabled		10		nA
Input Leakage Current	$\overline{\text{RESET}}$, SWCLK, and SWDIO pins				
Logic 1			140		µA
Logic 0			160		µA
Input Capacitance[1]			10		pF
Logic Input Voltage					
V_{INL}				0.2 × IOVDD	V
V_{INH}		0.7 × IOVDD			V
Logic Output Voltage					
High (V_{OH})	Source current (I_{SOURCE}) = 1 mA	IOVDD − 0.4			V
Low (V_{OL})	Sink current (I_{SINK}) = 1 mA			0.4	V
CRYSTAL OSCILLATOR[1]	32.768 kHz crystal inputs				
Logic Input Voltage, XTALI Only[15]					
V_{INL}				0.8	V
V_{INH}		1.7			V
XTALI Capacitance			6		pF
XTALO Capacitance			6		pF
ON-CHIP LOW POWER OSCILLATOR					
Oscillator Frequency			32.768		kHz
Accuracy		−30	±10	+30	%
ON-CHIP HIGH FREQUENCY OSCILLATOR					
Oscillator Frequency			16		MHz
Accuracy	−55°C to +125°C	−1.8		+1.4	%
Long-Term Stability[7]			0.8		°C/1000 Hr
PROCESSOR CLOCK RATE[1]	Nine programmable core clock selections within specified range	0.0625	0.5	16	MHz
Using an External Clock		0.032768		16	MHz
PROCESSOR START-UP TIME[1]					
At Power-On	Includes kernel power-on execution time		41		ms
After Reset Event	Includes kernel power-on execution time		1.44		ms
From Processor Power-Down (Mode 1, Mode 2, and Mode 3)	Clock frequency (f_{CLK}) is the Cortex-M3 core clock		3 to 5		f_{CLK}
From Total Halt or Hibernate Mode (Mode 4 or Mode 5)			30.8		µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER REQUIREMENTS					
Power Supply Voltage Range, V_{DD}	AVDD, IOVDD	1.8		3.6	V
Power Consumption					
I_{DD} (Microcontroller Unit (MCU) Active Mode)[16, 17]	Processor clock rate = 16 MHz, all peripherals on (CLKSYSDIV = 0)		5.5		mA
	Processor clock rate = 8 MHz, all peripherals on (CLKSYSDIV = 1)		3		mA
	Processor clock rate = 500 kHz, both ADCs on (input buffers off) with PGA gain = 4, 1 × SPI port on, and all timers on		1		mA
I_{DD} (MCU Powered Down)	Full temperature range, total halt mode (Mode 4)		4		µA
I_{DD}, Total (ADC0)[17]	PGA enabled, gain ≥ 32		320		µA
PGA	Gain = 4, 8, or 16, PGA only		130		µA
	Gain = 32, 64, or 128, PGA only		180		µA
Input Buffers	2 × input buffers = 70 µA		70		µA
Digital Interface and Modulator			70		µA
I_{DD} (ADC1)	Input buffers off, gain = 4, 8, or 16 only		200		µA
External Reference Input Buffers	60 µA each		120		µA

[1] These numbers are not production tested but are guaranteed by design and/or characterization data at production release.
[2] Tested at gain = 4 after initial offset calibration.
[3] Measured with an internal short. A system zero-scale calibration removes this error.
[4] A recalibration at any temperature removes these errors.
[5] These numbers do not include internal reference temperature drift.
[6] Factory calibrated at gain = 1.
[7] The long term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[8] System calibration at a specific gain removes the error at this gain.
[9] Input current is measured with one ADC measuring a channel. If both ADCs measure the same input channel, the input current increases (approximately doubles).
[10] Measured using the box method.
[11] Reference DAC linearity is calculated using a reduced code range of 0x0AB to 0xF30.
[12] Measured using a low-pass filter with resistance = 1 kΩ and capacitance = 100 nF.
[13] Endurance is qualified to 10,000 cycles as per JEDEC Standard 22, Method A117 and is measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.
[14] Retention lifetime equivalent at T_J = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime derates with junction temperature.
[15] Voltage input levels are relevant only if driving the crystal input from a voltage source. If a crystal is connected directly, the internal crystal interface determines the common-mode voltage.
[16] Typical additional supply current (I_{DD}) consumed during Flash/EE memory program and erase cycles are 7 mA.
[17] Total I_{DD} for ADC includes figures for PGA ≥ 32, input buffers, digital interface, and the Σ-Δ modulator.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVDD to AGND	−0.3 V to +3.96 V
IOVDD to DGND[1]	−0.3 V to +3.96 V
Digital Input Voltage to DGND[1]	−0.3 V to +3.96 V
Digital Output Voltage to DGND[1]	−0.3 V to +3.96 V
Analog Inputs to AGND	−0.3 V to +3.96 V
Temperature	
Operating Range	−55°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Peak Solder Reflow	
SnPb Assemblies (10 sec to 30 sec)	240°C
Pb-Free Assemblies (20 sec to 40 sec)	260°C

[1] DGND is the digital system ground reference.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient, thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case, thermal resistance.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-48-4	28	9.5	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with 25 thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADuCM362-EP

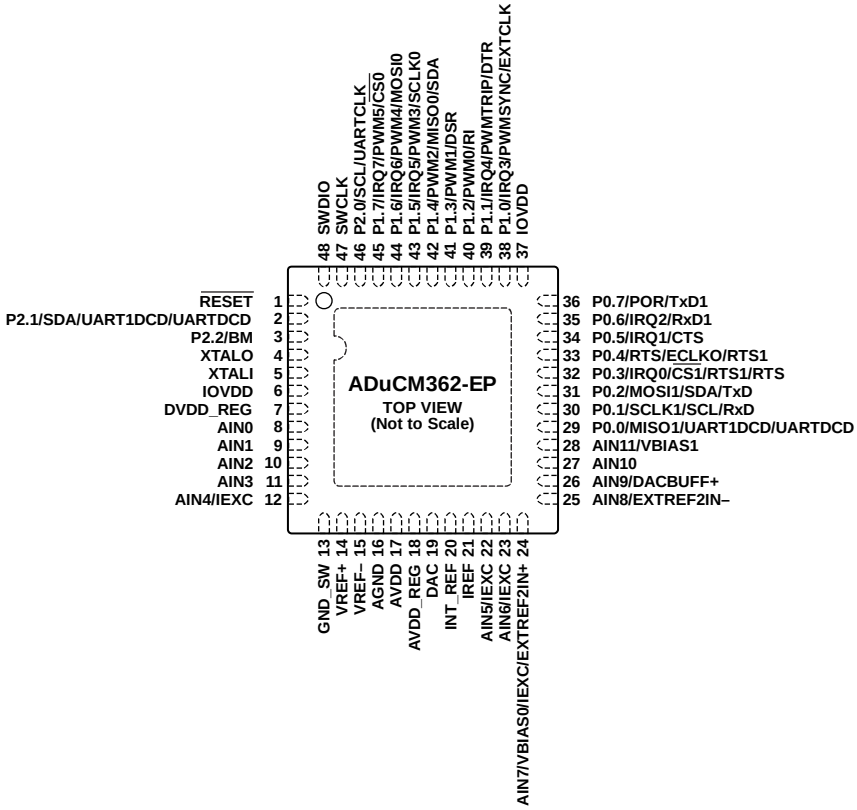
Table 4. ADuCM362-EP, 48-Lead LFCSP

ESD Model	Withstand Threshold	Class
HBM	±2 kV	2
FICDM	±1000 V	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE SOLDERED TO A METAL PLATE ON THE PCB AND TO DGND FOR MECHANICAL REASONS.

22534-007

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Reset Pin, Active Low Input. An internal pull-up is provided.
2	P2.1/SDA/UART1DCD/UARTDCD	General-Purpose Input/Output P2.1/I²C Serial Data Pin/UART1 Data Carrier Detect Pin/UART Data Carrier Detect Pin.
3	P2.2/BM	General-Purpose Input/Output P2.2/Boot Mode Input Select Pin. When the P2.2/BM pin is held low during and for a short time after any reset sequence, the device enters UART download mode.
4	XTALO	External Crystal Oscillator Output Pin. Optional 32.768 kHz source for real-time clock.
5	XTALI	External Crystal Oscillator Input Pin. Optional 32.768 kHz source for real-time clock.
6	IOVDD	Digital System Supply Pin. IOVDD must be connected to the digital system ground reference (DGND) via a 0.1 µF capacitor.
7	DVDD_REG	Digital Regulator Supply. DVDD_REG must be connected to DGND via a 470 nF capacitor and to AVDD_REG (Pin 18).
8	AIN0	ADC Analog Input 0. AIN0 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
9	AIN1	ADC Analog Input 1. AIN1 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
10	AIN2	ADC Analog Input 2. AIN2 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
11	AIN3	ADC Analog Input 3. AIN3 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
12	AIN4/IEXC	ADC Analog Input 4/Excitation Current Source. AIN4 can be configured as a positive or negative input to either ADC in differential or single-ended mode. IEXC can be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1.

Pin No.	Mnemonic	Description
13	GND_SW	Sensor Power Switch to Analog Ground Reference.
14	VREF+	External Reference Positive Input. An external reference can be applied between the VREF+ and VREF− pins.
15	VREF−	External Reference Negative Input. An external reference can be applied between the VREF+ and VREF− pins.
16	AGND	Analog System Ground Reference Pin.
17	AVDD	Analog System Supply Pin. AVDD must be connected to AGND via a 0.1 µF capacitor.
18	AVDD_REG	Internal Analog Regulator Supply Output. AVDD_REG must be connected to AGND via a 470 nF capacitor and to DVDD_REG (Pin 7).
19	DAC	DAC Voltage Output.
20	INT_REF	Internal Reference. INT_REF must be connected to ground via a 470 nF decoupling capacitor.
21	IREF	Optional Reference Current Resistor Connection for the Excitation Current Sources. The reference current used for the excitation current sources is set by a low drift (5 ppm/°C) external resistor connected to IREF.
22	AIN5/IEXC	ADC Analog Input 5/Excitation Current Source. AIN5 can be configured as a positive or negative input to either ADC in differential or single-ended mode. IEXC can also be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1.
23	AIN6/IEXC	ADC Analog Input 6/Excitation Current Source. AIN6 can be configured as a positive or negative input to either ADC in differential or single-ended mode. IEXC can also be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1.
24	AIN7/VBIAS0/IEXC/EXTREF2IN+	ADC Analog Input 7/Bias Voltage Output/Excitation Current Source/External Reference 2 Positive Input. AIN7 can be configured as a positive or negative input to either an ADC in differential or single-ended mode. VBIAS0 can be configured as an analog output pin to generate the bias voltage, VBIAS0, of AVDD_REG/2. IEXC can be configured as the output pin for Excitation Current Source 0 or Excitation Current Source 1. EXTREF2IN+ can be configured as the positive input for External Reference 2.
25	AIN8/EXTREF2IN−	ADC Analog Input 8/External Reference 2 Negative Input. AIN8 can be configured as a positive or negative input to either an ADC in differential or single-ended mode. EXTREF2IN− can be configured as the negative input for External Reference 2.
26	AIN9/DACBUFF+	ADC Analog Input 9/Noninverting Input to the DAC Output Buffer. AIN9 can be configured as a positive or negative input to either an ADC in differential or single-ended mode. DACBUFF+ can be configured as the noninverting input to the DAC output buffer when the DAC is configured for NPN mode.
27	AIN10	ADC Analog Input 10. AIN10 can be configured as a positive or negative input to either ADC in differential or single-ended mode.
28	AIN11/VBIAS1	ADC Analog Input 11/Bias Voltage Output. AIN11 can be configured as a positive or negative input to either an ADC in differential or single-ended mode. VBIAS1 can be configured as an analog output pin to generate the bias voltage, VBIAS1, of AVDD_REG/2 .
29	P0.0/MISO1/UART1DCD/ UARTDCD	General-Purpose Input/Output P0.0/SPI1 Master Input, Slave Output Pin/UART1 Data Carrier Detect Pin/UART Data Carrier Detect Pin.
30	P0.1/SCLK1/SCL/RxD	General-Purpose Input/Output P0.1/SPI1 Serial Clock Pin/I²C Serial Clock Pin/UART Serial Input (Data Input for the UART Downloader).
31	P0.2/MOSI1/SDA/TxD	General-Purpose Input/Output P0.2/SPI1 Master Output, Slave Input Pin/I²C Serial Data Pin/ UART Serial Output (Data Output for the UART Downloader).
32	P0.3/IRQ0/$\overline{\text{CS1}}$/RTS1/RTS	General-Purpose Input/Output P0.3/External Interrupt Request 0/SPI1 Chip Select Pin, Active Low (When Using SPI1, Configure as $\overline{\text{CS1}}$)/UART1 Request to Send Signal/UART Request to Send Signal.
33	P0.4/RTS/ECLKO/RTS1	General-Purpose Input/Output P0.4/UART Request to Send Signal/External Clock Output Pin for Test Purposes/UART1 Request to Send Signal.
34	P0.5/IRQ1/CTS	General-Purpose Input/Output P0.5/External Interrupt Request 1/UART Clear to Send Signal.
35	P0.6/IRQ2/RxD1	General-Purpose Input/Output P0.6/External Interrupt Request 2/UART1 Serial Input.
36	P0.7/POR/TxD1	General-Purpose Input/Output P0.7/Power-On Reset Pin (Active High)/UART1 Serial Output.
37	IOVDD	Digital System Supply Pin. IOVDD must be connected to DGND via a 0.1 µF capacitor.

Pin No.	Mnemonic	Description
38	P1.0/IRQ3/PWMSYNC/EXTCLK	General-Purpose Input/Output P1.0/External Interrupt Request 3/PWM External Synchronization Input/External Clock Input Pin.
39	P1.1/IRQ4/PWMTRIP/DTR	General-Purpose Input/Output P1.1/External Interrupt Request 4/PWM External Trip Input/ UART Data Terminal Ready Pin.
40	P1.2/PWM0/RI	General-Purpose Input/Output P1.2/PWM0 Output/UART Ring Indicator Pin.
41	P1.3/PWM1/DSR	General-Purpose Input/Output P1.3/PWM1 Output/UART Data Set Ready Pin.
42	P1.4/PWM2/MISO0/SDA	General-Purpose Input/Output P1.4/PWM2 Output/SPI0 Master Input, Slave Output Pin/I^2C Serial Data Pin.
43	P1.5/IRQ5/PWM3/SCLK0	General-Purpose Input/Output P1.5/External Interrupt Request 5/PWM3 Output/SPI0 Serial Clock Pin.
44	P1.6/IRQ6/PWM4/MOSI0	General-Purpose Input/Output P1.6/External Interrupt Request 6/PWM4 Output/SPI0 Master Output, Slave Input Pin.
45	P1.7/IRQ7/PWM5/$\overline{CS0}$	General-Purpose Input/Output P1.7/External Interrupt Request 7/PWM5 Output/SPI0 Chip Select Pin, Active Low (When Using SPI0, Configure as $\overline{CS0}$).
46	P2.0/SCL/UARTCLK	General-Purpose Input/Output P2.0/I^2C Serial Clock Pin/Input Clock Pin for UART Block Only.
47	SWCLK	Serial Wire Debug Clock Input Pin.
48	SWDIO	Serial Wire Debug Data Input/Output Pin.
	EP	Exposed Pad. The exposed pad must be soldered to a metal plate on the PCB and to DGND for mechanical reasons.

TYPICAL PERFORMANCE CHARACTERISTICS

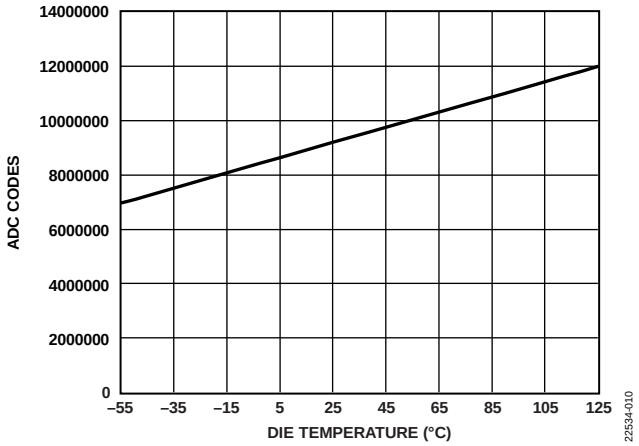
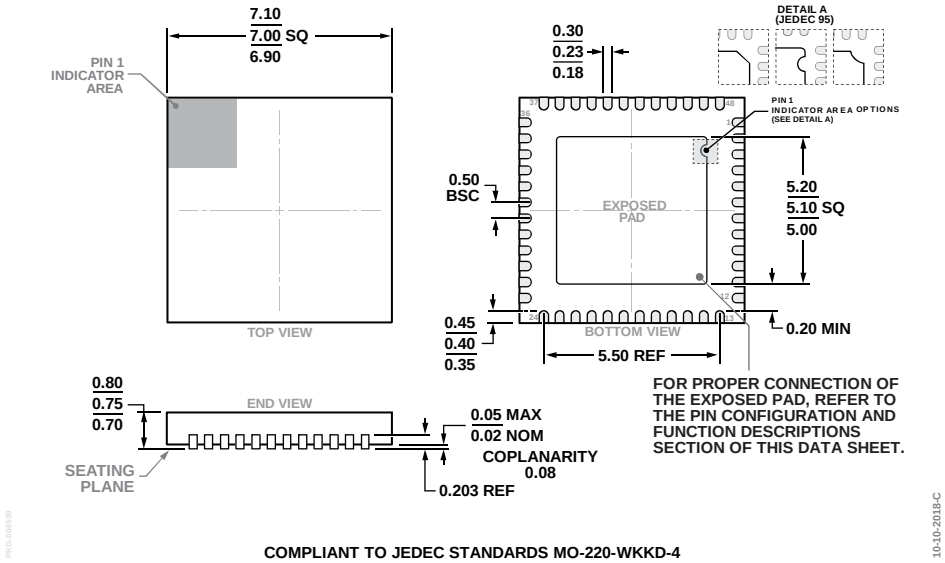


Figure 3. ADC Codes (Decimal Values) vs. Die Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD-4

Figure 4. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	ADCs	Flash/EE and SRAM	Temperature Range	Package Description	Package Option
ADuCM362TCPZ56EPR7	Dual 24-Bit	256 kB and 24 kB	−55°C to +125°C	48-Lead LFCSP	CP-48-4

[1] Z = RoHS-Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).