Common Drain Dual N -Channel Enhancement Mode MOSFET

MTA17A02CDV8

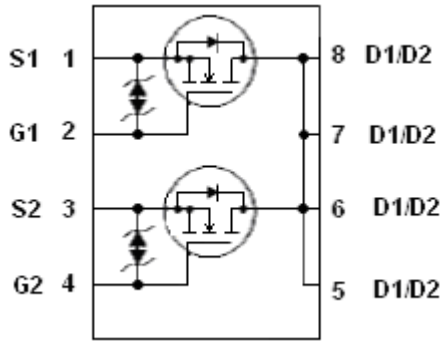
BV_{DSS}		20V
I_D	V_{GS}=4.5V	6.6A
R_{DSON} (TYP.)	V_{GS}=4.5V, I_D=6A	19.5mΩ
	V_{GS}=4.0V, I_D=6A	20.0mΩ
	V_{GS}=3.0V, I_D=6A	21.7 mΩ
	V_{GS}=2.5V, I_D=6A	23.4 mΩ

Features

- Simple drive requirement
- Low gate charge
- Low on-resistance
- Fast switching speed
- ESD protected
- Pb-free lead plating and halogen-free package

Equivalent Circuit

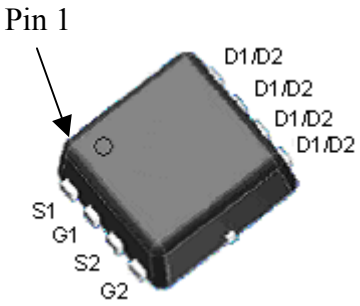
MTA17A02CDV8



G：Gate S：Source D：Drain

Outline

DFN3×3



Ordering Information

Device	Package	Shipping
MTA17A02CDV8-0-T6-G	DFN3×3 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel

Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

Packing spec, T6 : 3000 pcs / tape & reel,13” reel

Product rank, zero for no rank products

Product name

Absolute Maximum Ratings (Ta=25°C, unless otherwise specified)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current @ V_{GS}=4.5V, T_C=25°C		I_D	16.5	A
Continuous Drain Current @ V_{GS}=4.5V, T_C=100°C			10.4	
Continuous Drain Current @ V_{GS}=4.5V, T_A=25°C			6.6	
Continuous Drain Current @ V_{GS}=4.5V, T_A=70°C			5.3	
Pulsed Drain Current		I_{DM}	40 *1, 2	
Total Power Dissipation	T_A=25℃	P_D	2.5 *3	W
	T_A=70℃		1.6 *3	
Operating Junction and Storage Temperature Range		Tj, Tstg	-55~+150	°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	8	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	50 *3	°C/W

Note : 1. Pulse width limited by maximum junction temperature.
2. Duty cycle≤1%.
3. Surface mounted on a 1 in² pad of 2oz copper. In practice $R_{th,j-a}$ will be determined by the customer's PCB characteristics.

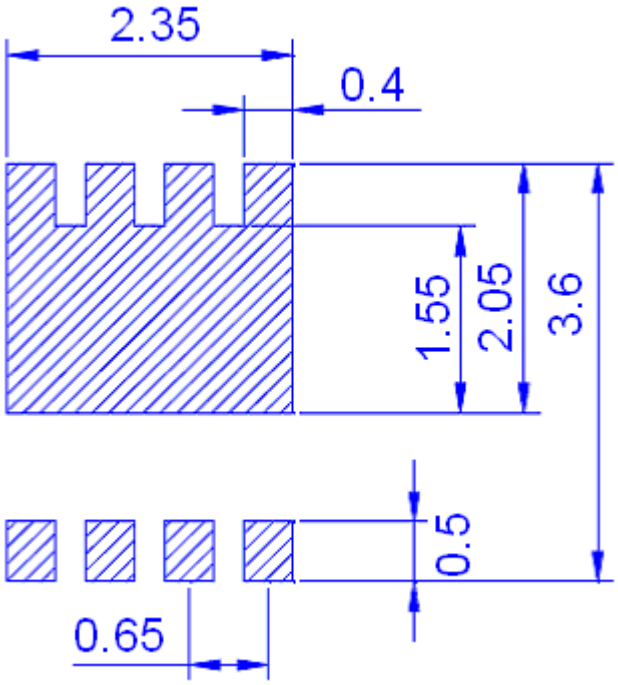
Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	20	-	-	V	V_{GS}=0V, I_D=250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.02	-	V/°C	Reference to 25°C, I_D=250μA
$V_{GS(th)}$	0.5	0.63	1.0	V	V_{DS}=V_{GS}, I_D=250μA
I_{GSS}	-	-	±10	μA	V_{GS}=±10V, V_{DS}=0V
I_{DSS}	-	-	1		V_{DS}=20V, V_{GS}=0V
	-	-	10		V_{DS}=16V, V_{GS}=0V, Tj=70°C
*$R_{DS(ON)}$	-	19.5	26	mΩ	I_D=6A, V_{GS}=4.5V
	-	20.0	27		I_D=6A, V_{GS}=4V
	-	21.7	30		I_D=6A, V_{GS}=3V
	-	23.4	32		I_D=6A, V_{GS}=2.5V
*G_{FS}	-	15	-	S	V_{DS}=5V, I_D=6A
Dynamic					
Ciss	-	365	-	pF	V_{DS}=10V, V_{GS}=0, f=1MHz
Coss	-	75	-		
Crss	-	30	-		

*$t_{d(ON)}$	-	260	-	ns	V_{DS}=10V, I_D=1A, V_{GS}=4.5V, R_G=6Ω
*t_r	-	670	-		
*$t_{d(OFF)}$	-	3850	-		
*t_f	-	1800	-		
*Qg	-	6.4	-	nC	V_{DS}=16V, I_D=6A, V_{GS}=4.5V
*Qgs	-	1.4	-		
*Qgd	-	1.5	-		
Source-Drain Diode					
*I_S	-	-	3	A	
*I_{SM}	-	-	5		
*V_{SD}	-	0.73	1.2	V	I_S=3A,V_{GS}=0V

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

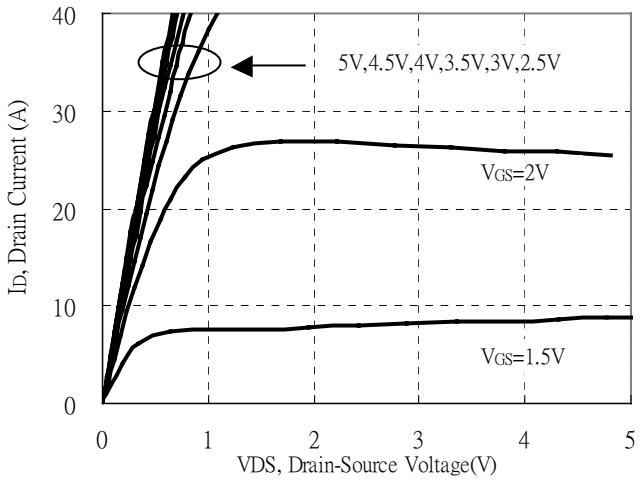
Recommended Soldering Footprint



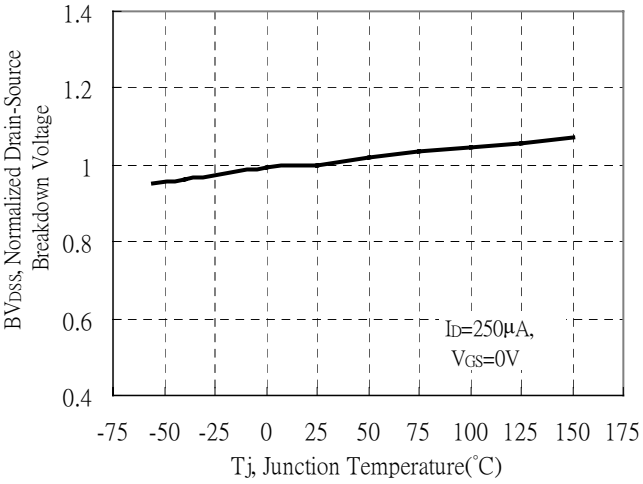
unit : mm

Typical Characteristics

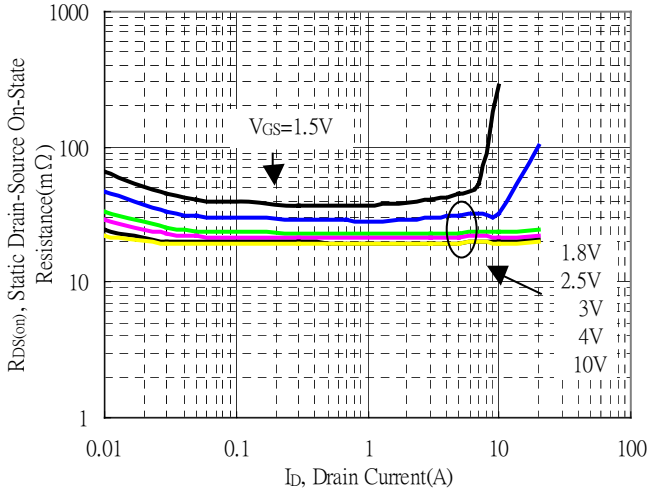
Typical Output Characteristics



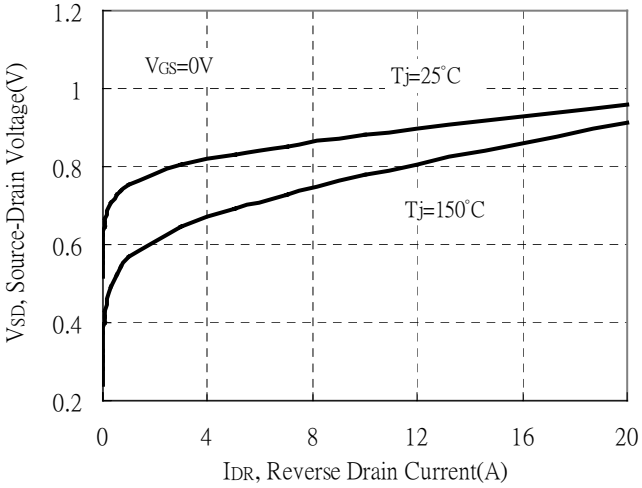
Brekdown Voltage vs Junction Temperature



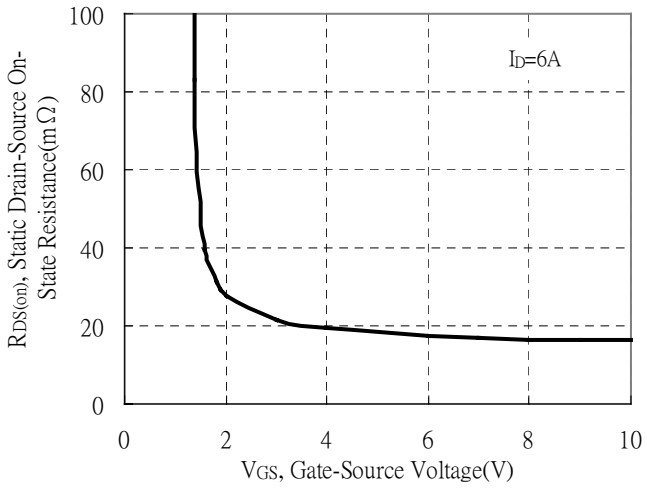
Static Drain-Source On-State resistance vs Drain Current



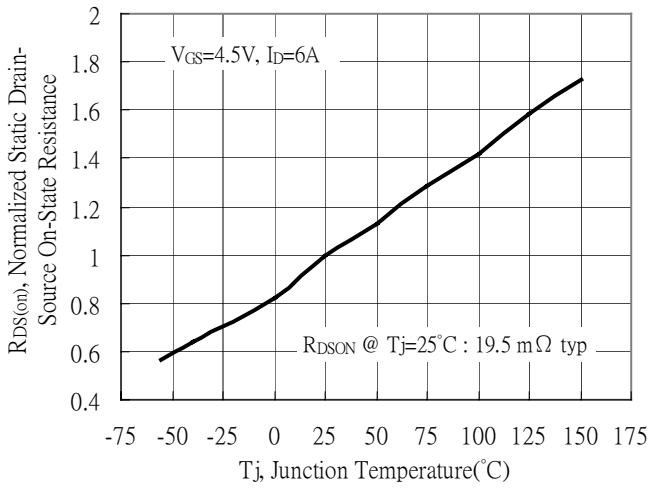
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

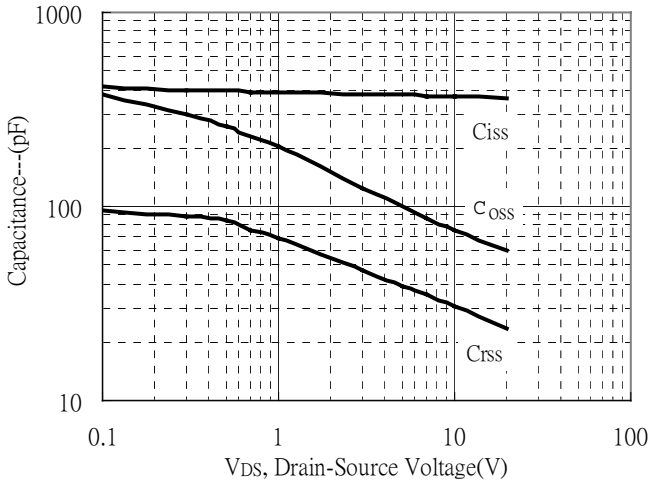


Drain-Source On-State Resistance vs Junction Tempearture

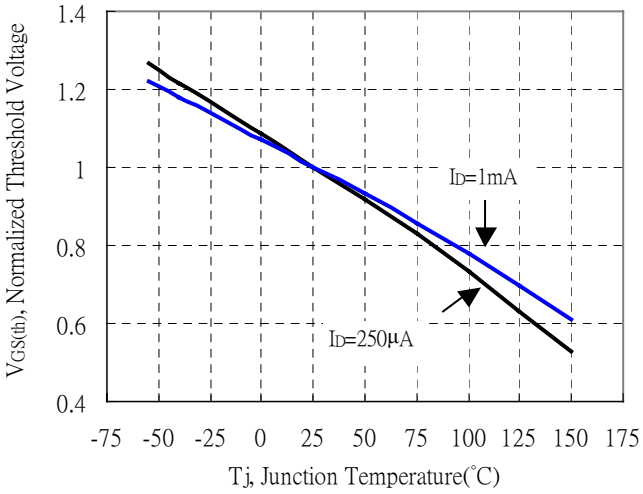


Typical Characteristics(Cont.)

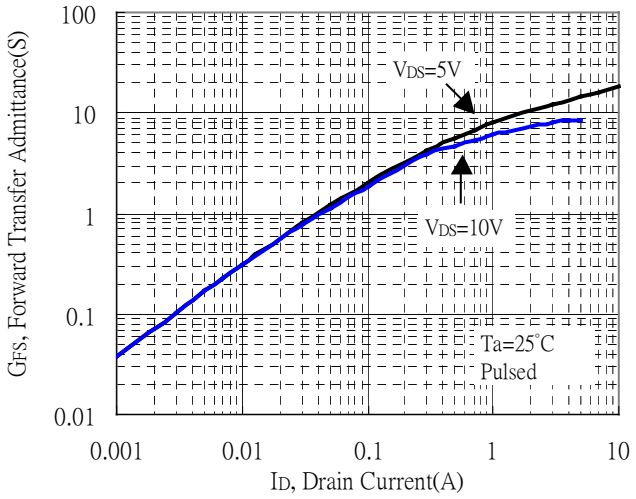
Capacitance vs Drain-to-Source Voltage



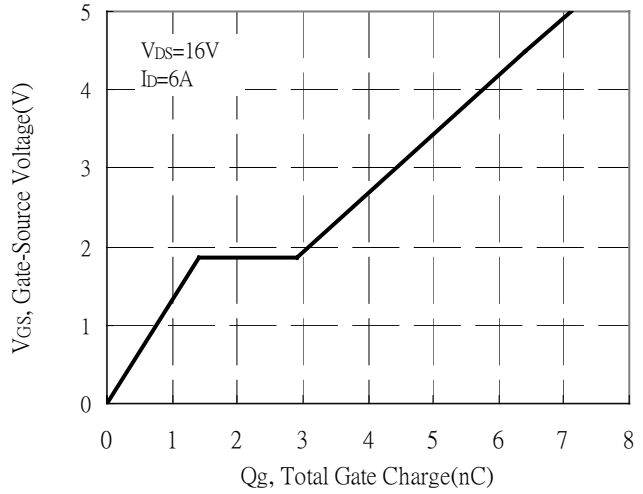
Threshold Voltage vs Junction Tempearture



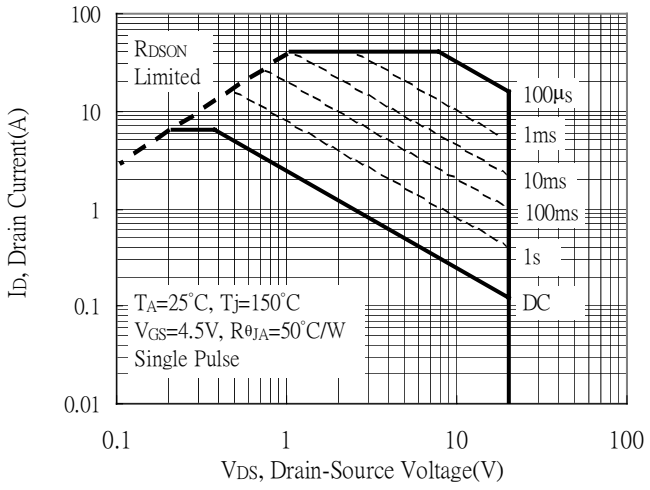
Forward Transfer Admittance vs Drain Current



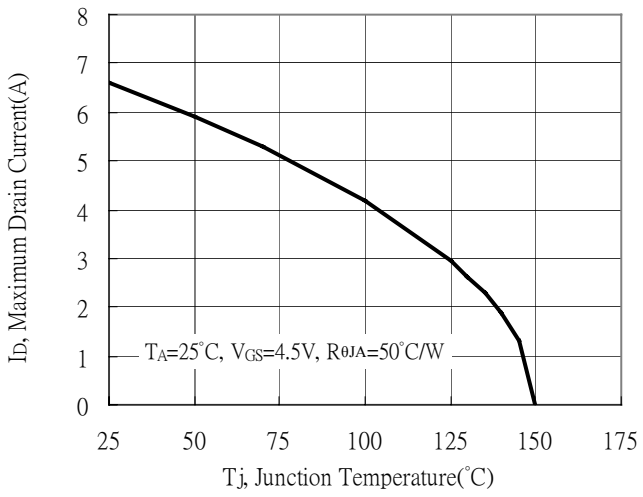
Gate Charge Characteristics



Maximum Safe Operating Area

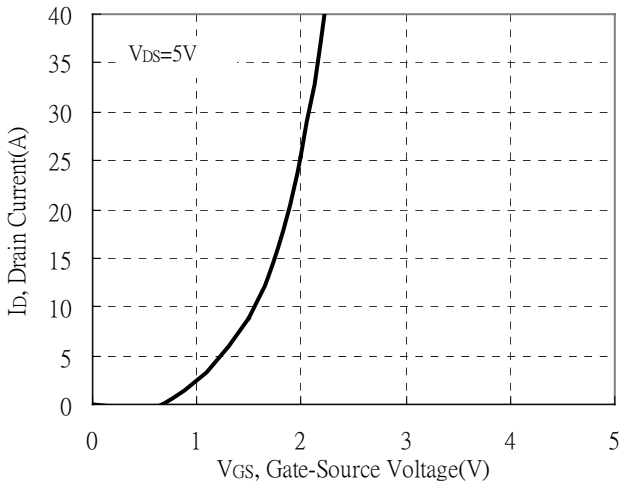


Maximum Drain Current vs Junction Temperature

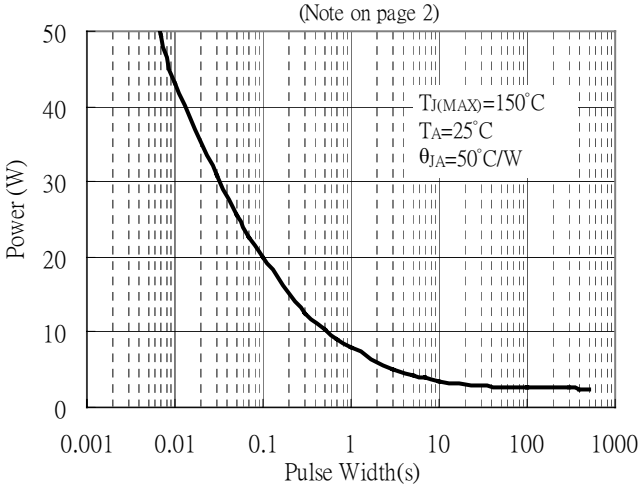


Typical Characteristics(Cont.)

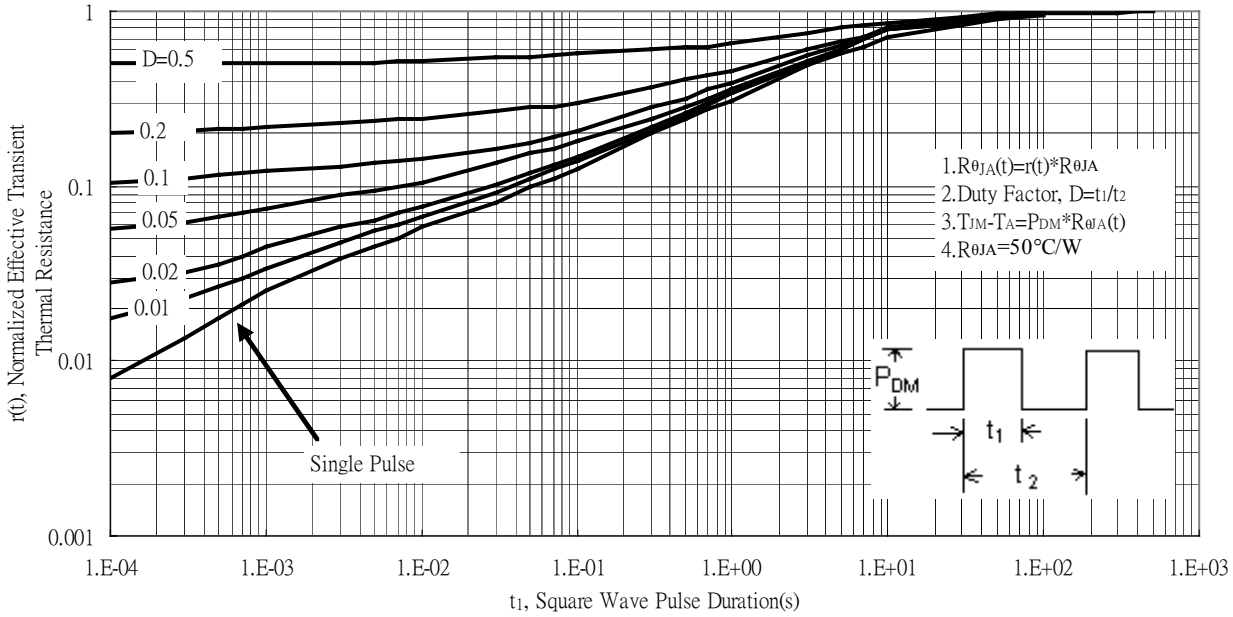
Typical Transfer Characteristics



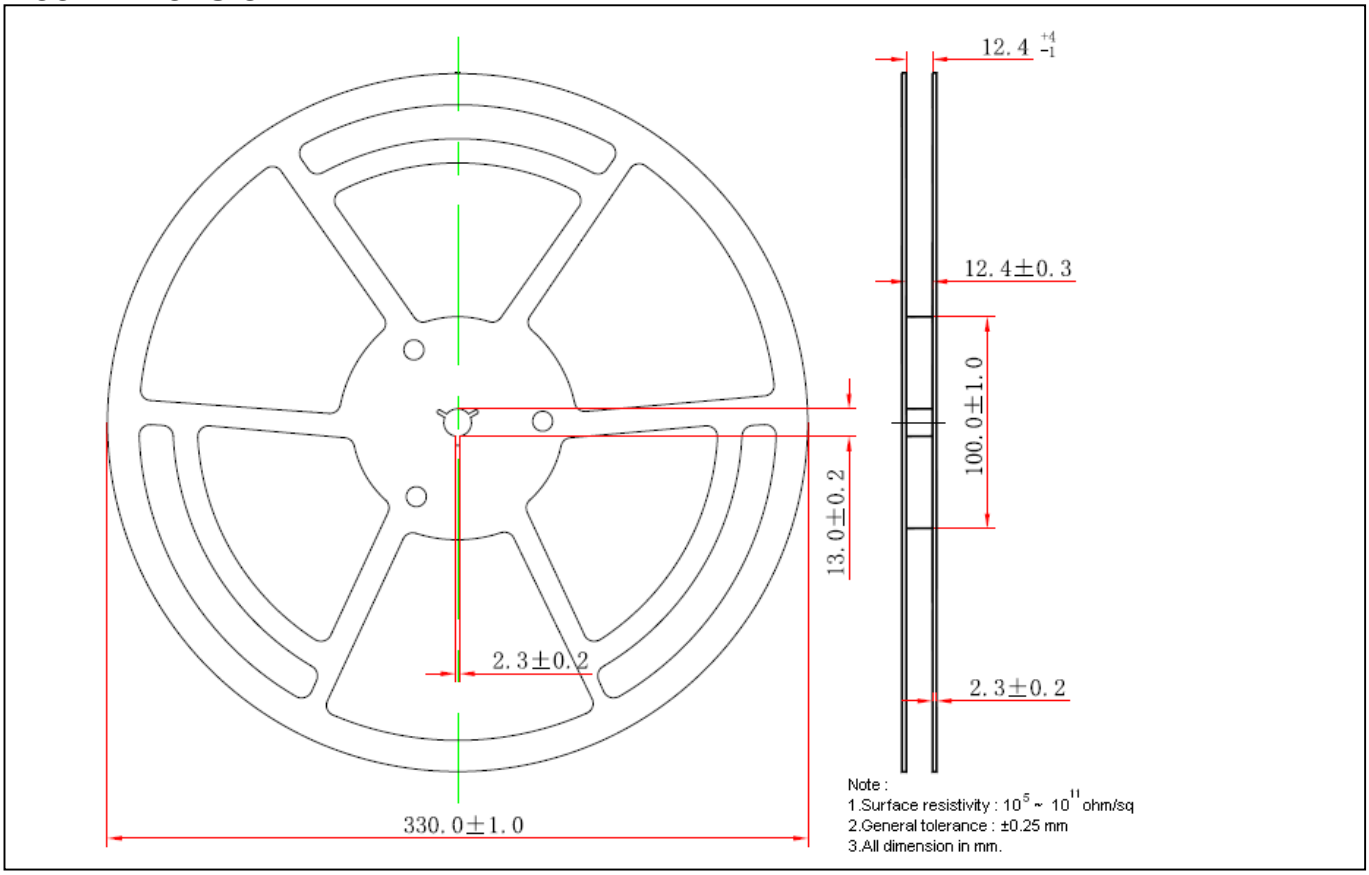
Single Pulse Power Rating, Junction to Ambient
(Note on page 2)



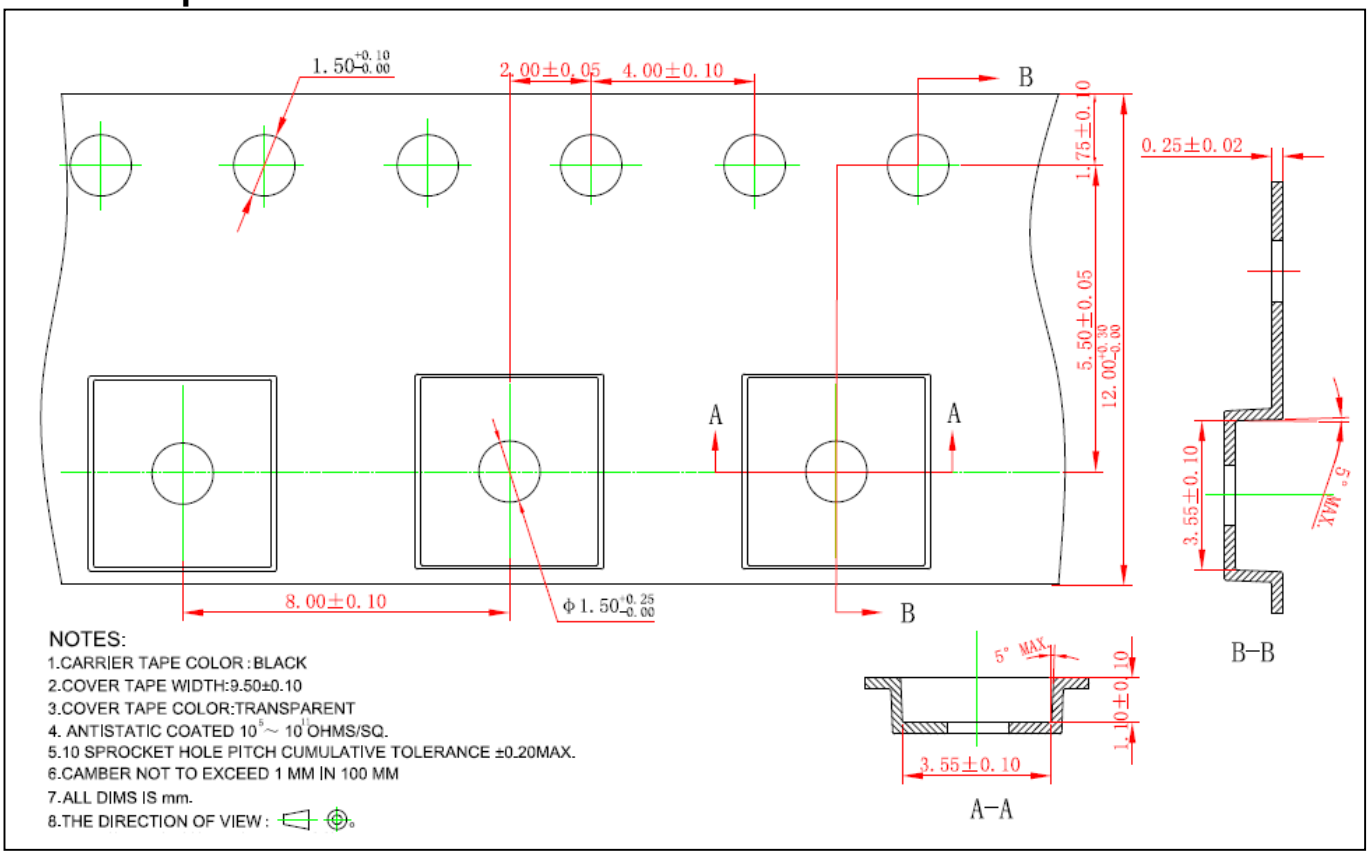
Transient Thermal Response Curves



Reel Dimension



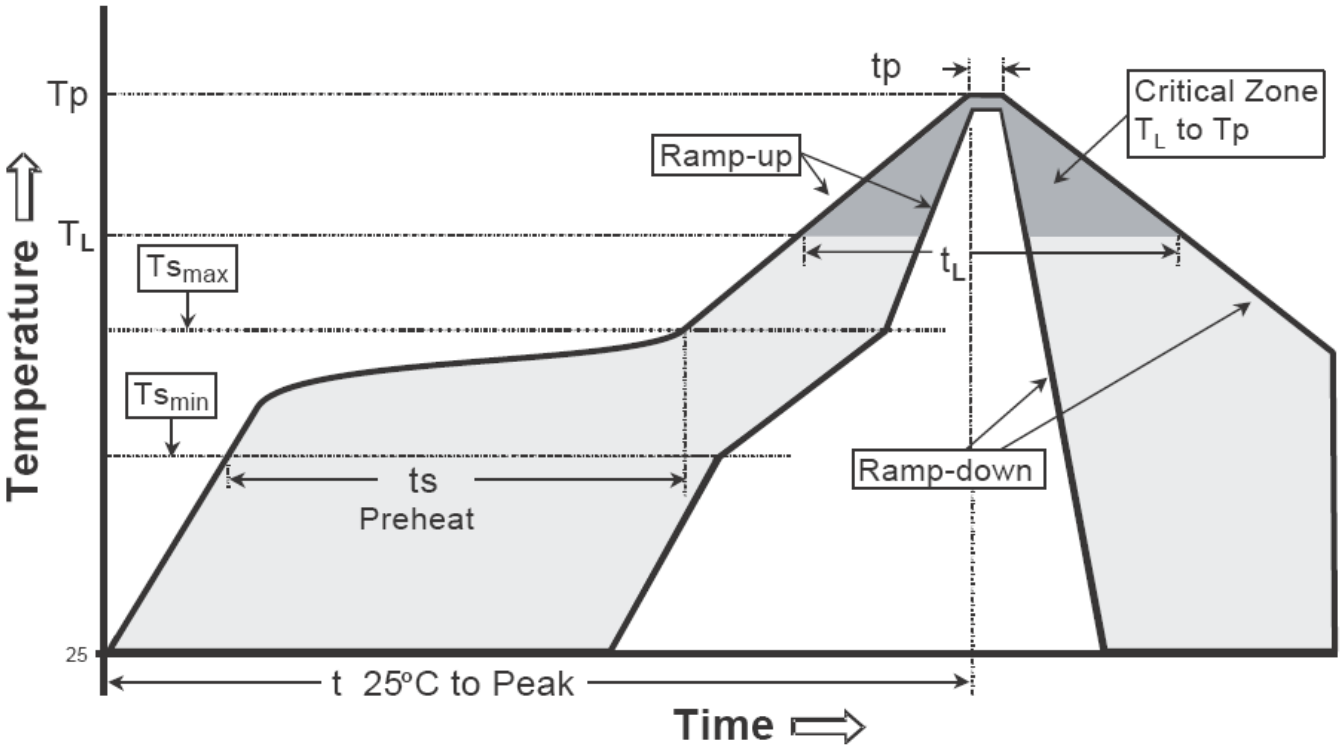
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

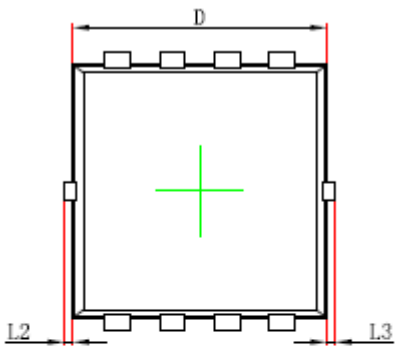
Recommended temperature profile for IR reflow



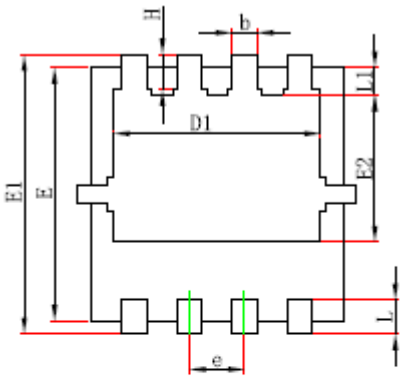
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

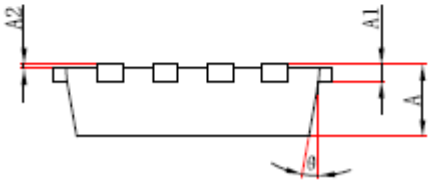
DFN3x3 Dimension



Top View

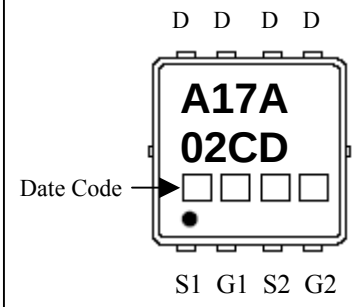


Bottom View



Side View

Marking :



8-Lead DFN3x3 Plastic Package
CYStek Package Code: V8

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033	b	0.200	0.400	0.008	0.016
A1	0.152 REF		0.006 REF		e	0.550	0.750	0.022	0.030
A2	0.000	0.050	0.000	0.002	L	0.300	0.500	0.012	0.020
D	2.900	3.100	0.114	0.122	L1	0.180	0.480	0.007	0.019
D1	2.300	2.600	0.091	0.102	L2	0.000	0.100	0.000	0.004
E	2.900	3.100	0.114	0.122	L3	0.000	0.100	0.000	0.004
E1	3.150	3.450	0.124	0.136	H	0.315	0.515	0.012	0.020
E2	1.535	1.935	0.060	0.076	θ	9°	13°	9°	13°

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.