**SRAM MODULE 1Mbyte (256K x 32-Bit) , 72-Pin**

**Part No. HMS25632M8B, HMS25632Z8B**

## GENERAL DESCRIPTION

The HMS25632M8B is a high-speed static random access memory (SRAM) module containing 262,144 words organized in a x32-bit configuration. The module consists of eight 256K x 4 SRAMs mounted on a 72-pin, double-sided, FR4-printed circuit board.

PD0 to PD3 identify the module's density allowing interchangeable use of alternate density, industry- standard modules. Eight chip enable inputs, (/CE1, /CE2, /CE3 and /CE4) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable(/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW.

Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible.

## FEATURES

- Access times : 8, 10,12, 15 and 20ns
- High-density 1MByte design
- High-reliability high-speed design
- Single + 5V ±0.5V power supply
- Easy memory expansion /CE and /OE functions
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- FR4-PCB design
- Part identification
  - HMS25632M8B : 72-pin SIMM design
  - HMS25632Z8B : 72-pin ZIP design

  → Pin-compatible with the HMS25632M8B

## OPTIONS MARKING

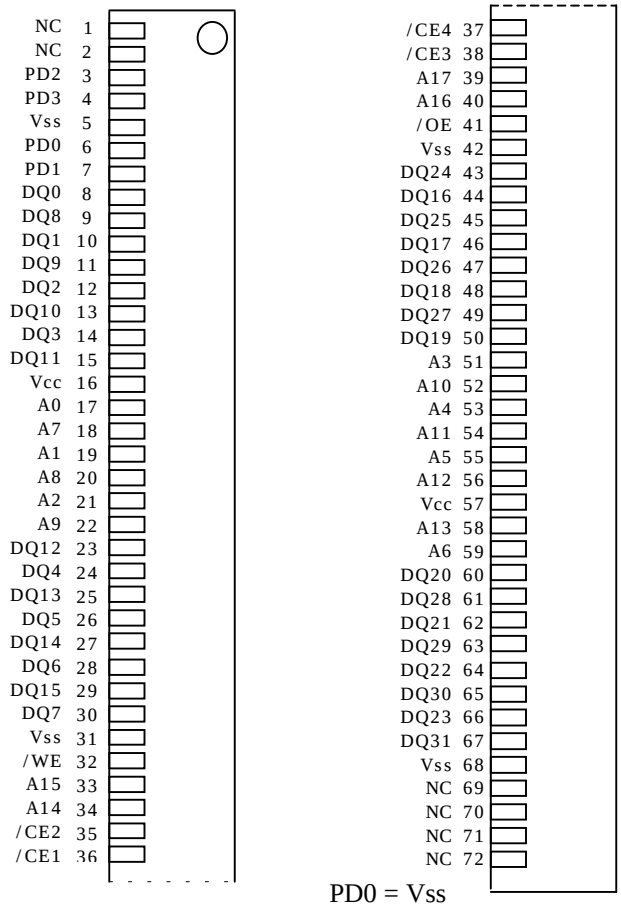
- Timing

| | |
|---|---|
| 10ns access | -10 |
| 12ns access | -12 |
| 15ns access | -15 |
| 20ns access | -20 |

- Packages

| | |
|---|---|
| 72-pin SIMM | M |
| 72-pin ZIP | Z |

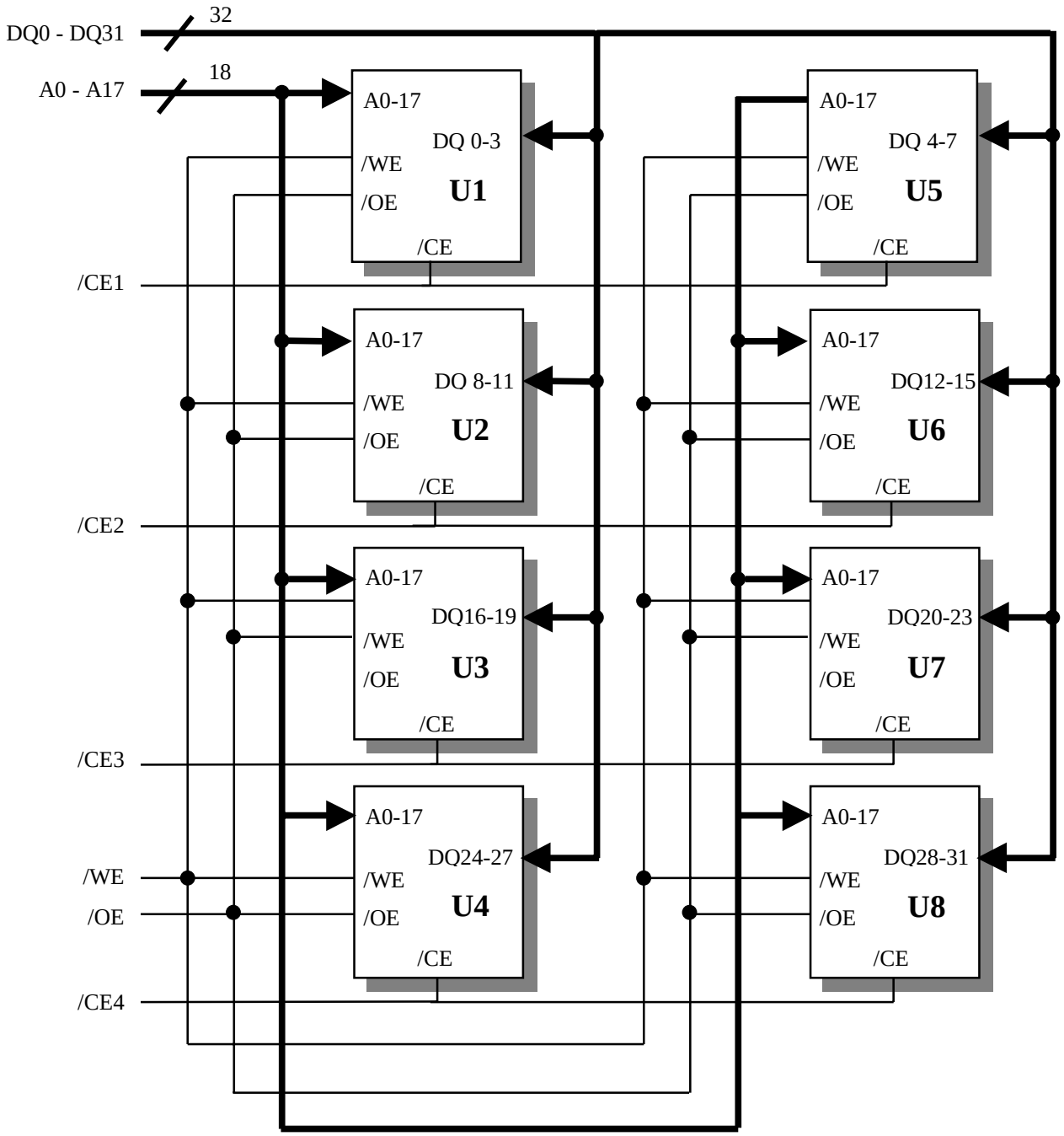
## PIN ASSIGNMENT




72-Pin **SIMM**
**TOP VIEW**

PD0 = Vss
PD1 = Vss
PD2 = Open
PD3 = Open

## FUNCTIONAL BLOCK DIAGRAM




| MODE | /OE | /CE | /WE | OUTPUT | POWER |
|---|---|---|---|---|---|
| STANDBY | X | H | X | HIGH-Z | STANDBY |
| NOT SELECTED | H | L | H | HIGH-Z | ACTIVE |
| READ | L | L | H | Dout | ACTIVE |
| WRITE | X | L | L | Din | ACTIVE |

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING |
|---|---|---|
| Voltage on Any Pin Relative to Vss | $V_{IN,OUT}$ | -0.5V to Vcc+0.5V |
| Voltage on Vcc Supply Relative to Vss | $V_{CC}$ | -0.5V to +7.0V |
| Power Dissipation | $P_D$ | 8W |
| Storage Temperature | $T_{STG}$ | -65°C to +150°C |
| Operating Temperature | $T_A$ | 0°C to +70°C |

- Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS ( $T_A$=0 to 70 °C )

| PARAMETER | SYMBOL | MIN | TYP. | MAX |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5V | 5.0V | 5.5V |
| Ground | $V_{SS}$ | 0 | 0 | 0 |
| Input High Voltage | $V_{IH}$ | 2.2 | - | Vcc+0.5V** |
| Input Low Voltage | $V_{IL}$ | -0.5* | - | 0.8V |

* $V_{IL}$(Min.) = -2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

****** $V_{IH}$(Min.) = Vcc+2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

## DC AND OPERATING CHARACTERISTICS (1)(0°C ≤ $T_A$ ≤ 70 °C ; Vcc = 5V ± 0.5V )

| PARAMETER | TEST CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Input Leakage Current | $V_{IN}$ = Vss to Vcc | $IL_I$ | -2 | 2 | μA |
| Output Leakage Current | /CE=$V_{IH}$ or /OE =$V_{IH}$ or /WE=$V_{IL}$<br>$V_{OUT}$=Vss to $V_{CC}$ | $IL_0$ | -2 | 2 | μA |
| Output High Voltage | $I_{OH}$ = -4.0Ma | $V_{OH}$ | 2.4 | | V |
| Output Low Voltage | $I_{OL}$ = 8.0mA | $V_{OL}$ | | 0.4 | V |

* Vcc=5.0V, Temp=25 °C

## DC AND OPERATING CHARACTERISTICS (2)

| DESCRIPTION | TEST CONDITIONS | SYMBOL | MAX | | | UNIT |
|---|---|---|---|---|---|---|
| | | | -12 | -15 | -20 | |
| Power Supply Current: Operating | Min. Cycle, 100% Duty<br>/CE=$V_{IL}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$,<br>$I_{OUT}$=0mA | $I_{CC}$ | 70 | 68 | 65 | mA |
| Power Supply Current: Standby | Min. Cycle, /CE=$V_{IH}$ | $I_{SB}$ | 30 | 30 | 30 | mA |
| | f=0MHZ, /CE≥$V_{CC}$-0.2V,<br>$V_{IN}$≥ $V_{CC}$-0.2V or $V_{IN}$≤0.2V | $I_{SB1}$ | 5 | 5 | 5 | mA |

## CAPACITANCE

| DESCRIPTION | TEST CONDITIONS | SYMBOL | MAX | UNIT |
|---|---|---|---|---|
| Input /Output Capacitance | $V_{I/O}$=0V | $C_{I/O}$ | 8 | pF |
| Input Capacitance | $V_{IN}$=0V | $C_{IN}$ | 6 | pF |

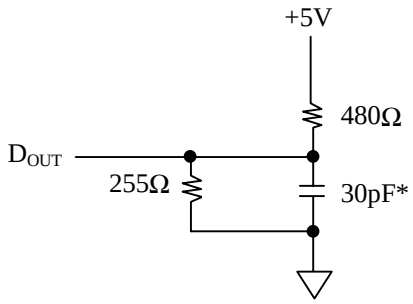
* **NOTE** : Capacitance is sampled and not 100% tested

## AC CHARACTERISTICS ($0^oC \le T_A \le 70\ ^oC$ ; Vcc = 5V ± 0.5V, unless otherwise specified)

**TEST CONDITIONS**

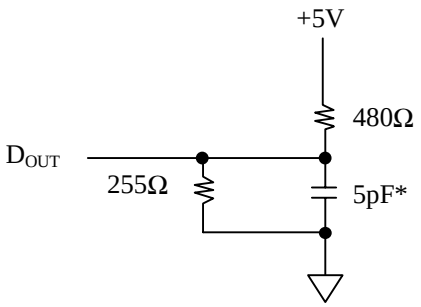
| PARAMETER | VALUE |
|---|---|
| Input Pulse Level | 0 to 3V |
| Input Rise and Fall Time | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See below |

Output Load




Output Load (B)

for $t_{HZ}$, $t_{LZ}$, $t_{WHZ}$, $t_{OW}$, $t_{OLZ}$ & $t_{OHZ}$




## READ CYCLE

| PARAMETER | SYMBOL | -12 | | -15 | | -20 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Read Cycle Time | $t_{RC}$ | 12 | | 15 | | 20 | | ns |
| Address Access Time | $t_{AA}$ | | 12 | | 15 | | 20 | ns |
| Chip Select to Output | $t_{CO}$ | | 12 | | 15 | | 20 | ns |
| Output Enable to Output | $t_{OE}$ | | 6 | | 7 | | 9 | ns |
| Output Enable to Low-Z Output | $t_{OLZ}$ | 0 | | 0 | | 0 | | ns |
| Chip Enable to Low-Z Output | $t_{LZ}$ | 3 | | 3 | | 3 | | ns |
| Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 6 | 0 | 7 | 0 | 9 | ns |
| Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 6 | 0 | 7 | 0 | 9 | ns |
| Output Hold from Address Change | $t_{OH}$ | 3 | | 3 | | 3 | | ns |
| Chip Select to Power Up Time | $t_{PU}$ | - | | 0 | | 0 | | ns |

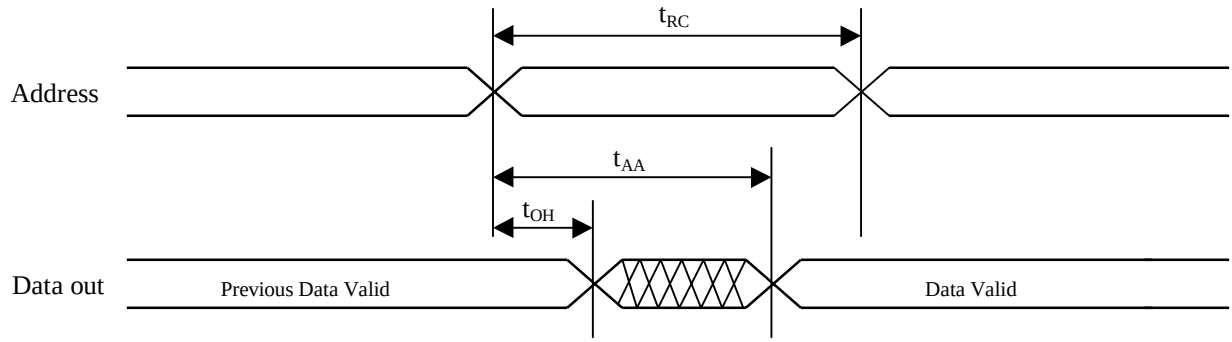
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Chip Select to Power Down Time | $t_{PD}$ | - | 12 | | 15 | | 20 | ns |

## WRITE CYCLE

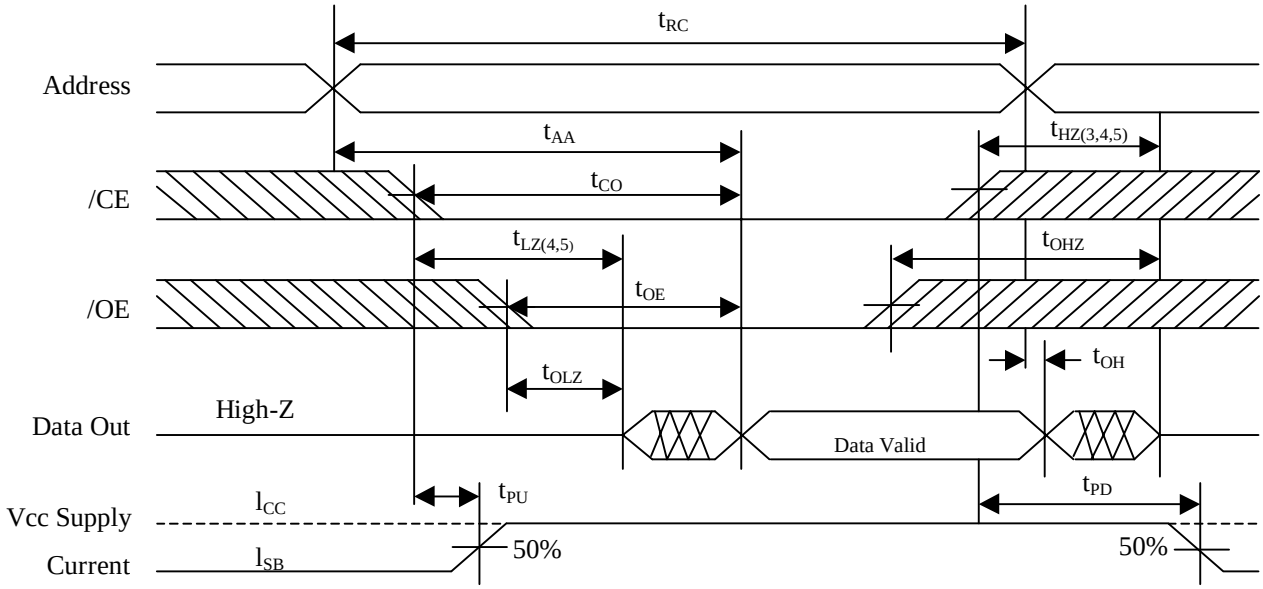
| PARAMETER | SYMBOL | -12 | | -15 | | -20 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Write Cycle Time | $t_{WC}$ | 12 | | 15 | | 20 | | ns |
| Chip Select to End of Write | $t_{CW}$ | 8 | | 9 | | 10 | | ns |
| Address Set-up Time | $t_{AS}$ | 0 | | 0 | | 0 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 8 | | 9 | | 10 | | ns |
| Write Pulse Width | $t_{WP}$ | 8 | | 9 | | 10 | | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | 0 | | ns |
| Write to Output High-Z | $t_{WHZ}$ | 0 | 6 | 0 | 7 | 0 | 9 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 6 | | 7 | | 8 | | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | | 0 | | 0 | | ns |
| End of Write to Output Low-Z | $t_{OW}$ | 3 | | 3 | | 5 | | ns |

## TIMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE( Address Controlled) ( /CE = /OE = $V_{IL}$ , /WE = $V_{IH}$)



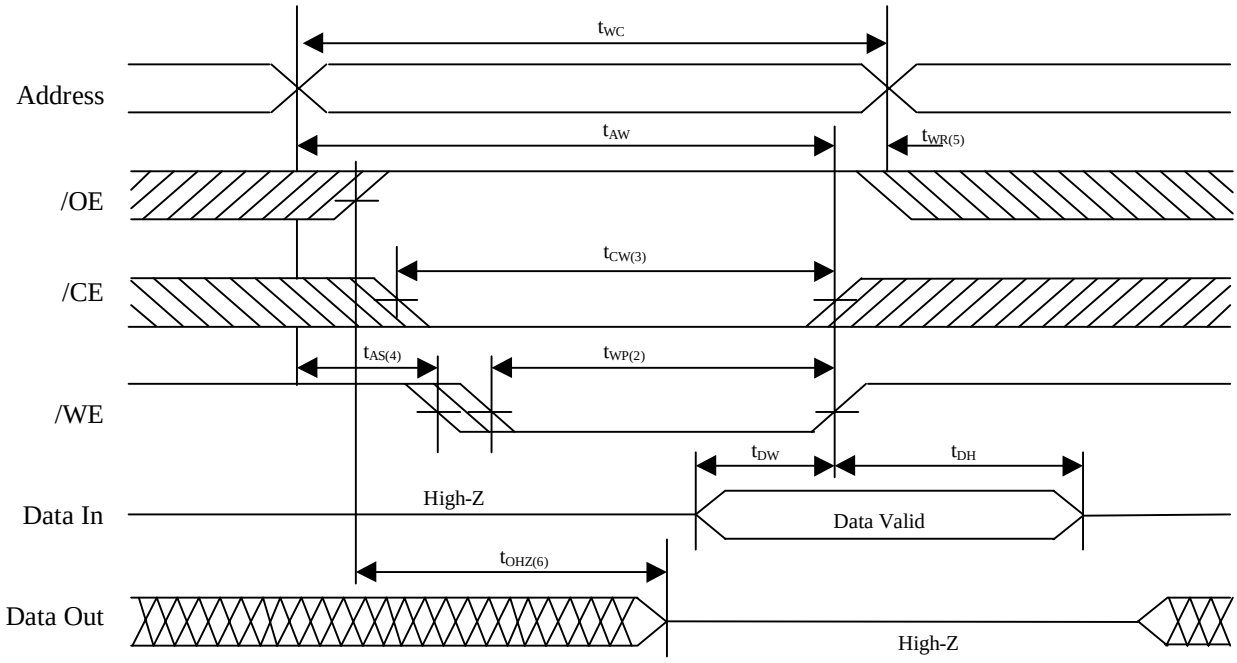
## TIMING WAVEFORM OF READ CYCLE ( /CE Controlled )



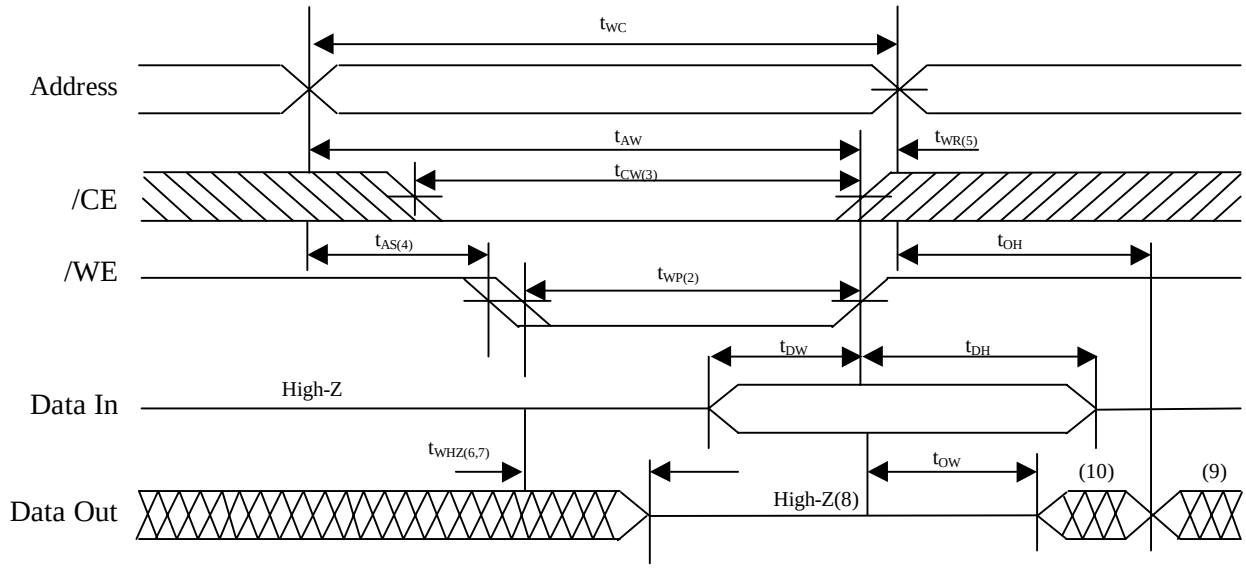

### Notes (Read Cycle)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to first transition address.
3. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to $V_{OH}$ or $V_{OL}$ levels.
4. At any given temperature and voltage condition, $t_{HZ}$ (max.) is less than $t_{LZ}$ (min.) both for a given device and from device to device.
5. Transition is measured ± 200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CE = $V_{IL}$.
7. Address valid prior to coincident with /CE transition low.

## TIMING WAVEFORM OF WRITE CYCLE (/OE = Clock )



**TIMING WAVEFORM OF WRITE CYCLE** (/OE Low Fixed )




**Notes**(Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CE and a low /WE. A write begins at the latest transition among /CE going low and /WE going low : A write ends at the earliest transition among /CE going high and /WE going high. $t_{WP}$ is measured from the beginning of write to the end of write.
3. $t_{CW}$ is measured from the later of /CE going low to the end of write.
4. $t_{AS}$ is measured from the address valid to the beginning of write.
5. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applied in case a write ends as /CE, or /WE going high.
6. If /OE,/CE and /WE are in the read mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CE goes low simultaneously with /WE going low or after /WE going low, the outputs remain high impedance state.
9. $D_{OUT}$ is the read data of the new address.
10. When /CE is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

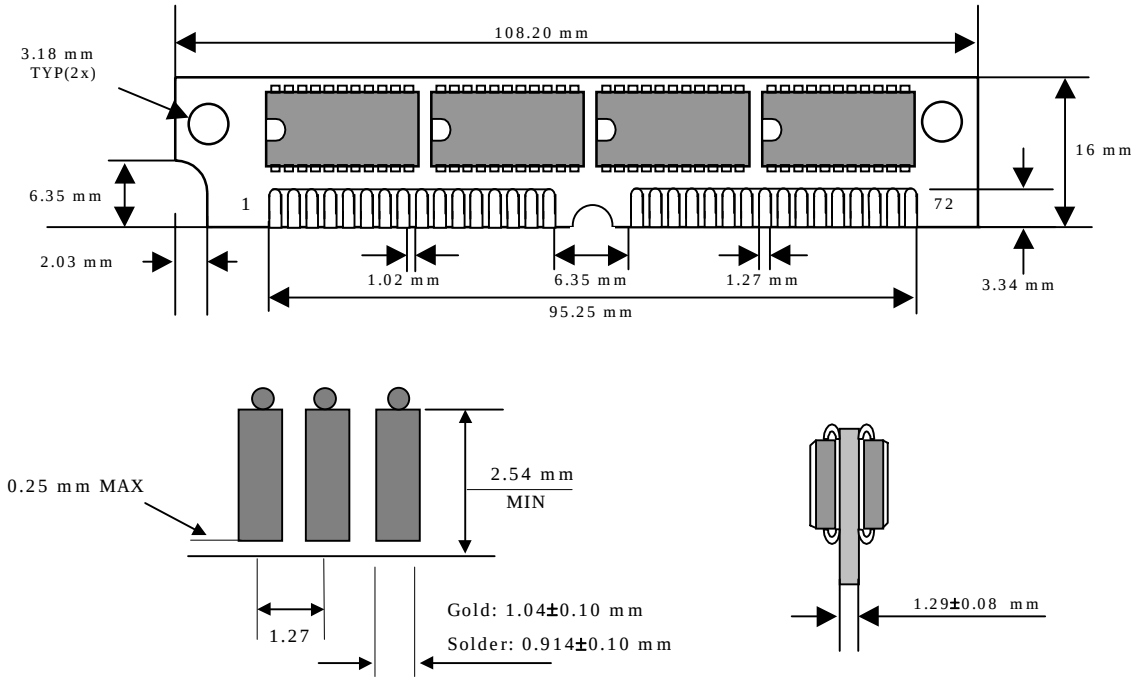
# FUNCTIONAL DESCRIPTION

| /CE | /WE | /OE | MODE | I/O PIN | SUPPLY CURRENT |
|---|---|---|---|---|---|
| H | X* | X | Not Select | High-Z | $l_{SB}$, $l_{SB1}$ |
| L | H | H | Output Disable | High-Z | $l_{CC}$ |
| L | H | L | Read | $D_{OUT}$ | $l_{CC}$ |
| L | L | X | Write | $D_{IN}$ | $l_{CC}$ |

Note: X means Don't Care

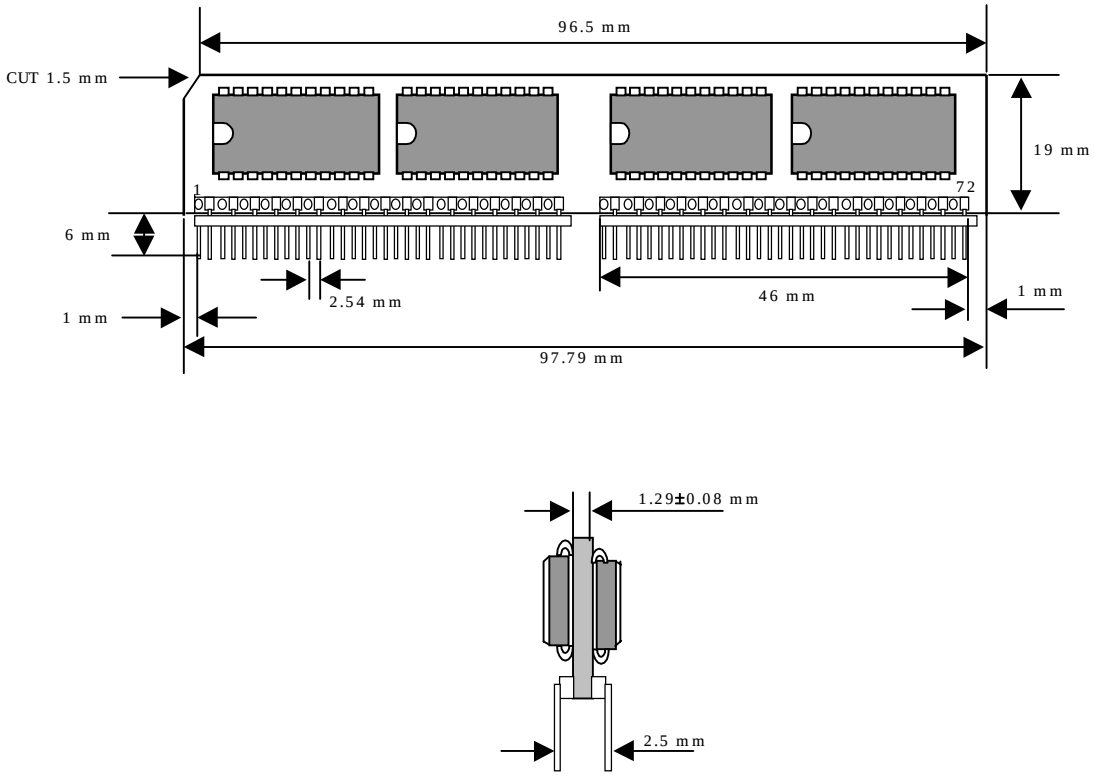
# PACKAGING DIMMENSIONS

## SIMM Design

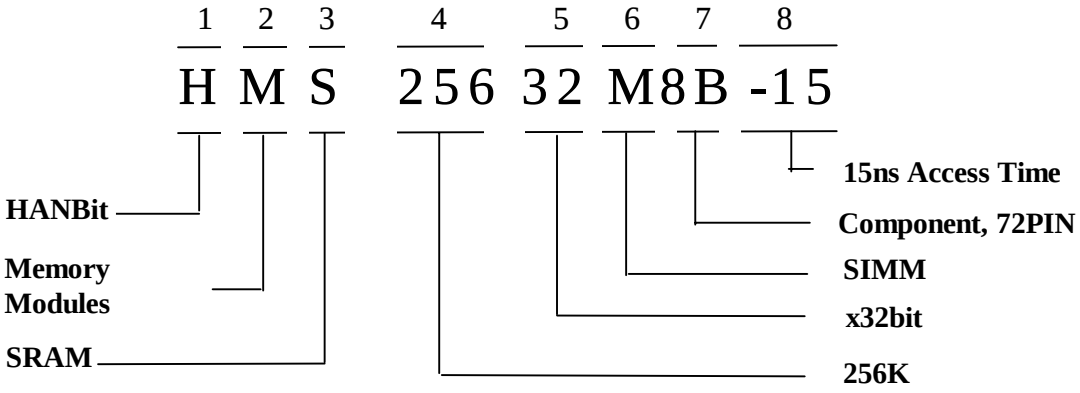



(Solder & Gold Plating Lead)

## ZIP Design



## ORDERING INFORMATION




**1. - Product Line Identifier**
**HANBit ---------- H**
**2. - Memory Modules**
**3. - SRAM**
**4. - Depth : 256K**
**5. - Width : x 32bit**
**6. - Package Code**
**SIMM ---------- M**
**ZIP ---------- Z**

**7. - Number of Memory Components, 72PIN**
**8. - Access time**
**10 ---------- 10ns**
**12 ---------- 12ns**
**15 ---------- 15ns**
**17 ---------- 17ns**
**20 ---------- 20ns**