

Primary Side Quasi-Resonant BJT Controller with CV/CC Operation

REV. 00

General Description

The LD7515L is an excellent primary side feedback BJT controller with CV/CC operation, integrated with several functions of protections. It minimizes the component counts and is available in a tiny SOT-26 package. Those make it an ideal design for low cost applications.

It provides functions of ultra-low startup current, green-mode power-saving operation and leading-edge blanking of the current sensing. Also, the LD7515L features Internal OTP (Over Temperature Protection) and OVP (Over Voltage Protection) to prevent the circuit from being damaged due to abnormal conditions.

In most cases, the power supply with primary-side feedback controller would accompany with some serious load regulation effect. To deal with this problem, the LD7515L consists of dedicated load regulation compensation circuit to enhance its performance.

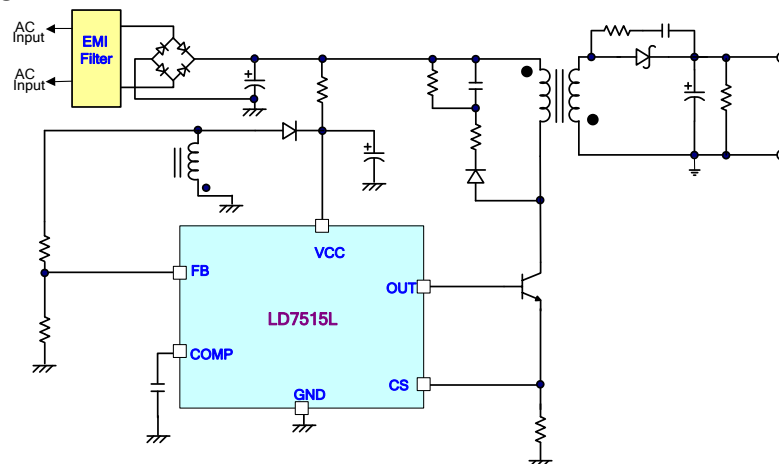
Features

- Primary-Side Feedback Control with Quasi-Resonant Operation
- Direct Drive of BJT Switch
- Constant Voltage within $\pm 5\%$
- Built-In Adjustable Load Regulation Compensation
- Constant Current Control
- Ultra-Low Startup Current ($< 1.9\mu\text{A}$)
- 0.5mA Low Operating Current at Light Load
- 60 kHz Maximum Switching Frequency.
- Current Mode Control
- Green Mode Control Improve Efficiency
- LEB (Leading-Edge Blanking) on CS Pin
- Built-in Soft Start
- VCC OVP (Over Voltage Protection)
- FB Pin Open/Short Protection
- Internal OTP (Over Temperature Protection)

Applications

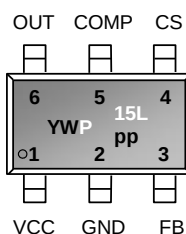
- Mobile Phone Adapter
- Lower Power AC/DC Adapter

Typical Application



Pin Configuration

SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005.....)
 WW, W : Week code
 PP : Production code
 P15L : LD7515L

Ordering Information

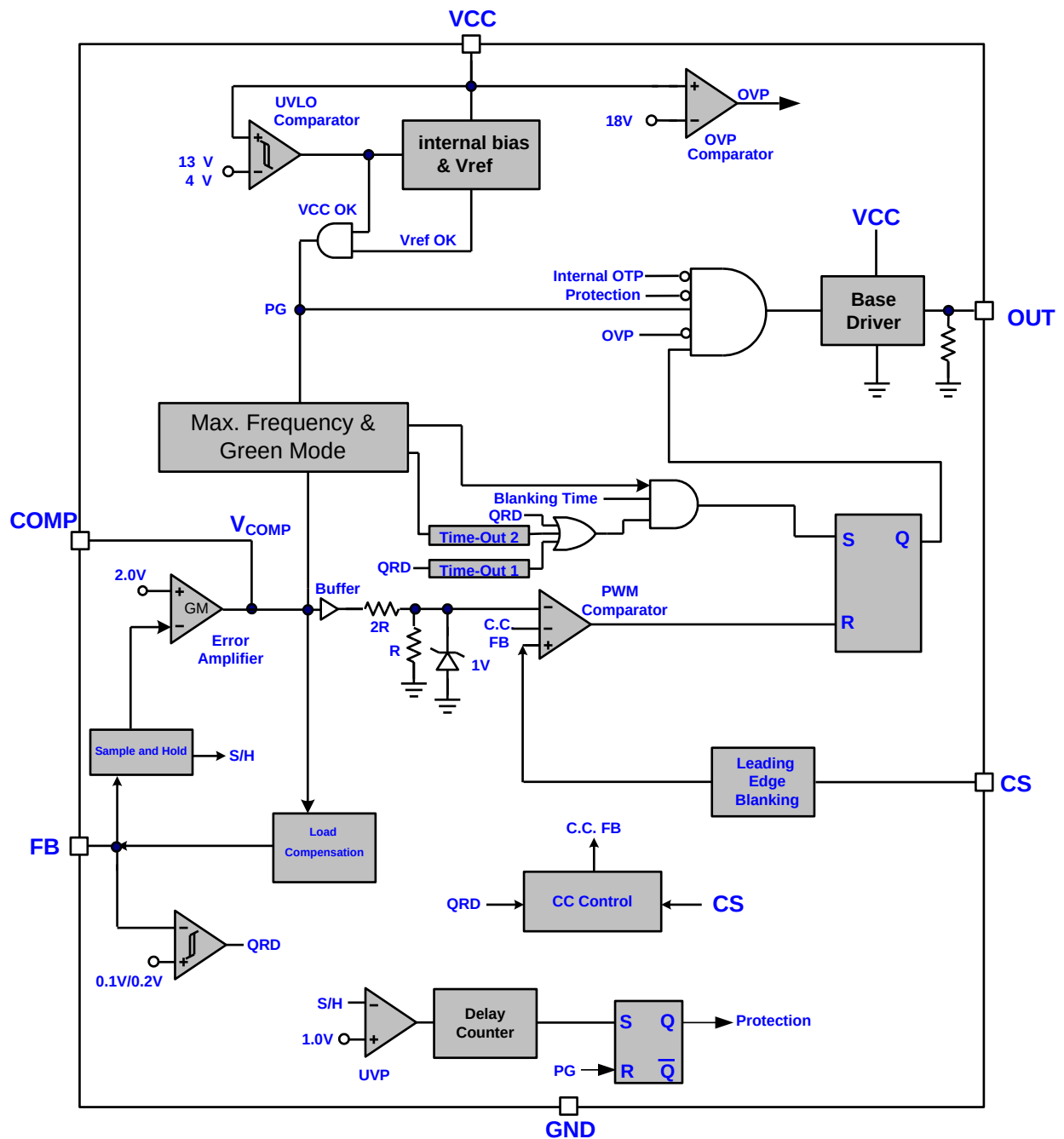
Part number	Package	Top Mark	Shipping
LD7515L GL	SOT-26	YWP/15L	3000 / tape & reel

The LD7515L is ROHS compliant/Green Packaged

Pin Descriptions

PIN	NAME	FUNCTION
1	VCC	Supply voltage pin.
2	GND	Ground.
3	FB	Auxiliary voltage sense and Quasi Resonant detection.
4	CS	Current sense pin, connect to sense the Switch current.
5	COMP	Output of the error amplifier for voltage compensation.
6	OUT	Base drive output to drive the external BJT Switch.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC,	20V
OUT,	-0.3V ~3.3V
COMP, FB, CS,	-0.3V ~3.3V
FB(AC current $\leq 3\text{mA}$),	-0.7V ~ 3.3V
Maximum Junction Temperature,	150°C
Storage Temperature Range,	-65°C to 150°C
Package Thermal Resistance (SOT-26, θ_{JA}),	200°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C),	200mW
Lead temperature (Soldering, 10sec),	260°C
ESD Voltage Protection, Human Body Model,	2.5 KV
ESD Voltage Protection, Machine Model,	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	110	°C
Supply VCC Voltage	5.5	16	V
VCC Capacitor	2.2	10	μF
Start-up resistor Value (AC Side, Half Wave)	1M	6.6M	Ω
Comp Pin Capacitor	470	4700	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1 μF ~0.47 μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=12.0V)

PARAMETER	CONDITIONS	SYM.	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)						
Startup Current	V _{CC} =UVLO-ON-0.05V	I _{CC_ST}		1.0	1.9	μA
Operating Current	V _{COMP} =0V, OUT=open, FB=2V	I _{CC_OP2}		0.5		mA
	OVP/FB UVP tripped, FB=0V	I _{CC_OPA}	0.18	0.25	0.32	mA
UVLO (off)		V _{CC_OFF}	3.4	4.0	4.6	V
UVLO (on)		V _{CC_ON}	12	13	14	V
Vcc OVP Level		V _{CC_OVP}	17	18	19	V
Error Amplifier (COMP pin)						
Reference Voltage, V _{REF}		V _{REF}	1.97	2.00	2.03	V
Output Sink Current	V _{FB} = V _{REF} +0.05, V _{COMP} =2V*	I _{COMP_SINK1}		-4		μA
Output Source Current	V _{FB} = V _{REF} -0.05V, V _{COMP} =2V*	I _{COMP_SOURCE1}		4		μA
Output Upper Clamp Voltage	V _{FB} =1.0V *	V _{COMP_CLAMP}		3		V
Load Compensation Current	V _{COMP} =3V	I _{LOAD COMP}	17	20	23	μA
Current Sensing (CS Pin)						
Maximum Input Voltage		V _{CS_MAX}	0.93	1	1.07	V
Minimum V _{CS-OFF}	V _{COMP} < 0.45V*	V _{CS_MIN}	150	175	195	mV
Leading Edge Blanking Time	*	T _{LEB}	430	600	770	ns
Oscillator for Switching Frequency						
Maximum Frequency		F _{SW_MAX}	54.5	60	65.5	kHz
Green Mode Frequency	*	F _{SW_GREEN}		25		kHz
Minimum Frequency		F _{SW_MIN}	0.6	0.8	1.0	kHz
Maximum On Time		T _{ON_MAX}	11	16	21	μs
Output Drive (OUT Pin)						
Max. Output Base Current	V _{CS} =1V	I _{B_MAX}	54	62	69	mA
FB Under Voltage Protection (UVP, FB Pin)						
Under Voltage Level		V _{FB_UVP}	0.9	1.0	1.1	V
UVP Delay Time	At start-up*	T _{D_FBUVP_SS}		20		ms
On Chip OTP (Over Temperature)						
OTP Level	**	T _{INOTP}	115	130	145	°C
OTP Hysteresis	*	T _{INOTP_HYS}		30		°C

*: Guaranteed by design.

** : For reference only, parameter verified in design phase.

Typical Performance Characteristics

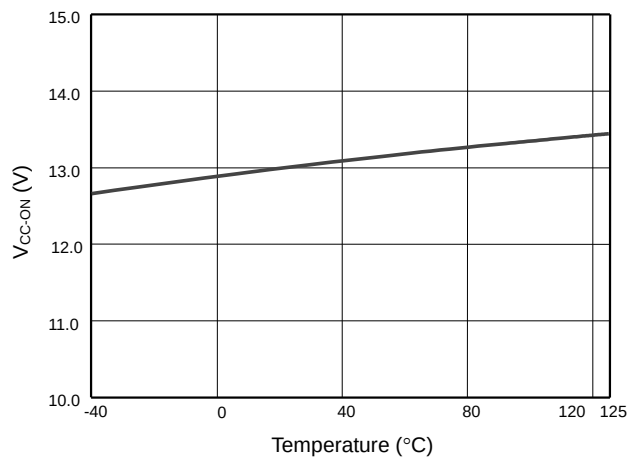


Fig. 1 UVLO (on) vs. Temperature

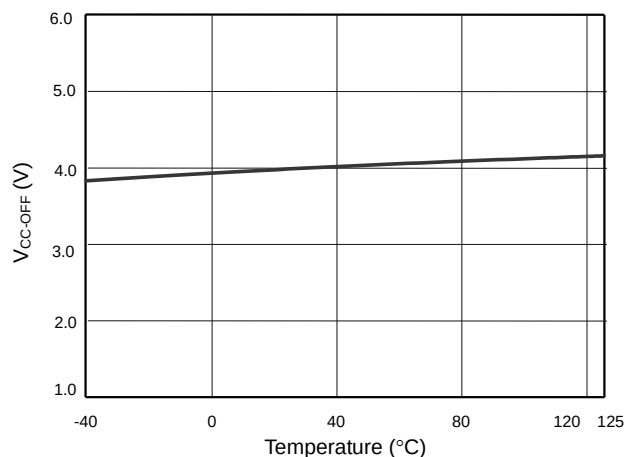


Fig. 2 UVLO (off) vs. Temperature

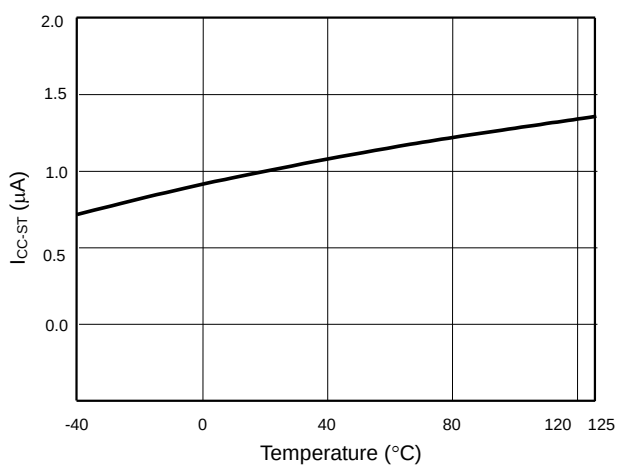


Fig. 3 Startup Current vs. Temperature

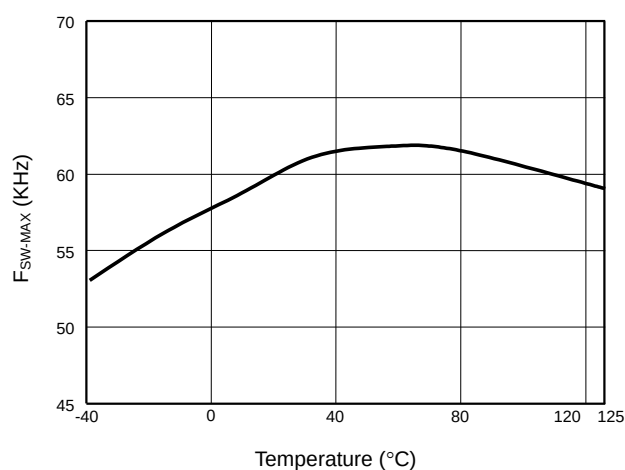


Fig. 4 Max Frequency vs. Temperature

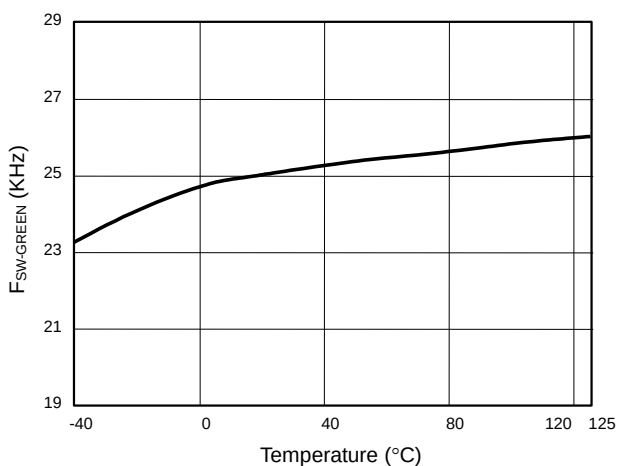


Fig. 5 Green Mode Frequency vs. Temperature

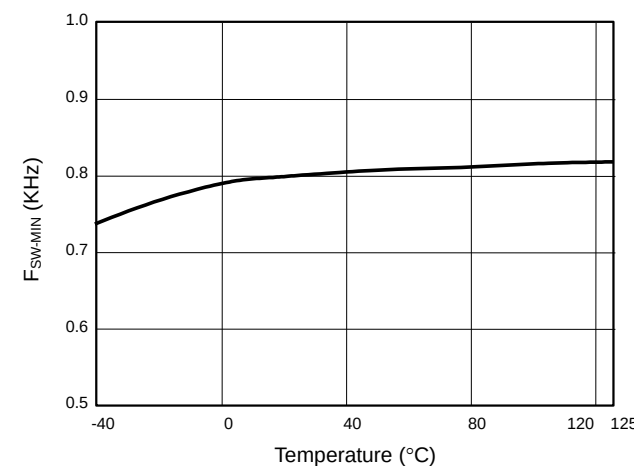


Fig. 6 Min Frequency vs. Temperature

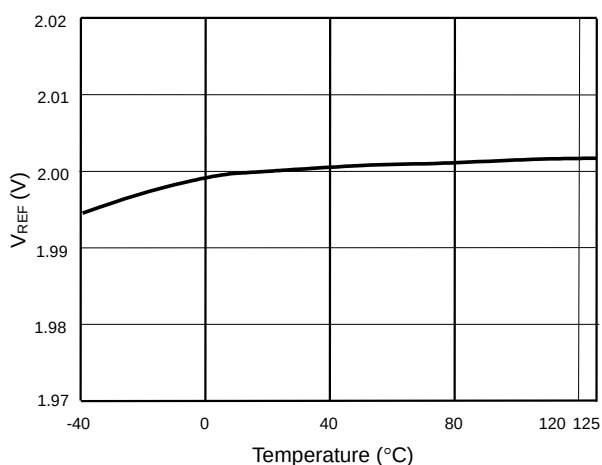


Fig. 7 Reference Voltage vs. Temperature

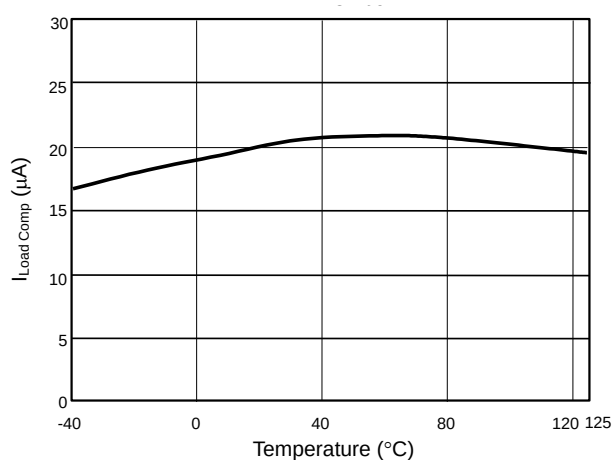


Fig. 8 Load Compensation vs. Temperature

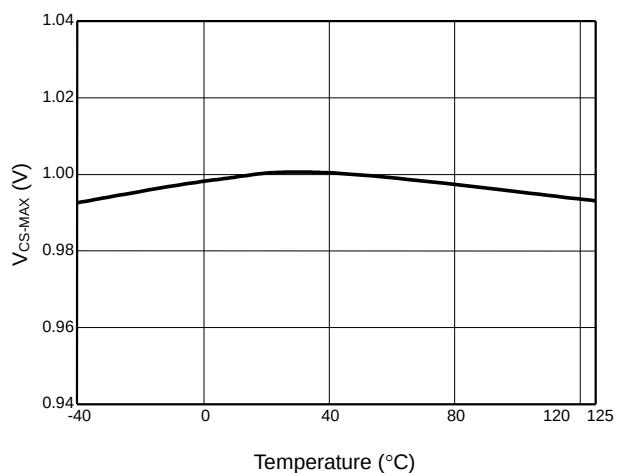


Fig. 9 V_{CS} (off) vs. Temperature

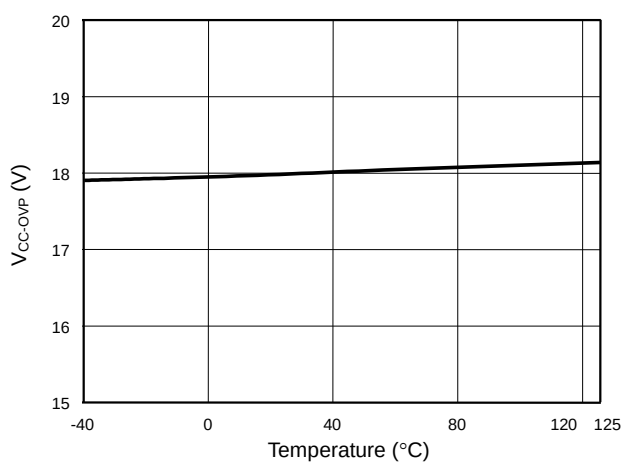


Fig. 10 V_{CC} OVP vs. Temperature

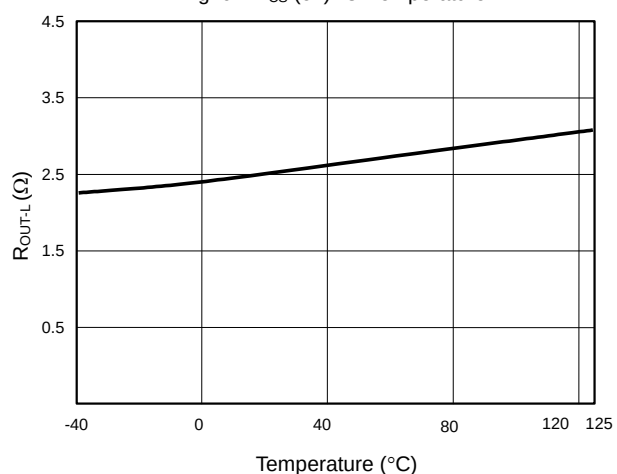


Fig. 11 Output Low ON-resistance vs. Temperature

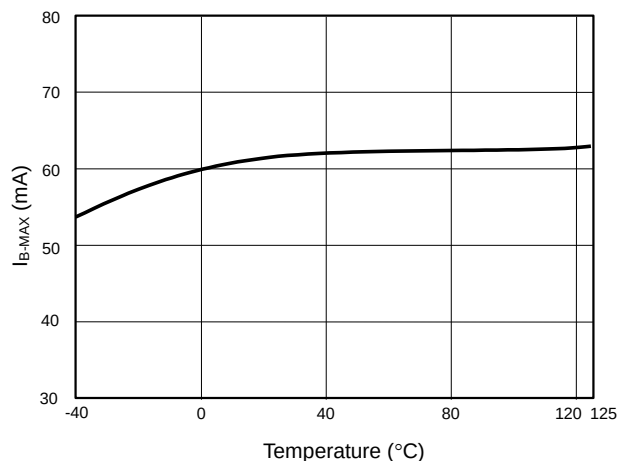


Fig. 12 Max. Output Base Current vs. Temperature

Application Information

Operation Overview

The LD7515L is an excellent primary side feedback controller with Quasi-Resonant operation to provide high efficiency. The LD7515L removes the need for secondary feedback circuits while achieving excellent line and load regulation. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. It integrates with more functions to reduce the external components counts and the size. Major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across VCC pin. It would assure the supply voltage enough to turn on the LD7515L and further to drive the power BJT. As shown in Fig. 13, a hysteresis is built in to prevent shutdown from voltage dip during startup.

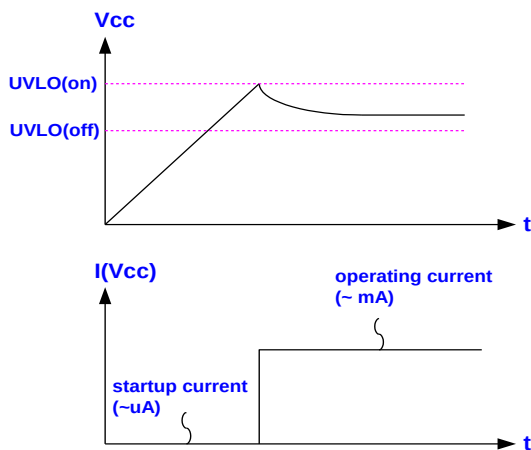


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate VCC of the LD7515L is shown in Fig. 14. At startup transient, the VCC is below the UVLO(on) threshold, so there's no pulse delivered out from LD7515L to drive the power BJT. Therefore, the current through R1 will be used to charge the capacitor C1. Until the VCC is fully charged to deliver the drive-out signal, the auxiliary winding of the transformer will provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and some unique circuit design, the LD7515L requires only 1.9 μ A max to start up. Higher resistance of R1 will spend much more time to start up. The user is recommended to select proper value of R1 and C1 to optimize the power consumption and startup time.

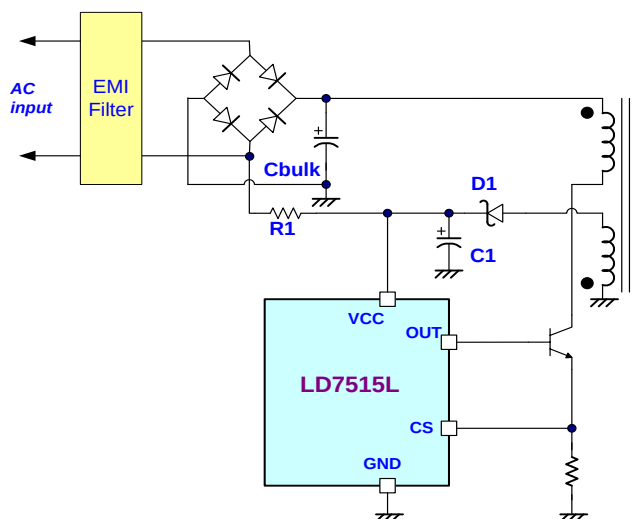


Fig. 14

Principle of CV Operation

In the DCM flyback converter, it can sense the output voltage from auxiliary winding. LD7515L samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig. 15. The voltage induced in the auxiliary winding is a reflection of the secondary winding voltage while the BJT is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the auxiliary voltage is sampled after the sample delay time which is defined as 30~50% of secondary current discharge time from previous cycle. And will be hold until the next sampling period. The sampled voltage is compared with an internal reference V_{REF} (2.0V) and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT} = 2.0V(1 + \frac{R_a}{R_b})(\frac{N_s}{N_a}) - V_F$$

Where V_F indicates the drop voltage of the output diode, R_a and R_b are top and bottom feedback resistor value, N_s and N_a are the turns of transformer secondary and auxiliary.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. To optimize the collector voltage clamp circuit will minimize the high frequency ringing and achieve the best regulation. Fig. 16 shows the desired collector voltage waveform in compare to those with large undershoot due to leakage inductance induced ring (Fig. 17). The ringing may make the sample error and cause poor performance for output voltage regulation. A proper selection for resistor R_S , in series with the clamp diode, may reduce any large undershoot, as shown in Fig. 18.

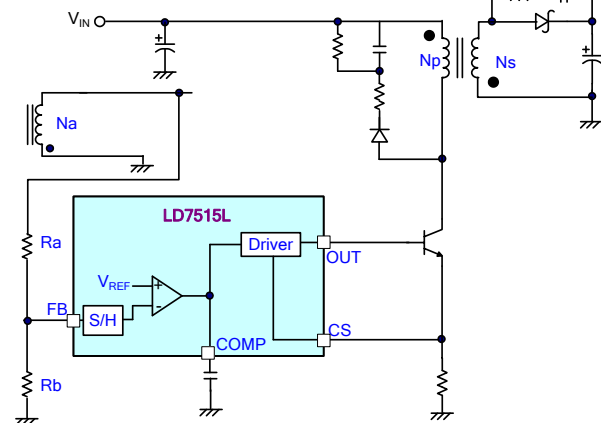


Fig. 15

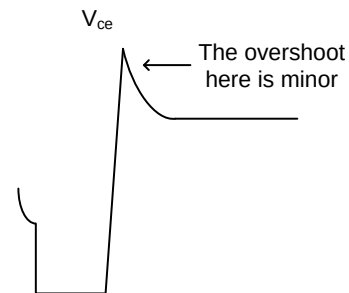


Fig.16

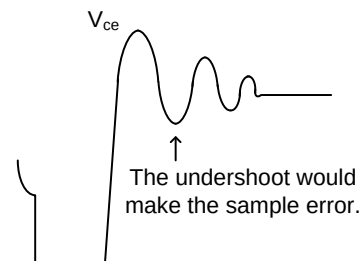


Fig.17

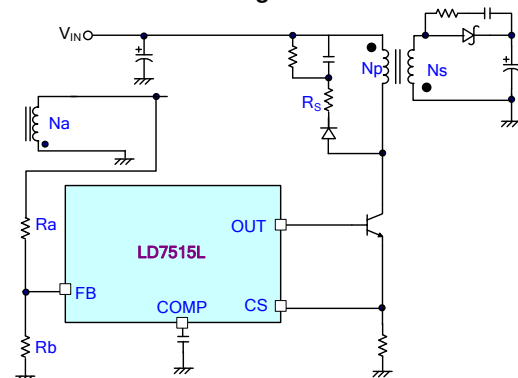


Fig.18

Load Regulation Compensation

LD7515L is implemented with load regulation compensation to compensate the cable voltage drop and to achieve a better voltage regulation. The offset voltage across FB is produced by the internal sink current source during the sampling period. The internal sink current source is proportional to the value of V_{COMP} to compensate the cable loss as shown in Fig. 19. So, the offset voltage will decrease as the V_{COMP} decreases from full-load to no-load. It is programmable by adjusting the resistance of the voltage divider to compensate the drop for cable lines used in various conditions. The equation of internal sink current is shown as:

$$I_{FB} = (V_{COMP} - 0.45) \times 7.85 (\mu A)$$

The compensation current versus V_{COMP} is shown as:

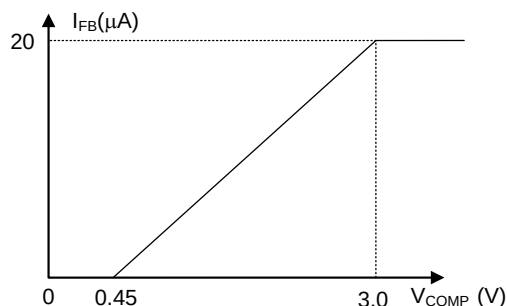


Fig. 19

Quasi-Resonant Mode Detection

The LD7515L employs quasi-resonant (QR) switching scheme to switch in valley-mode either in CV or CC operation. This will greatly reduce the switching loss and the ratio dv/dt in the entire operating range for the power supply. Fig. 20 shows the typical QR detection block. The QR detection block will detect auxiliary winding signal to drive BJT as FB pin voltage drops to 0.1V. The QR comparator will not activate if FB pin voltage remains above 0.2V.

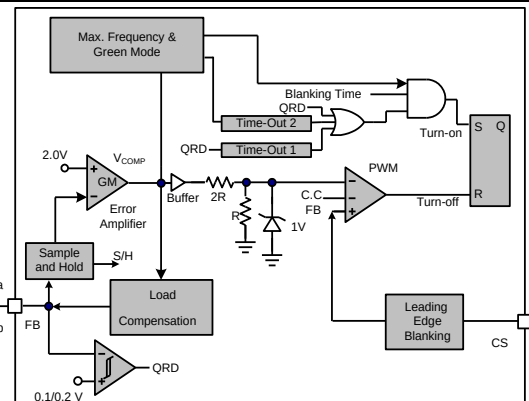


Fig. 20

Multi-Mode Operation

The LD7515L is a QR controller operating in multi-modes. The controller changes operation modes according to line voltage and load conditions. At heavy-load ($V_{COMP} > 1.8V$, Fig. 21), there might be two situations to meet. If the system AC input is in low line, the LD7515L will turn on in first valley. If in high line, the switching frequency will increase till over the limit of 60 kHz and skip the first valley to turn on in 2nd, 3rd....valley. The switching frequency would vary depending on the line voltage and the load conditions when the system is operated in QR mode.

At medium or light load conditions ($0.7V < V_{COMP} < 1.4V$), the frequency clamp is reduced to 25 kHz maximum. However, the characteristic in valley switching behaves well without problem in this condition. The LD7515L will turn on in 4th, 5th.... valley. That is, when the load decreases, the system will automatically skip some valleys and the switching frequency is therefore reduced. A smooth frequency fold-back and high power efficiency are then achieved.

At zero load or very light load conditions ($V_{COMP} < 0.3V$), the system operates in minimum frequency for power saving. The system modulates the frequency according to the load and V_{COMP} conditions.

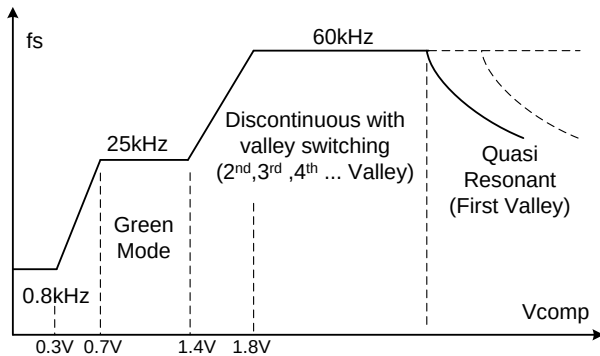


Fig. 21

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 22, the LD7515L detects the primary BJT current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 1V. From above, the BJT peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{1V}{R_{CS}}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the turn-on current spike.

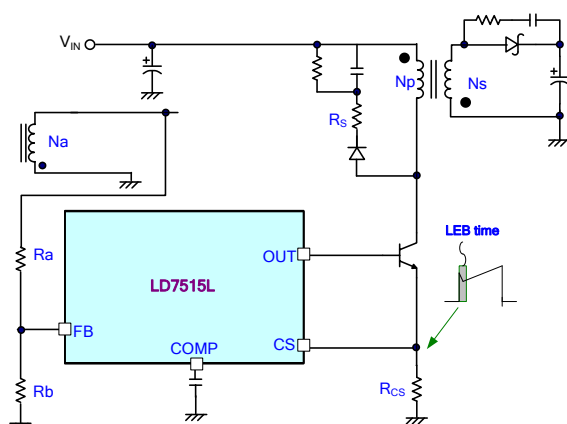


Fig. 22

Principle of C.C. Operation

The primary side control scheme is applied to eliminate secondary feedback circuit or opto-coupler, which will reduce the system cost. The switching waveforms are shown in Fig. 23. The output current "Io" can be expressed as:

$$\begin{aligned} I_o &= \frac{1}{2} \frac{i_{S,PK} \times T_{DIS}}{T_s} \\ &= \frac{1}{2} \frac{N_p}{N_s} \times i_{P,PK} \times \frac{T_{DIS}}{T_s} \\ &= \frac{1}{2} \frac{N_p}{N_s} \times \frac{V_{CS}}{R_{CS}} \times \frac{T_{DIS}}{T_s} \end{aligned}$$

The primary peak current ($i_{P,PK}$), inductor current discharge time (T_{DIS}) and switching period (T_s) can be detected by the IC. The ratio of $V_{CS} \cdot T_{DIS} / T_s$ will be modulated as a constant ($V_{CS} \cdot T_{DIS} / T_s = 1/3$). So that I_o can be obtained as

$$\begin{aligned} I_o &= \frac{1}{2} \frac{N_p}{N_s} \times \frac{V_{CS}}{R_s} \times \frac{T_{DIS}}{T_s} \\ &= \frac{1}{2} \frac{N_p}{N_s} \times \frac{1}{R_s} \times \frac{1}{3} \end{aligned}$$

However this is an approximate equation. The user may fine-tune it according to the experiment result.

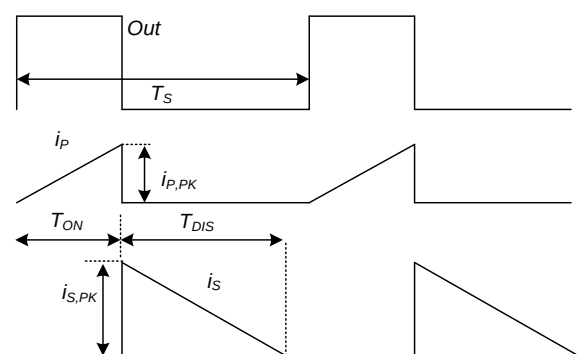


Fig. 23

OVP (Over Voltage Protection) on Vcc – Auto Recovery

LD7515L is implemented with OVP function through Vcc. As the Vcc voltage rises over the OVP threshold voltage, the output drive circuit will be shut off simultaneously thus to stop the switching of the power BJT until the next UVLO(on) arrives. The Vcc OVP function of LD7515L is an auto-recovery type protection. The Fig. 24 shows its operation. That is, if the OVP condition is removed, it will resume to normal output voltage and Vcc level in normal condition.

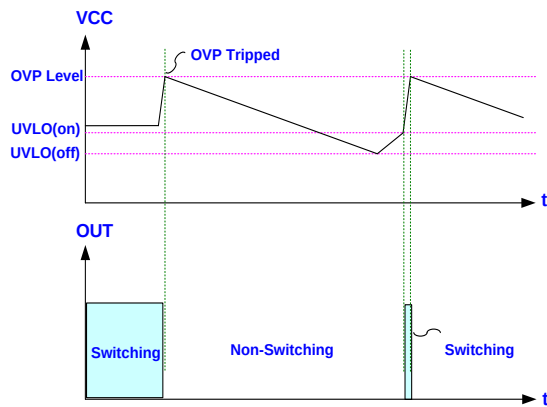


Fig. 24

FB Under Voltage Protection (FB UVP) & FB Short Circuit Protection – Auto Recovery

LD7515L is implemented with an UVP function over FB pin. If the FB voltage falls below 1.0V over the delay time, the protection will be activated to stop the switching of the power BJT until the next UVLO(on) arrives. The FB UVP function in LD7515L is an auto-recovery type protection. The Fig. 25 shows its operation. The FB UVP is disabled during the soft start period. During the soft start period, the FB UVP is disabled. To avoid output over voltage in soft start period. The Fig. 26 shows the operation. While FB is short to GND, FB pin keeps in zero voltage level. If FB cannot detect any voltage signal over 0.2V in the beginning of soft start period, then the soft start will turn to

generate a driving signal every 4ms until FB UVP delay to shut down IC and auto recovery.

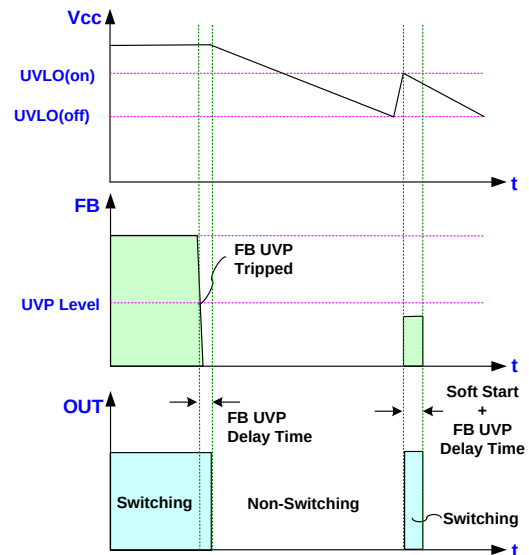


Fig. 25

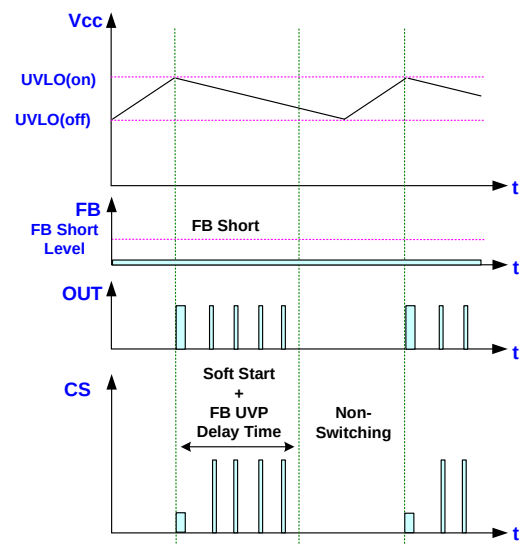
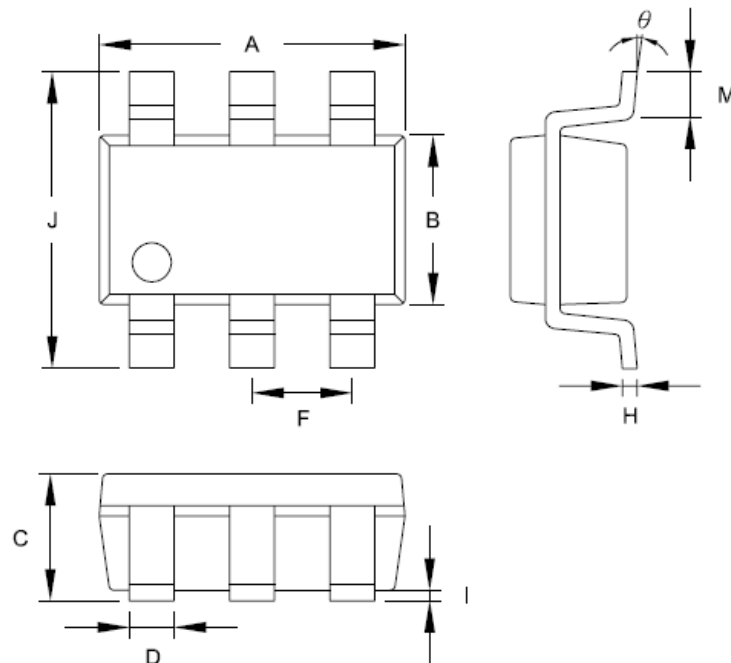


Fig. 26

Package Information

SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-----	1.450	-----	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	08/05/2015	Original Specification.