TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

65,536-WORD BY 16-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V1664J is a 1,048,576-bit high-speed static random access memory (SRAM) organized as 65,536 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed and low-voltage operation, it operates from a single 3.3 V power supply. Chip enable ($\overline{CE}$) can be used to place the device in a low-power mode, and output enable ($\overline{OE}$) provides fast memory access. Data byte control signals (LB, UB) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55V1664J is available in plastic 44-pin SOJ packages (400 mil width) for high density surface assembly.

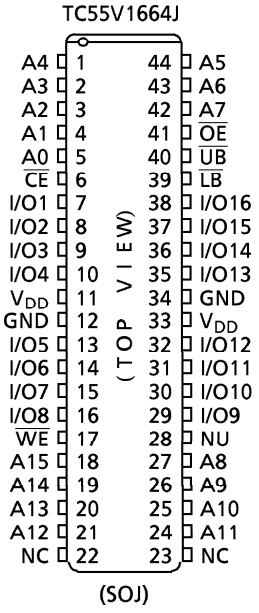
FEATURES

- Fast access time (the following are maximum values)
  TC55V1664J-12: 12 ns
  TC55V1664J-15: 15 ns
- Low-power dissipation
  (the following are maximum values)

Cycle Time	12	15	20	30	ns
Operation (max)	190	170	150	130	mA

  Standby: 2 mA (all devices)
- Single power supply voltage of 3.3 ± 0.3 V.
  TC55V1664J-12: 3.3 V ± 5%
  TC55V1664J-15: 3.3 ± 0.3 V
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using $\overline{OE}$
- Data byte control using $\overline{LB}$ (IO1 to IO8) and $\overline{UB}$ (IO9 to IO16)
- Packages:
  SOJ44-P-400-1.27 (Weight: 1.64 g typ)

PIN ASSIGNMENT



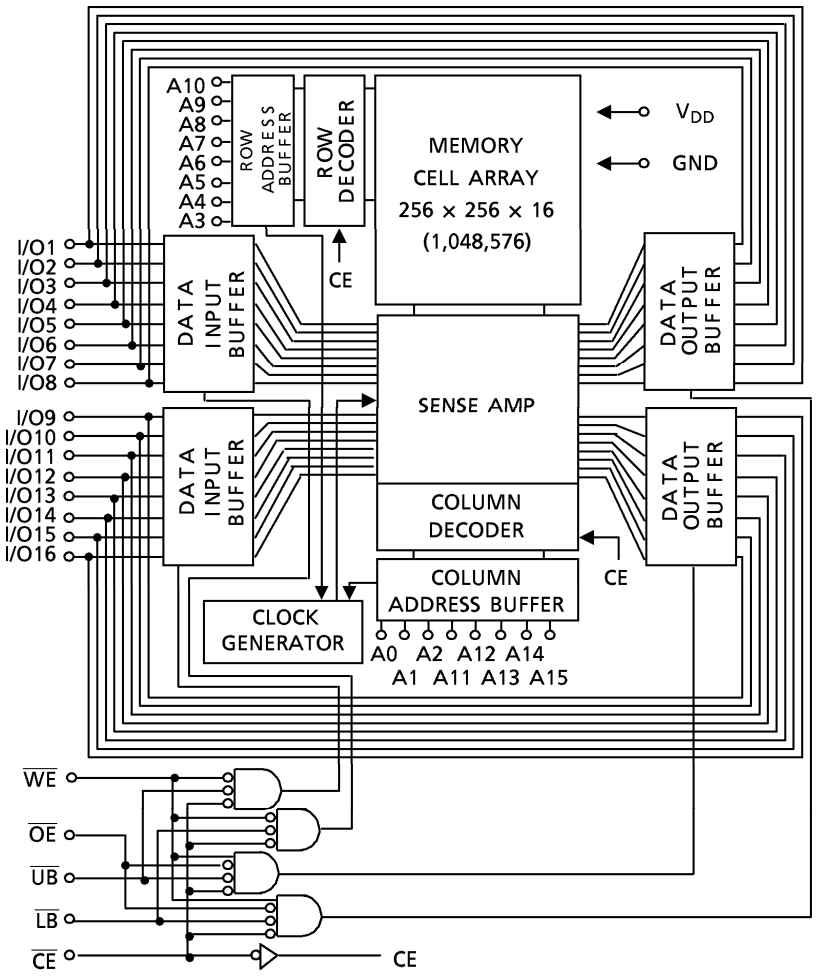
PIN NAMES

A0 to A15	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power (+ 3.3 V)
GND	Ground
NC	No Connection
NU	Not Used (Input)

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 0.5 to 4.6	V
V_{IN}	Input Terminal Voltage	− 0.5 * to 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	− 0.5 * to V_{DD} + 0.5**	V
P_D	Power Dissipation	1.2	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	− 65 to 150	°C
T_{opr}	Operating Temperature	− 10 to 85	°C

*: − 1.5 V with a pulse width of 20% · t_{RC} min (4 ns max)
**: V_{DD} + 1.5 V with a pulse width of 20% · t_{RC} min (4 ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	– 12	3.135	3.3	3.465	V
		– 15	3.0	3.3	3.6	
V_{IH}	Input High Voltage		2.0	–	V_{DD} + 0.3**	V
V_{IL}	Input Low Voltage		– 0.3 *	–	0.8	V

*: – 1.0 V with a pulse width of 20% · t_{RC} min (4 ns max)
**: V_{DD} + 1.0 V with a pulse width of 20% · t_{RC} min (4 ns max)

DC CHARACTERISTICS (Ta = 0° to 70°C, -12: V_{DD} = 3.3 V ± 5%, -15: V_{DD} = 3.3 ± 0.3 V)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current (Except NU Pin)	V_{IN} = 0 V to V_{DD}		– 1	–	1	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 V to V_{DD}		– 1	–	1	μA
$I_{I(NU)}$	Input Current (NU Pin)	V_{IN} = 0 to 0.8 V		– 1	–	20	μA
		V_{IN} = 0 to 0.2 V		– 1	–	1	
V_{OH}	Output High Voltage	I_{OH} = – 2 mA		2.4	–	–	V
		I_{OH} = – 100 μA		V_{DD} – 0.2	–	–	
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		–	–	0.4	
		I_{OL} = 100 μA		–	–	0.2	
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, Iout = 0 mA Other Inputs = V_{IH} or V_{IL}	tcycle = 12 ns	–	–	190	mA
			tcycle = 15 ns	–	–	170	
			tcycle = 20 ns	–	–	150	
			tcycle = 30 ns	–	–	130	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}		–	–	20	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} – 0.2 V Other Inputs = V_{DD} – 0.2 V/0.2 V		–	–	2	

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	×	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Outputs Disable	L	H	H	×	×	High Impedance	High Impedance	I_{DDO}
	L	×	×	H	H			
Standby	H	×	×	×	×	High Impedance	High Impedance	I_{DDS}

×: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V. You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS

(Ta = 0° to 70°C (Note 1), -12: V_{DD} = 3.3 V ± 5%, -15: V_{DD} = 3.3V ± 0.3 V)

READ CYCLE

SYMBOL	PARAMETER	TC55V1664J-12		TC55V1664J-15		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	12	–	15	–	ns
t_{ACC}	Address Access Time	–	12	–	15	
t_{CO}	Chip Enable Access Time	–	12	–	15	
t_{OE}	Output Enable Access Time	–	6	–	8	
t_{BA}	Upper Byte, Lower Byte Access Time	–	6	–	8	
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	
t_{COE}	Output Enable Time from Chip Enable	3	–	3	–	
t_{OEE}	Output Enable Time from Output Enable	1	–	1	–	
t_{BE}	Output Enable Time from Upper Byte, Lower Byte	1	–	1	–	
t_{COD}	Output Disable Time from Chip Enable	–	7	–	8	
t_{ODO}	Output Disable Time from Output Enable	–	7	–	8	
t_{BD}	Output Disable Time from Upper Byte, Lower Byte	–	7	–	8	

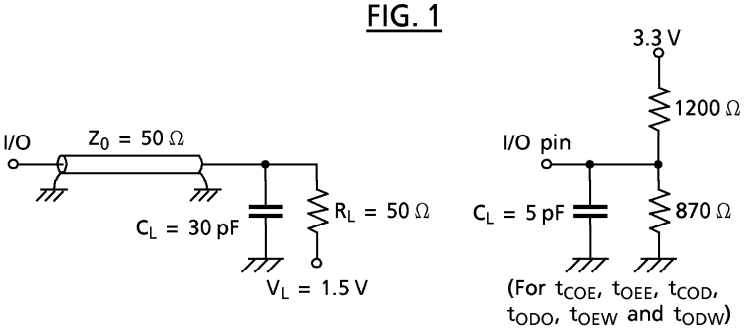
WRITE CYCLE

SYMBOL	PARAMETER	TC55V1664J-12		TC55V1664J-15		UNIT
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	12	–	15	–	ns
t_{WP}	Write Pulse Width	8	–	9	–	
t_{CW}	Chip Enable to End of Write	10	–	12	–	
t_{BW}	Upper Byte, Lower Byte Enable to End of Write	10	–	11	–	
t_{AW}	Address Valid to End of Write	10	–	11	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	7	–	8	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from Write Enable	1	–	1	–	
t_{ODW}	Output Disable Time from Write Enable	–	7	–	8	

AC TEST CONDITIONS

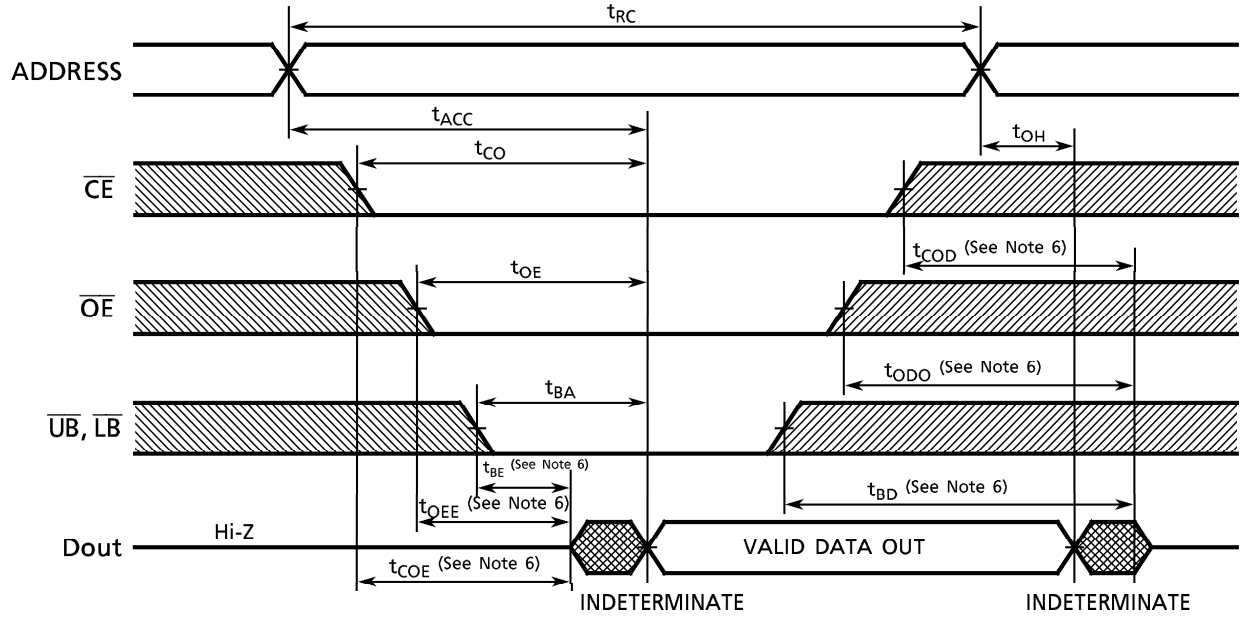
Input Pulse Level	3.0 V, 0.0 V
Input Pulse Rise and Fall Time	3 ns
Input Timing Measurement Reference Level	1.5 V
Output Timing Measurement Reference Level	1.5 V
Output Load	Fig. 1

FIG. 1

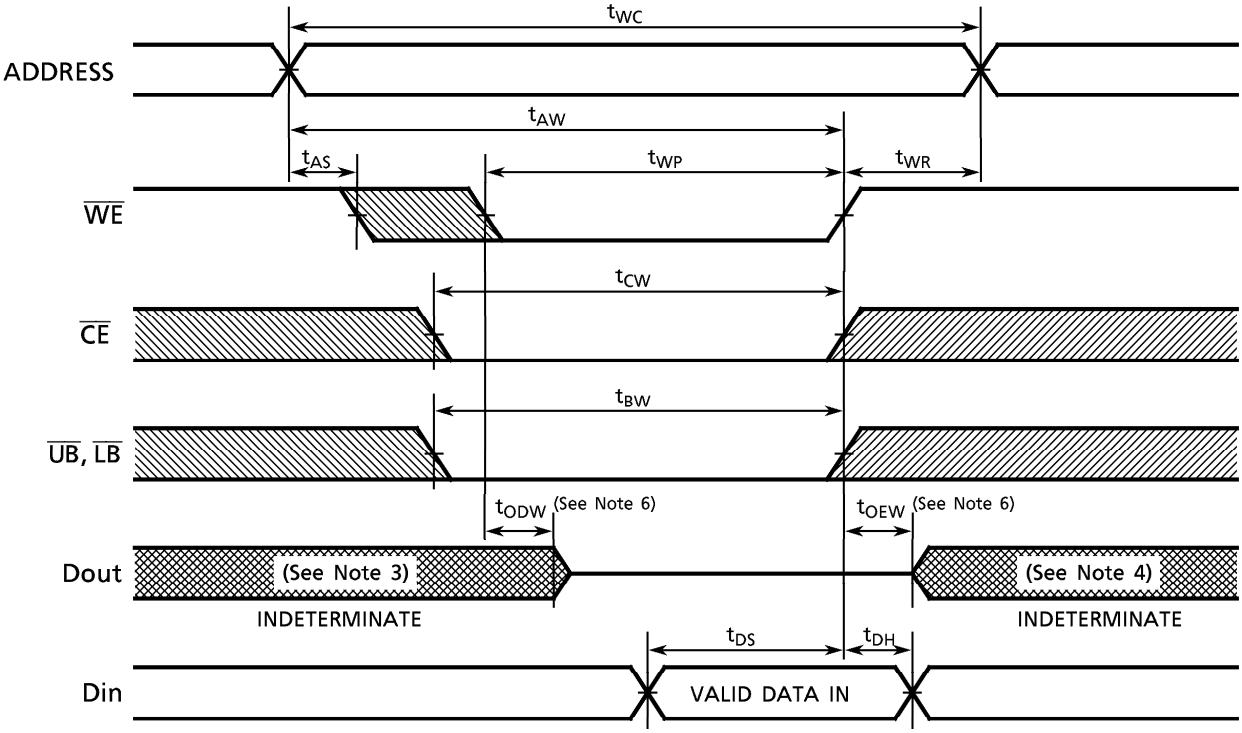


TIMING DIAGRAMS

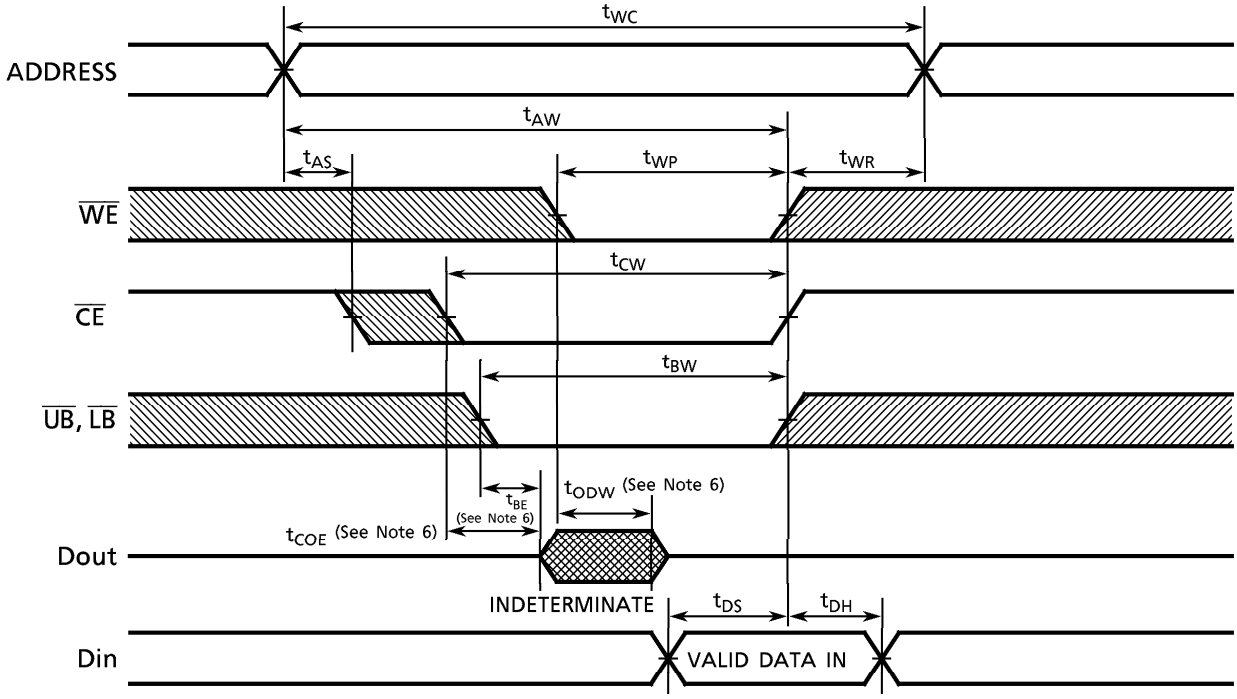
READ CYCLE (See Note 2)



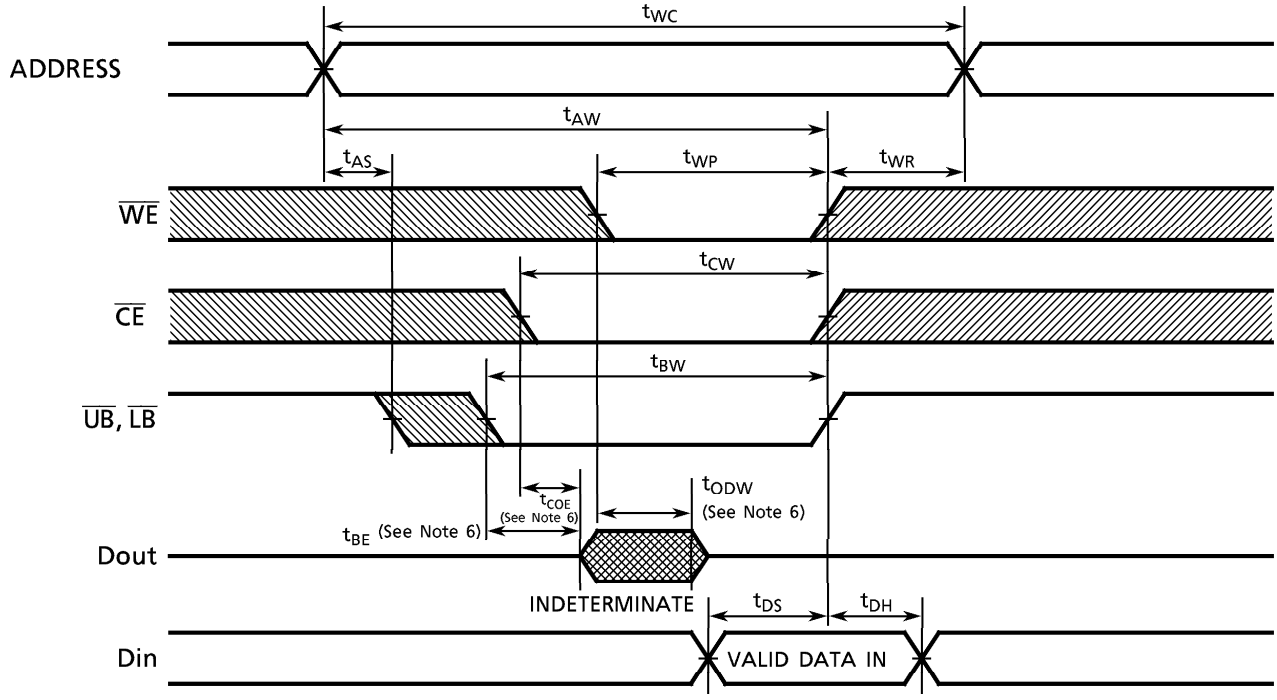
WRITE CYCLE 1 (WE CONTROLLED) (See Note 5)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 5)



WRITE CYCLE 3 ($\overline{UB}$, $\overline{LB}$ CONTROLLED) (See Note 5)



Note: (1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) $\overline{WE}$ remains High for the Read Cycle.

(3) If $\overline{CE}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

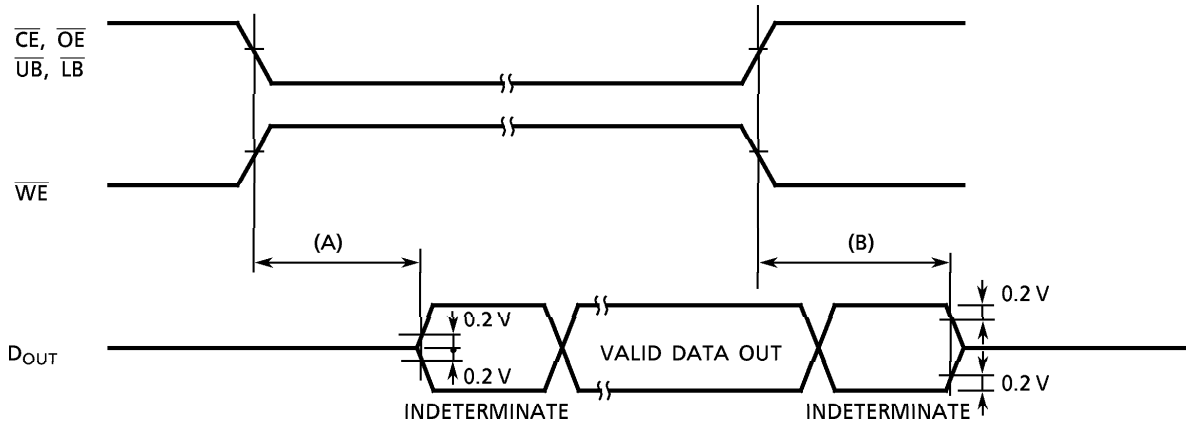
(4) If $\overline{CE}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

(5) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1

(A) t_{COE}, t_{OEE}, t_{BE}, t_{OEW} ····· Output Enable Time

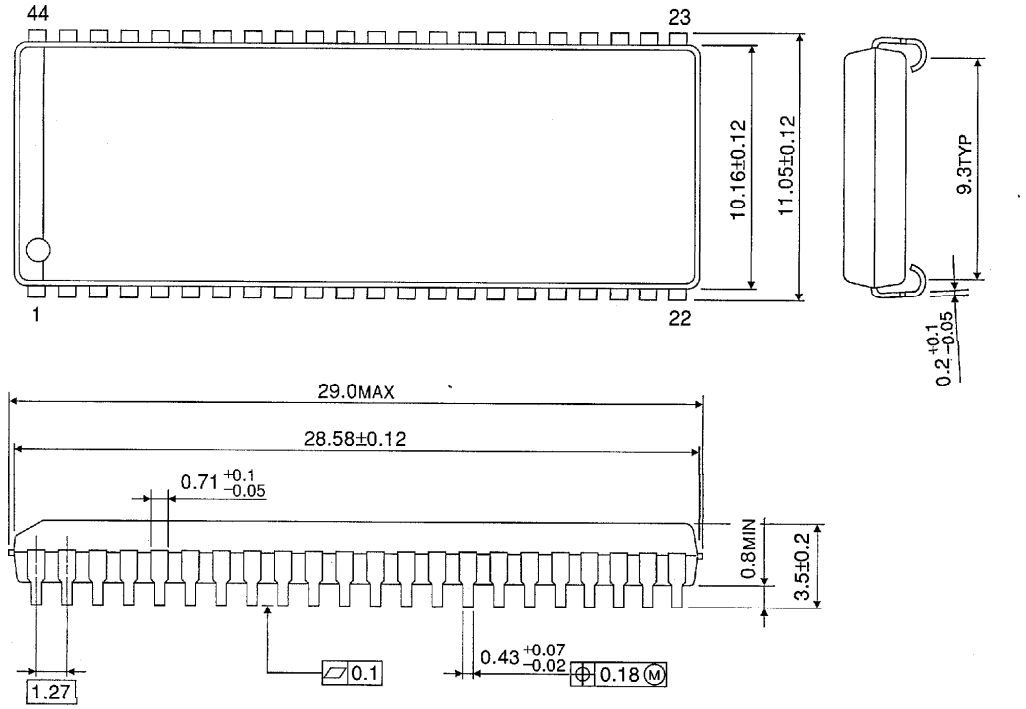
(B) t_{COD}, t_{ODO}, t_{BD}, t_{ODW} ····· Output Disable Time



PACKAGE DIMENSIONS

Plastic SOJ (SOJ44-P-400-1.27)

Units in mm



Weight: 1.64 g (typ)