CUSTOMER PRODUCT SPECIFICATION

Z86C27-ROM
Z86C97-ROMLESS
CMOS Z8® 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C27 and Z86C97 Digital Television Controller (DTC) introduce a new level of sophistication to single-chip architecture. The Z86C27/C97 are members of the Z8 single-chip microcontroller family with 8 Kbytes of ROM (Z86C27), ROMless (Z86C97) and 236 bytes of RAM. Both devices are housed in a 64-pin DIP package, and are CMOS compatible. Having the ROM/ROMless selectivity, the DTC offers both external memory and pre-programmed ROM which enables the Z8 microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program). The Z86C97 ROMless offers the use of external memory rather than a preprogrammed ROM. This enables the Z8 microcontroller to be used in prototyping, low volume applications or where code flexibility is required. Zilog's DTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86C27/C97 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The devices have an 8-bit internal data path controlled by a Z8 microcontroller, and On Screen Display (OSD) logic circuits/Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and Port 3), Interrupt control logic (1 software, 2 external and 3 internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support 8 rows by 20 columns for 128 kinds of characters. The character color is specified by row. One of the 8 rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5x7 dot pattern) or high resolution (11x15 dot pattern) characters. The Z86C97 currently supports high resolution characters only.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Seven 6-bit PWM ports are used for controlling audio signal level. Five 8-bit PWM ports are used to vary picture levels.

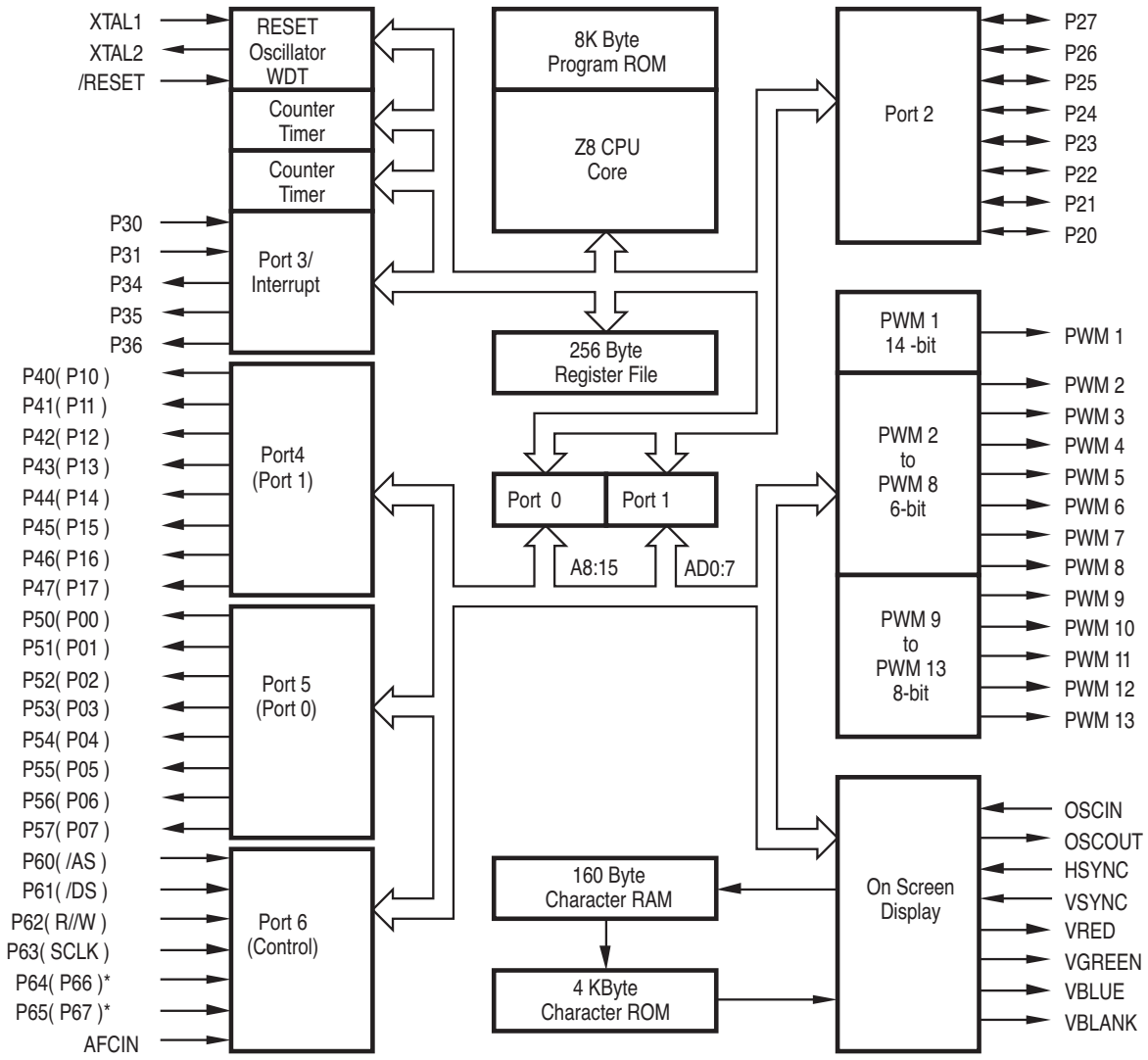
The DTC applications demand powerful I/O capabilities. The Z86C27/C97 fulfills this with 35 I/O pins dedicated to input and output. These lines are grouped into five ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Register File and Data Memory. The Register File is composed of 236 bytes of general purpose register, two I/O Port registers and 15 control and status registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the DTC's offer two on-chip counter/timers with a large number of user selectable modes (see block diagram).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

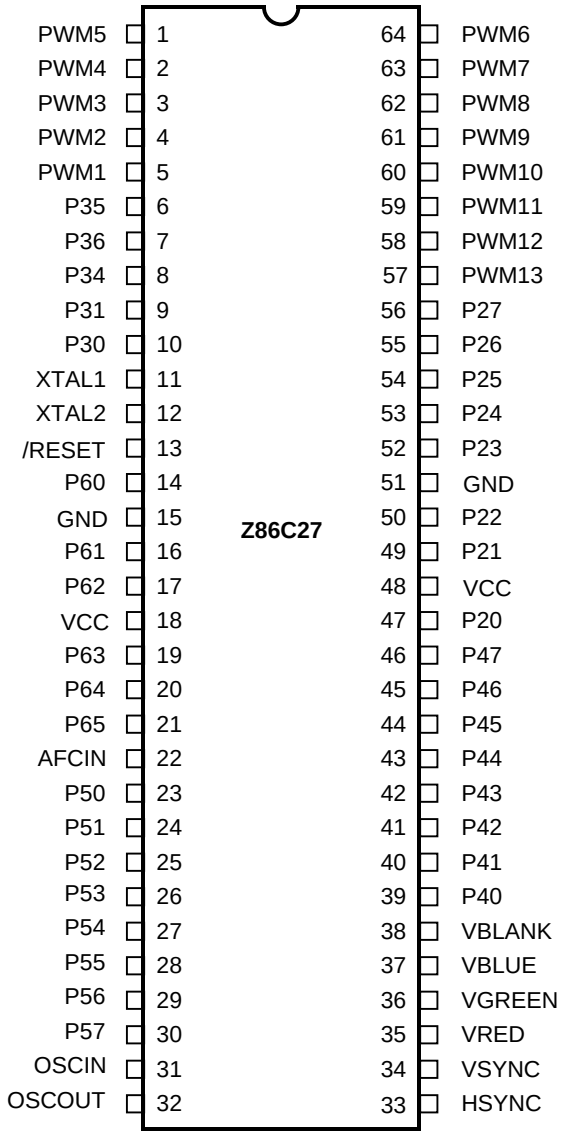
GENERAL DESCRIPTION (Continued)



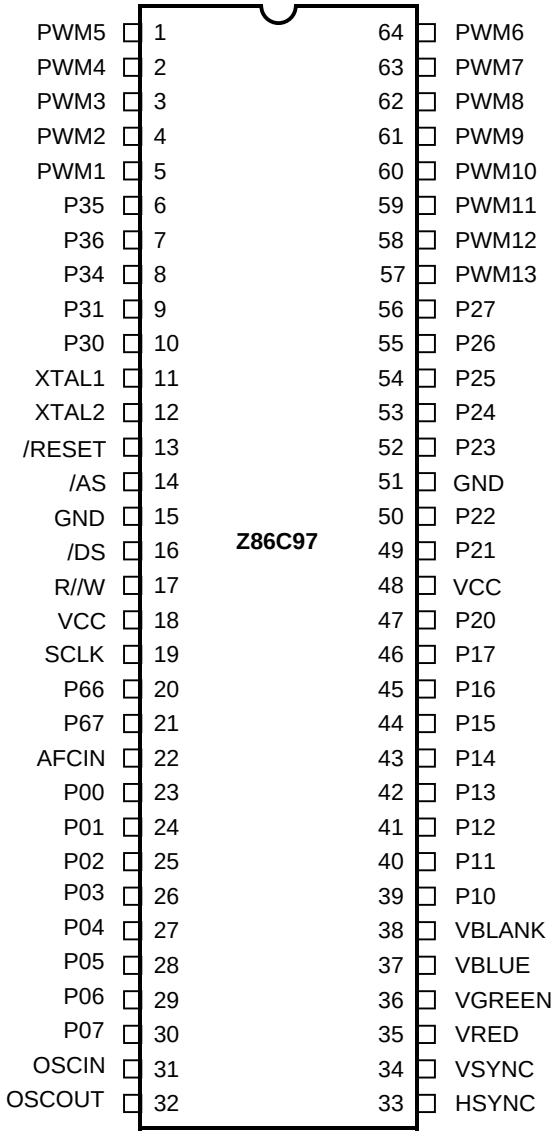
* ( ) Denotes Z86C97 signal differences.

Functional Block Diagram

PIN CONFIGURATION



Z86C27 Mask-ROM Plastic DIP



Z86C97 ROMless Plastic DIP

ABSOLUTE MAXIMUM RATINGS

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

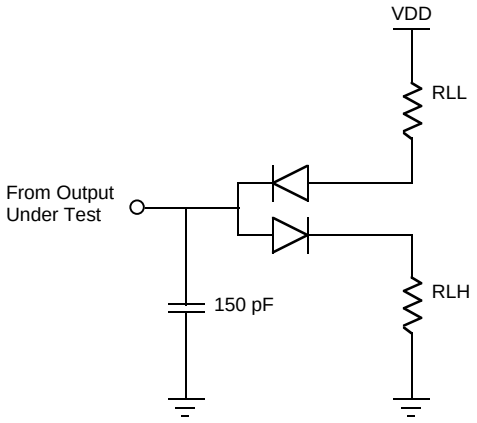
Symbol	Parameters	Min	Max	Units	Notes
V_{CC}	Power Supply Voltage †	–0.3	+7	V	
V_I	Input Voltage	–0.3	V_{CC} +0.3	V	
V_I	Input Voltage	–0.3	V_{CC} +0.3	V	[1]
V_O	Output Voltage	–0.3	V_{CC} +8.0	V	[2]
I_{OH}	Output Current High		–10	mA	1 pin
I_{OH}	Output Current High		–100	mA	all total
I_{OL}	Output Current Low		20	mA	1 pin
I_{OL}	Output Current Low		40	mA	[3] (1 pin)
I_{OL}	Output Current Low,all total		200	mA	
T_A	Operating Temperature	††			
T_{STG}	Storage Temperature	–65	+150	C	

Notes:
[1] Port 2 open-drain
[2] PWM open-drain outputs
[3] Port 5

† Voltage on all pins with respect to GND.
†† See Ordering Information

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Test Load Diagram).



Test Load Diagram

CAPACITANCE

T_A=25°C, V_{CC}=GND=0 V, Freq=1.0 MHz, unmeasured pins to GND.

Parameter	Max	Units
Input capacitance	10	pF
Output capacitance	20	pF
I/O capacitance	25	pF
AFC_{IN} input capacitance	10	pF

DC CHARACTERISTICS

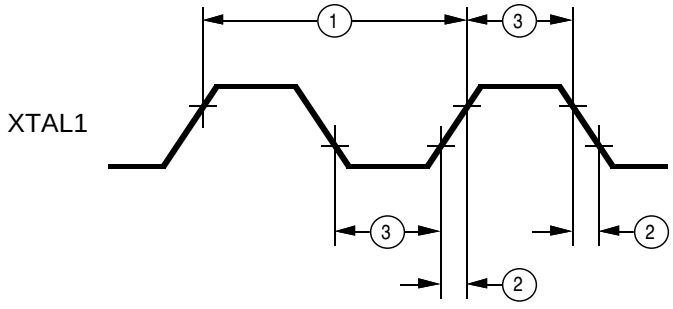
T_A=0°C to +70°C; V_{CC}=+4.5 V to +5.5 V; F_{OSC}=4 MHz

Symbol	Parameter	T_A=0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	1.48	V	
V_{ILC}	Input XTAL/Osc In Low		0.07 V_{CC}	0.98	V	External Clock Generator Driven
V_{IH}	Input Voltage	0.7 V_{CC}	V_{CC}	3.0	V	
V_{IHC}	Input XTAL/Osc in High	0.8 V_{CC}	V_{CC}	3.2	V	External Clock Generator Driven
V_{HY}	Schmitt Hysteresis	0.1 V_{CC}		0.8	V	
V_{PU}	Maximum Pull-up Voltage		12		V	[2]
V_{OL}	Output Voltage Low		0.4	0.16	V	I_{OL}=1.00 mA
			0.4	0.19	V	I_{OL}=3.2 mA, [1]
			0.4	0.19	V	I_{OL}=0.75 mA [2]
			1.5	1.00	V	I_{OL}=10 mA [1]
V_{00-01}	AFC Level 01 In		0.45 V_{CC}	1.9	V	
V_{01-11}	AFC Level 11 In	0.5 V_{CC}	0.75 V_{CC}	3.12	V	
V_{OH}	Output Voltage High	V_{CC}–0.4		4.75	V	I_{OH}= –0.75 mA
I_{IR}	Reset Input Current		–80	–46	µA	V_{RL}=0 V
I_{IL}	Input Leakage	–3.0	3.0	0.01	µA	0 V,V_{CC}
I_{OL}	Tri-State Leakage	–3.0	3.0	0.02	µA	0 V,V_{CC}
I_{CC}	Supply Current		20	13.2	mA	All inputs at rail
I_{CC1}			6	3.2	mA	All inputs at rail
I_{CC2}			10	0	µA	All inputs at rail

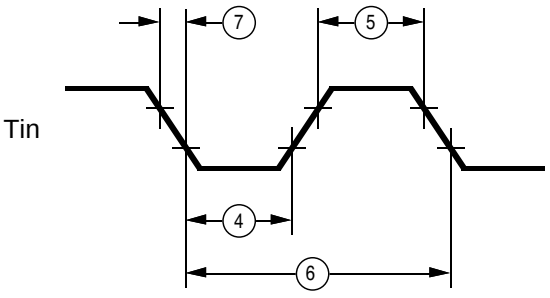
Notes:
[1] Port 5
[2] PWM Open-Drain

AC CHARACTERISTICS

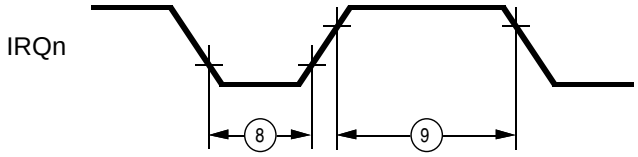
Timing Diagrams



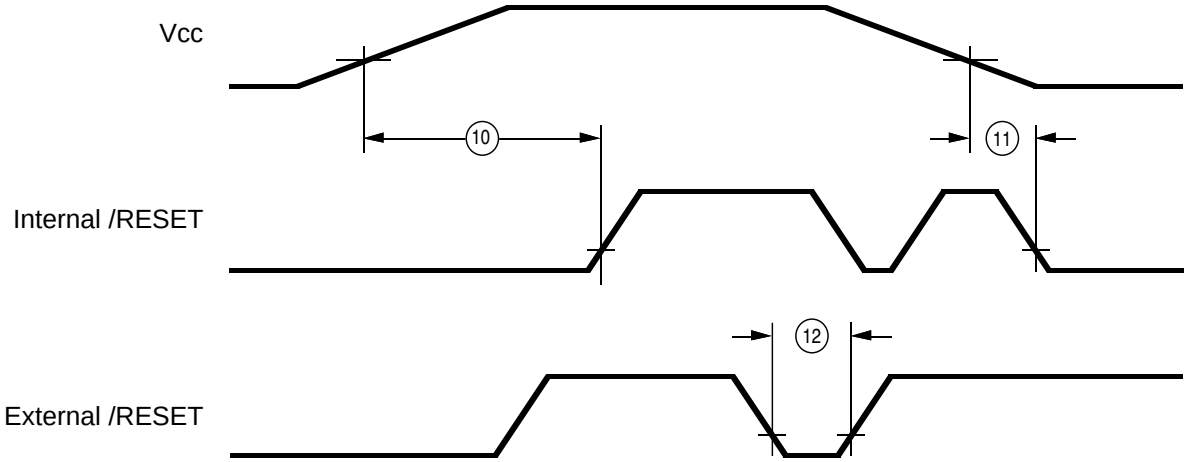
External Clock



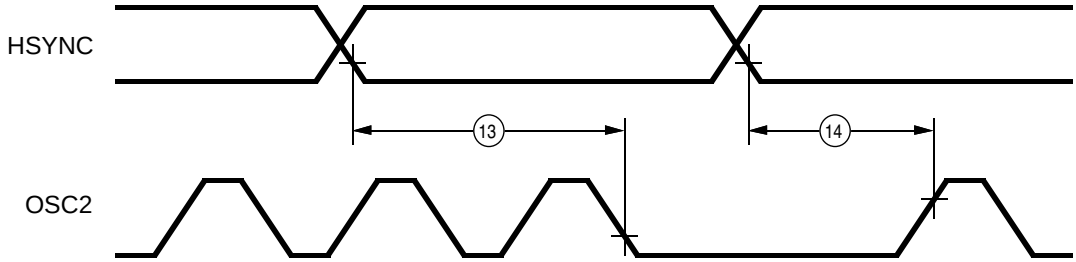
Counter Timer



Interrupt Request



Power On Reset



On Screen Display

AC CHARACTERISTICS

T_A=0° C to +70° C; V_{CC}=+4.5 V to +5.5 V; F_{OSC}=4 MHz,

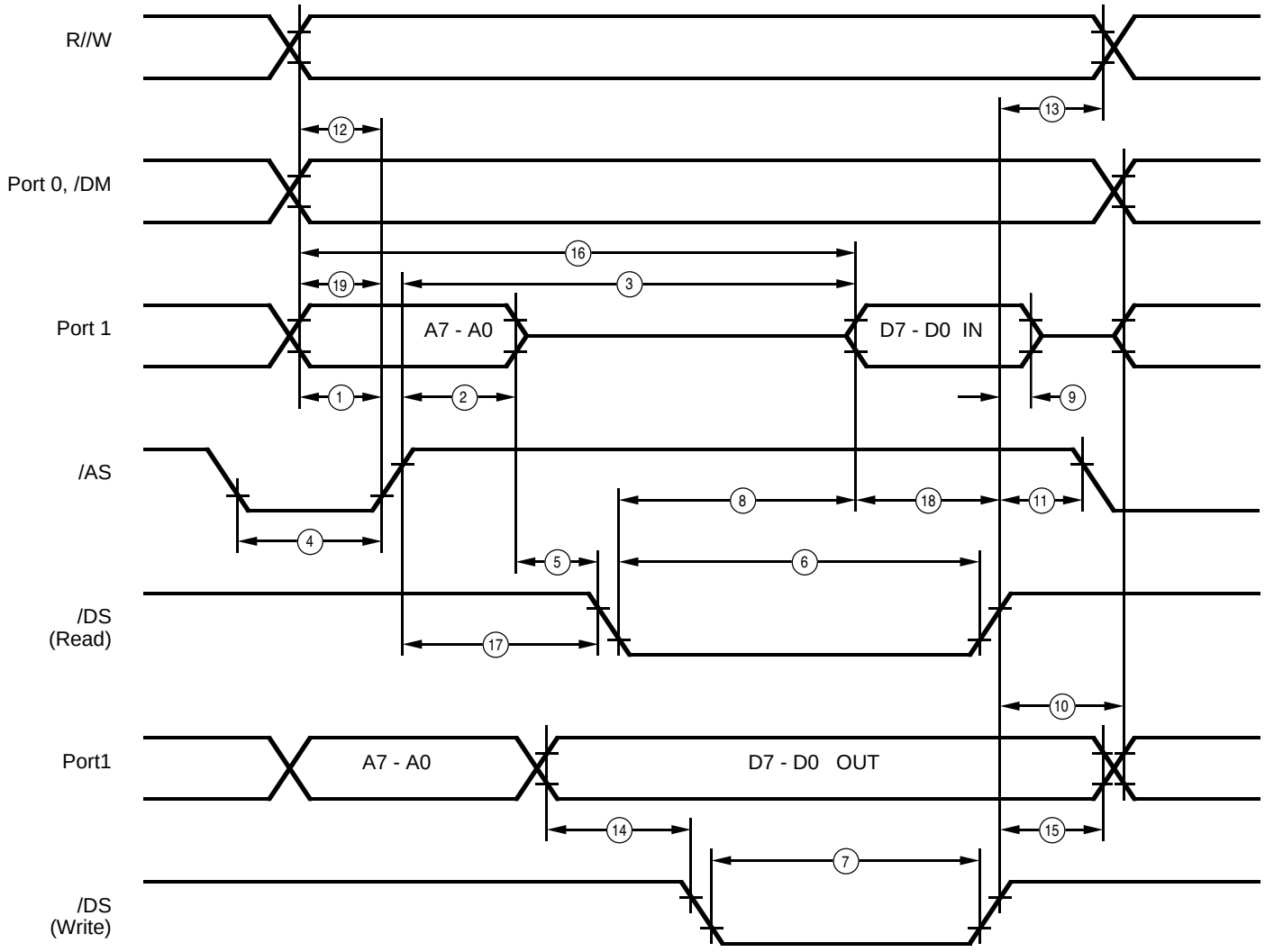
No	Symbol	Parameter	Min	Max	Unit
1	TpC	Input clock period	250	1000	ns
2	TrC,TfC	Clock input raise and fall		15	ns
3	TwC	Input clock width	125		ns
4	TwTinL	Timer input low width	70		ns
5	TwTinH	Timer input high width	3 TpC		
6	TpTin	Timer input period	8 TpC		
7	TrTin,TfTin	Timer input raise and fall		100	ns
8A	TwIL	Int req input low	70		ns
8B	TwIL		3 TpC		
9	TwIH	Int request input high	3 TpC		
10	TdPOR	Power On Reset delay	25	100	ms
11	TdLVIRES	Low voltage detect to In-Internal RESET condition	200		ns
12	TwRES	Reset minimum width	5 TpC		
13	TdHsOI	Hsync start to Vosc stop	2 TpV	3 TpV	
14	TdHsOh	Hsync end to Vosc start		1 TpV	
15	TdWDT	WDT Refresh Time		12	ms

Notes:
[1] Refer to DC Characteristics for details on switching levels.

* Units in nanoseconds

AC CHARACTERISTICS

Unique to Z86C97 External Memory Read/Write Timing Diagram



Z86C97 External Memory Read/Write Timing

AC CHARACTERISTICS

Unique to Z86C97, T_A=0°C to +70°C; V_{CC}=+4.5 V to +5.5 V; F_{OSC} = 4 MHz

No	Symbol	Parameter	Min	Max	Unit	Notes
1	TdA(AS)	Address Valid to /AS High Delay	35		ns	[2]
2	TdAS(AS)	/AS High to Address Float Delay	45		ns	[2]
3	TdAS(DR)	/AS High to Read Data Required Valid		250	ns	[1,2]
4	TwAS	/AS Low Width	55		ns	[2]
5	TdAZ(DS)	Address Float to /DS Low	0		ns	[2]
6	TwDSR	/DS (Read) Low Width	185		ns	[1,2]
7	TwDSW	DS (Write) Low Width	110		ns	[1,2]
8	TdDSR(DR)	/DS Low to Read Data Required Valid		130	ns	[1,2]
9	ThDR(DS)	Read Data to /DS High Hold		5	ns	
10	TdDS(A)	/DS High to Address Active Delay	55		ns	[2]
11	TdDS(AS)	/DS High to /AS Low Delay	55		ns	[2]
12	TdR/W(AS)	R//W Valid to /AS High Delay	35		ns	[2]
13	TdDS(R/W)	/DS High to R//W Not Valid	55		ns	[2]
14	TdDW(DSW)	Write Data Valid to /DS Low Delay	35		ns	[2]
15	TdDS(DW)	/DS High to Write Data Not Valid	55		ns	[2]
16	TdA(DR)	Address Valid to Read Data Required Valid		330	ns	[1,2]
17	TdAS(DS)	/AS High to /DS Low Delay	65		ns	[2]
18	TdDI(DS)	Data Input Setup to /DS High	75		ns	[1]

Notes:

[1] When using extended memory timing, for parameters 3, 6, 7, 8, and 16, add 2 TpC (250 ns @ 4.0 MHz).

[2] Min and Max times are in nanoseconds unless otherwise noted.

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