Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
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SFF20N60M
SFF20N60Z

DESIGNER'S DATA SHEET

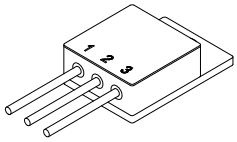
20 AMP / 600 Volts
Typ 0.30 Ω
N-Channel POWER MOSFET

Part Number / Ordering Information [1/]

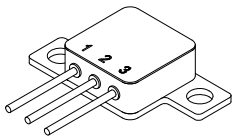
SFF20N60 ___ ___ ___

- **Screening** [2/] ___ = Not Screen; TX = TX Level; TXV = TXV Level; S = S Level
- **Lead Option** [3/] ___ = Straight Leads; DB = Down Bend; UB = Up Bend
- **Package** [3/] M = TO-254; Z = TO-254Z

TO-254 (M)



TO-254Z (Z)

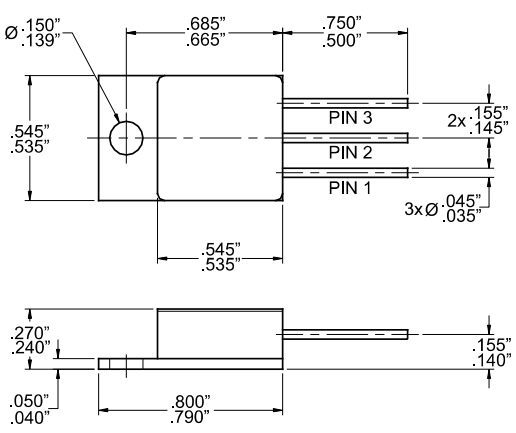


Features:

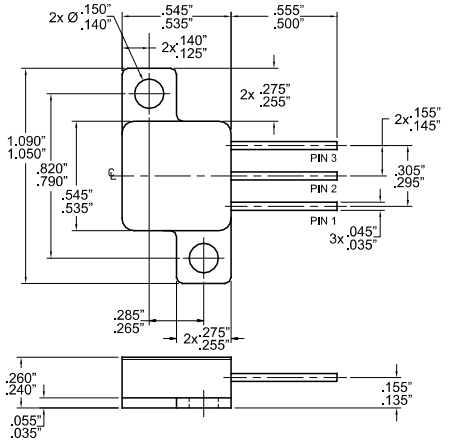
- Rugged Construction with Polysilicon Gate
- Low $R_{DS(ON)}$ and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dV/dt performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Hermetically Sealed, Isolated Surface Mount Power Package
- Ceramic Seals for Improved Hermeticity
- TX, TXV, S-Level screening available
- Replacement for IXTH20N60 Types

Maximum Ratings		Symbol	Value	Units
Drain – Source Voltage		V_{DS}	600	Volts
Gate – Source Voltage		V_{GS}	±30	Volts
Continues Drain Current		I_D	20	Amps
Avalanche Energy, repetitive **Avalanche energy, single pulse**		E_{AR} E_{AS}	0.03 1.0	J
Power Dissipation	T_C = 25ºC T_C = 55ºC	P_D	150 114	W
Operating & Storage Temperature		Top & Tstg	-55 to +175	ºC
Maximum Thermal Resistance Junction to Case		$R_{\theta JC}$	0.83	ºC/W

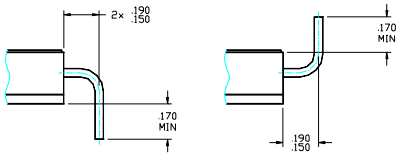
Case Outline: TO-254 (M)



Case Outline: TO-254Z (Z)



Optional Lead Bend Configuration



MDB & ZDB **MUB & ZUB**

Suffixes

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	DATA SHEET #: F00201D	DOC

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SFF20N60M
SFF20N60Z

Electrical Characteristics [3/]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage (V_{GS} = 0V, I_D = 250µA)		BV_{DSS}	600	—	—	Volts
Drain to Source On State Resistance (V_{GS} = 10V, I_D = 60% Rated ID)		$R_{DS(on)}$	—	0.30	0.35	Ω
On State Drain Current (V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max, V_{GS} = 10V)		$I_{D(on)}$	20	25	—	A
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 4mA)		$V_{GS(th)}$	2.0	3.4	4.5	V
Gate to Source Leakage (At Rated V_{GS})		I_{GSS}	—	—	±100	nA
Zero Gate Voltage Drain Current (V_{GS} = 0V)	V_{DS} = Rated, T_A = 25ºC V_{DS} = 80% Rated, T_A = 125ºC	I_{DSS}	— —	— —	25 1.0	µA mA
Forward Transconductance * (V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max, I_{DS} = 50% Rated ID)		g_{fs}	10	20	—	Mho
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 10V 50% Rated V_{DS} 50% Rated I_D	Q_g Q_{gs} Q_{gd}	— — —	100 23 45	170 40 85	nC
Turn on Delay Time **Rise Time** **Turn on Delay Time** **Fall Time**	V_{DD} = 50% Rated V_{DS} 50% Rated I_D R_G = 6.2Ω	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	28 30 80 25	40 60 150 60	nsec
Diode Forward Voltage * (I_S = Rated I_D, V_{GS} = 0V, T_J = 25°C)		V_{SD}	—	0.875	1.5	V
Diode Reverse Recovery Time **Reverse Recovery Charge** (I_F = 10A, di/dt = 100A/µsec, T_J = 25°C)		t_{rr} Q_{RR}	— —	240 1.3	800 —	nsec µC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0V V_{DS} = 25V f = 1MHz	C_{iss} C_{oss} C_{rss}	— — —	4000 400 120	— — —	pF

NOTES:

* Pulse test: pulse width = 300µsec, duty cycle = 2%

1/ For ordering information, price, and availability - contact factory.

2/ Screening based on MIL-PRF-19500. Screening flows available on request.

3/ Unless otherwise specified, all electrical characteristics @25ºC.

Available Part Numbers:

SFF20N60M; SFF20N60MDB; SFF20N60MUB;
SFF20N60Z; SFF20N60ZDB; SFF20N60ZUB;

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3