TEXAS INSTRUMENTS
DRV8251A
SLVSFU6 – JANUARY 2022

DRV8251A 4.1-A Brushed DC Motor Driver with Integrated Current Sense and Regulation

1 Features

- N-channel H-bridge brushed DC motor driver
- 4.5-V to 48-V operating supply voltage range
- Pin-to-pin, $R_{DS(on)}$, voltage, and current sense/ regulation variants (external shunt resistor and integrated current mirror)
  - DRV8870: 6.5-V to 45-V, 565-mΩ, shunt
  - DRV8251: 4.5-V to 48-V, 450-mΩ, shunt
  - DRV8251A: 4.5-V to 48-V, 450-mΩ, mirror
  - DRV8231: 4.5-V to 33-V, 600-mΩ, shunt
  - DRV8231A: 4.5-V to 33-V, 600-mΩ, mirror
- High output current capability: 4.1-A Peak
- PWM control interface
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Integrated IPROPI current sensing for stall detection and current regulation
- Low-power sleep mode
  - <1-µA at V_{VM} = 24-V, T_J = 25°C
- Small package and footprint
  - 8-Pin HSOP with PowerPAD™, 4.9 × 6.0 mm
- Integrated protection features
  - VM undervoltage lockout (UVLO)
  - Auto-retry overcurrent protection (OCP)
  - Thermal shutdown (TSD)

2 Applications

- Printers
- Vacuum robot
- Washer and dryer
- Coffee machine
- POS printer
- Electricity meter
- ATMs (Automated Teller Machines)
- Ventilators
- Surgical equipment
- Electronic hospital bed and bed control
- Fitness machine

3 Description

The DRV8251A device is an integrated motor driver with N-channel H-bridge, charge pump, current sense feedback, current regulation, and protection circuitry. The charge pump improves efficiency by supporting N-channel MOSFET half bridges and 100% duty cycle driving.

An internal current mirror architecture on the IPROPI pin implements current sensing and regulation. This eliminates the need for a large power shunt resistor, saving board area and reducing system cost. The IPROPI current-sense output allows a microcontroller to detect motor stall or changes in load conditions. The external voltage reference pin, VREF, determines the threshold of current regulation during start-up and stall events without interaction from a microcontroller.

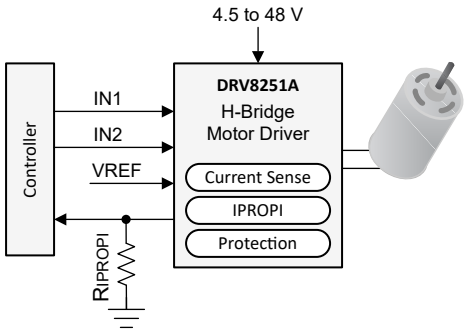
A low-power sleep mode achieves ultra-low quiescent current draw by shutting down most of the internal circuitry. Internal protection features include supply undervoltage lockout, output overcurrent, and device overtemperature.

The DRV8251A is part of a family of devices which come in pin-to-pin, scalable $R_{DS(on)}$ and supply voltage options to support various loads and supply rails with minimal design changes. See Section 5 for information on the devices in this family. View the full portfolio of brushed motor drivers on ti.com.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8251ADDA	HSOP (8)	4.90 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2022	*	Initial Release

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5 Device Comparison

Table 5-1. Device Comparison Table

Device name	Supply voltage (V)	$R_{DS(on)}$ (mΩ)	Current regulation	Current-sense feedback	Overcurrent protection response	Package	Pin-to-pin devices
DRV8870	6.5 to 45	565	External Shunt Resistor	External Amplifier	Automatic Retry	HSOP (4.9x6)	DRV8870, DRV8251, DRV8231
DRV8251	4.5 to 48	450			Latched Disable	HSOP (4.9x6)	
DRV8231	4.5 to 33	600			Automatic Retry	HSOP (4.9x6) WSON (2x2)	
DRV8251A	4.5 to 48	450	Internal current mirror (IPROPI)		Automatic Retry	HSOP (4.9x6)	DRV8251A, DRV8231A
DRV8231A	4.5 to 33	600			Automatic Retry	HSOP (4.9x6) WSON (2x2)	

6 Pin Configuration and Functions

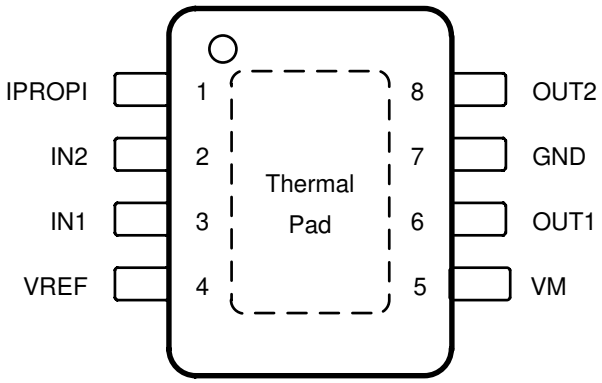


Figure 6-1. DDA Package 8-Pin HSOP Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	7	PWR	Device power ground. Connect to system ground.
IN1	3	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns. See Table 8-2.
IN2	2	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns. See Table 8-2.
IPROPI	1	PWR	Analog current output proportional to load current. Section 8.4.2.1.
OUT1	6	O	H-bridge output. Connect directly to the motor or other inductive load.
OUT2	8	O	H-bridge output. Connect directly to the motor or other inductive load.
VM	5	PWR	4.5-V to 48-V power supply. Connect a 0.1-µF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
VREF	4	I	Analog input. Apply a voltage between 0 to 5 V. For information on current regulation, see the Section 8.4.2.1 section.
PAD		—	Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.3	50	V
Power supply transient voltage ramp	VM	0	2	V/µs
Logic pin voltage	INx	-0.3	7	V
Reference input pin voltage	VREF	-0.3	6	V
Output pin voltage	OUTx	-0.7	VM + 0.7	V
Current sense input pin voltage	IPROPI	-0.3	5.75	V
Output current	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ± 6000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 750 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	VM	4.5		48	V
V_{VREF}	Reference voltage	VREF	0		3.6	V
V_{IN}	Logic input voltage	INx	0		5.5	V
f_{PWM}	PWM frequency	INx	0		200	kHz
I_{OUT} (1)	Peak output current, 4.5 ≤ V_{VM} < 5.5 V	OUTx	0		3.7	A
	Peak output current, V_{VM} ≥ 5.5 V		0		4.1	A
I_{IPROPI}	Peak output current	IPROPI	0		3	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		DRV8251A DDA (HSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.4	°C/W

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THERMAL METRIC(1)		DRV8251A DDA (HSOP) 8 PINS	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

4.5 V ≤ V_{VM} ≤ 48 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 25 °C and V_{VM} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
I_{VMQ}	VM sleep mode current	V_{VM} = 24 V, IN1 = IN2 = 0, T_J = 25°C			1	µA
I_{VM}	VM active mode current	V_{VM} = 24 V, IN1 = IN2 = 1		3	4	mA
t_{WAKE}	Turnon time	Control signal to active mode			250	µs
t_{SLEEP}	Turnoff time	Control signal to sleep mode	0.8		1.5	ms
LOGIC-LEVEL INPUTS (INx)						
V_{IL}	Input logic low voltage				0.5	V
V_{IH}	Input logic high voltage		1.5			V
V_{HYS}	Input hysteresis			200		mV
I_{IL}	Input logic low current	V_{IN} = 0 V	-1		1	µA
I_{IH}	Input logic high current	V_{IN} = 3.3 V		33	100	µA
R_{PD}	Input pulldown resistance	To GND		100		kΩ
DRIVER OUTPUTS (OUTx)						
$R_{DS(on)_HS}$	High-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		225		mΩ
$R_{DS(on)_LS}$	Low-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		225		mΩ
V_{SD}	Body diode forward voltage	I_{OUT} = 1 A		0.8		V
t_{RISE}	Output rise time	V_{VM} = 24 V, OUTx rising from 10% to 90%		220		ns
t_{FALL}	Output fall time	V_{VM} = 24 V, OUTx falling from 90% to 10%		220		ns
t_{PD}	Input to output propagation delay	INx to OUTx		0.7	1	µs
t_{DEAD}	Output dead time			200		ns
INTEGRATED CURRENT SENSE AND REGULATION (IPROPI, VREF)						
A_{IPROPI}	Current mirror scaling factor			1575		µA/A
A_{ERR}	Current mirror total error	I_{OUT} = 1.5 A, V_{VM} ≥ 6.5 V, V_{IPROPI} ≤ 3.0 V	-5		5	%
t_{OFF}	Current regulation off time			25		µs
t_{BLK}	Current regulation blanking time			1.4		µs
t_{DELAY}	Current sense delay time			1.1		µs
t_{DEG}	Current regulation deglitch time			0.7		µs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising	4.15	4.3	4.45	V
		Supply falling	4.05	4.2	4.35	V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		100		mV

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4.5 V ≤ V_{VM} ≤ 48 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 25 °C and V_{VM} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{UVLO}	Supply undervoltage deglitch time			10		µs
I_{OCP}	Overcurrent protection trip point	4.5 ≤ V_{VM} < 5.5 V	3.7			A
		V_{VM} ≥ 5.5 V	4.1			A
t_{OCP}	Overcurrent protection deglitch time			1.5		µs
t_{RETRY}	Overcurrent protection retry time			3		ms
T_{TSD}	Thermal shutdown temperature		150	175		°C
T_{HYS}	Thermal shutdown hysteresis			40		°C

7.6 Typical Characteristics

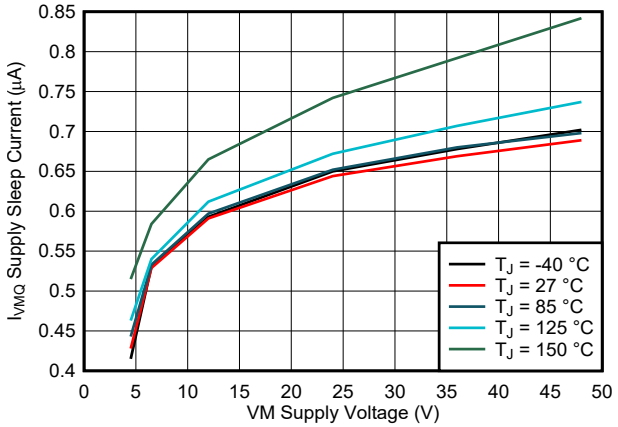


Figure 7-1. Sleep Current (I_{VMQ}) vs. Supply Voltage (V_{VM})

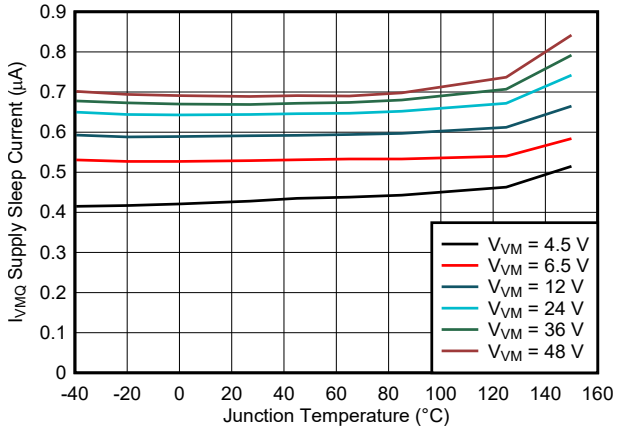


Figure 7-2. Sleep Current (I_{VMQ}) vs. Junction Temperature (T_J)

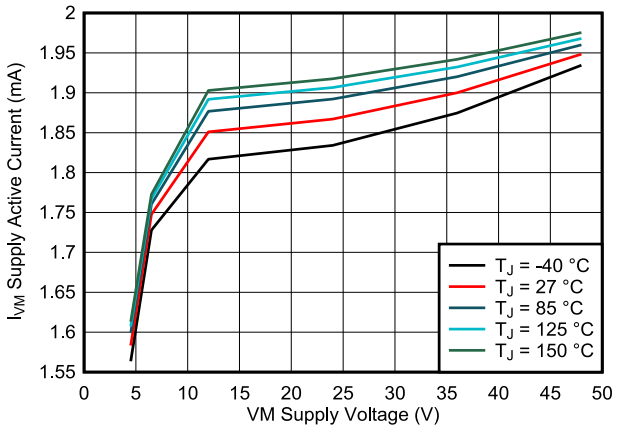


Figure 7-3. Active Current (I_{VM}) vs. Supply Voltage (V_{VM})

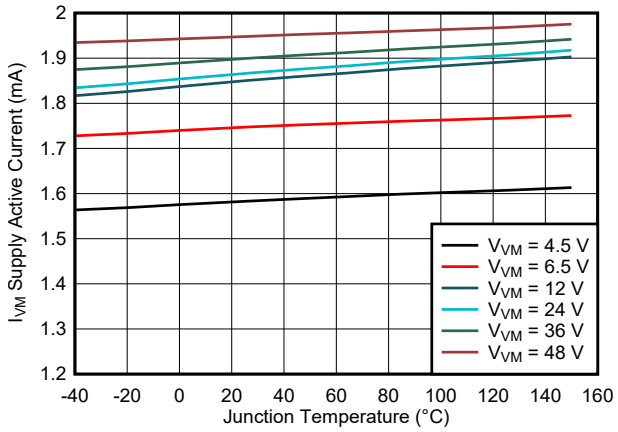


Figure 7-4. Active Current (I_{VM}) vs. Junction Temperature (T_J)

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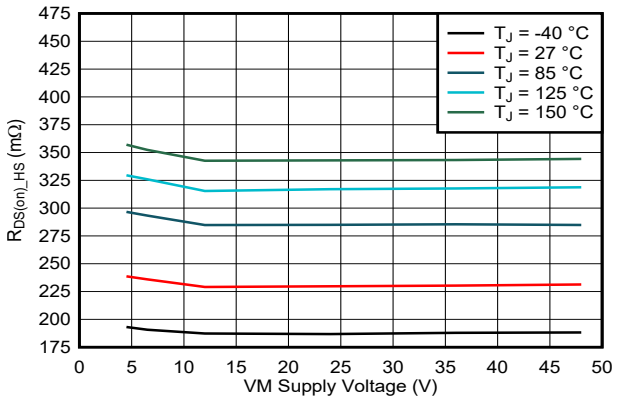


Figure 7-5. High-Side $R_{DS(on)}$ vs. VM Supply Voltage

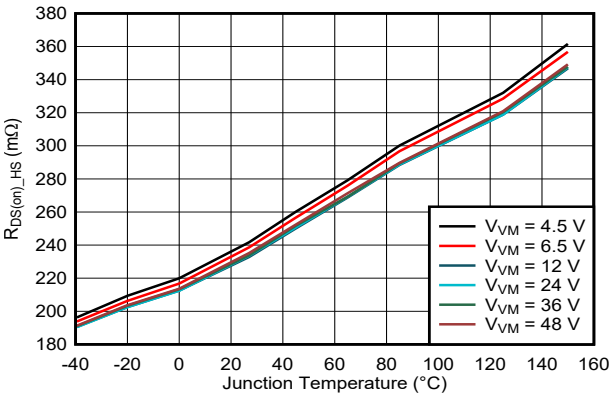


Figure 7-6. High-Side $R_{DS(on)}$ vs. Junction Temperature (T_J)

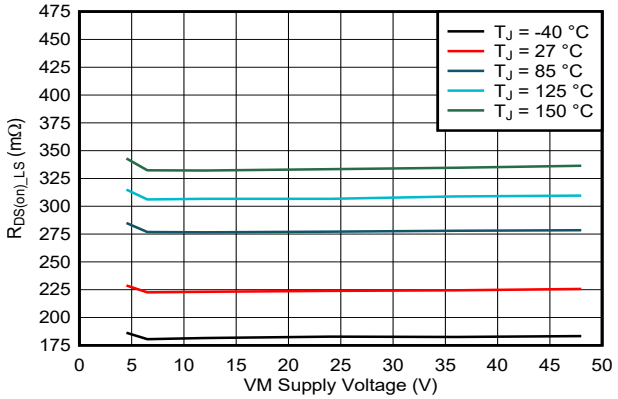


Figure 7-7. Low-Side $R_{DS(on)}$ vs. VM Supply Voltage

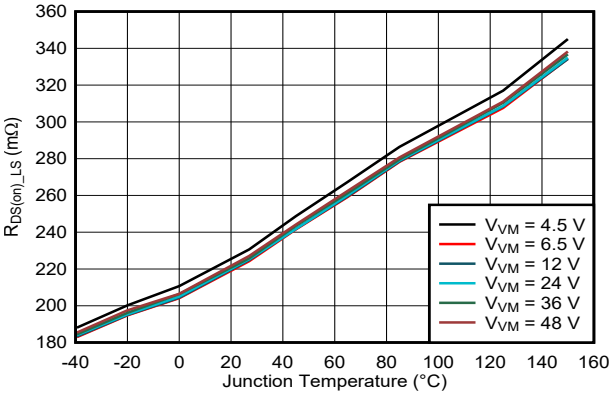
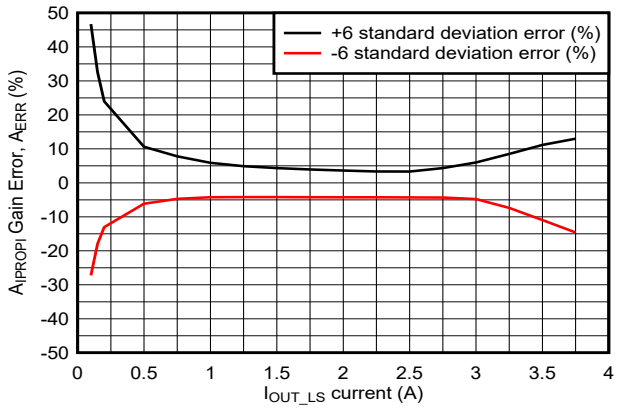


Figure 7-8. Low-Side $R_{DS(on)}$ vs. Junction Temperature (T_J)



6.5 V ≤ V_{VM} ≤ 48 V 0 V ≤ V_{IPROPI} ≤ 3 V -40 °C ≤ T_J ≤ 150 °C

Figure 7-9. Gain error of AIPROPI vs. Motor Current

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7.7 Timing Diagrams

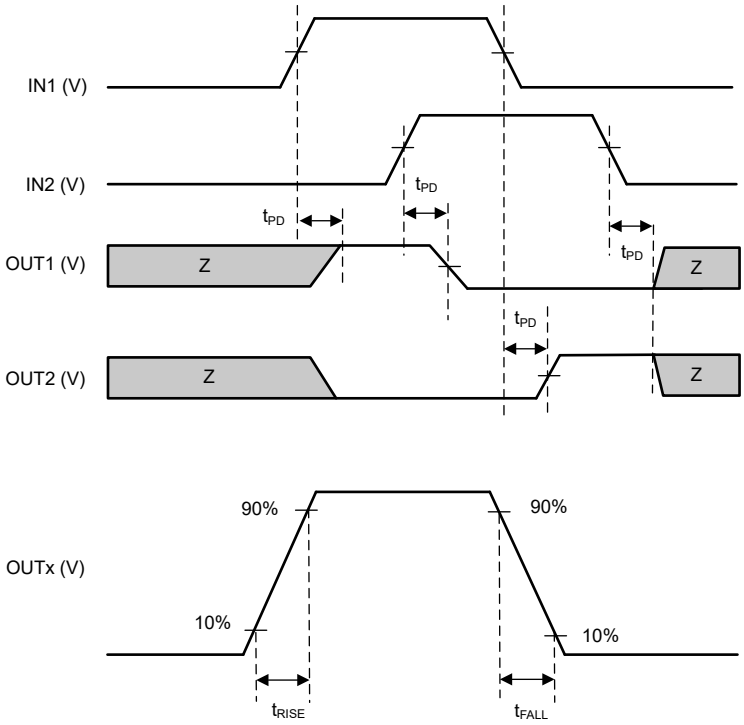


Figure 7-10. Input-to-Output Timing

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8 Detailed Description

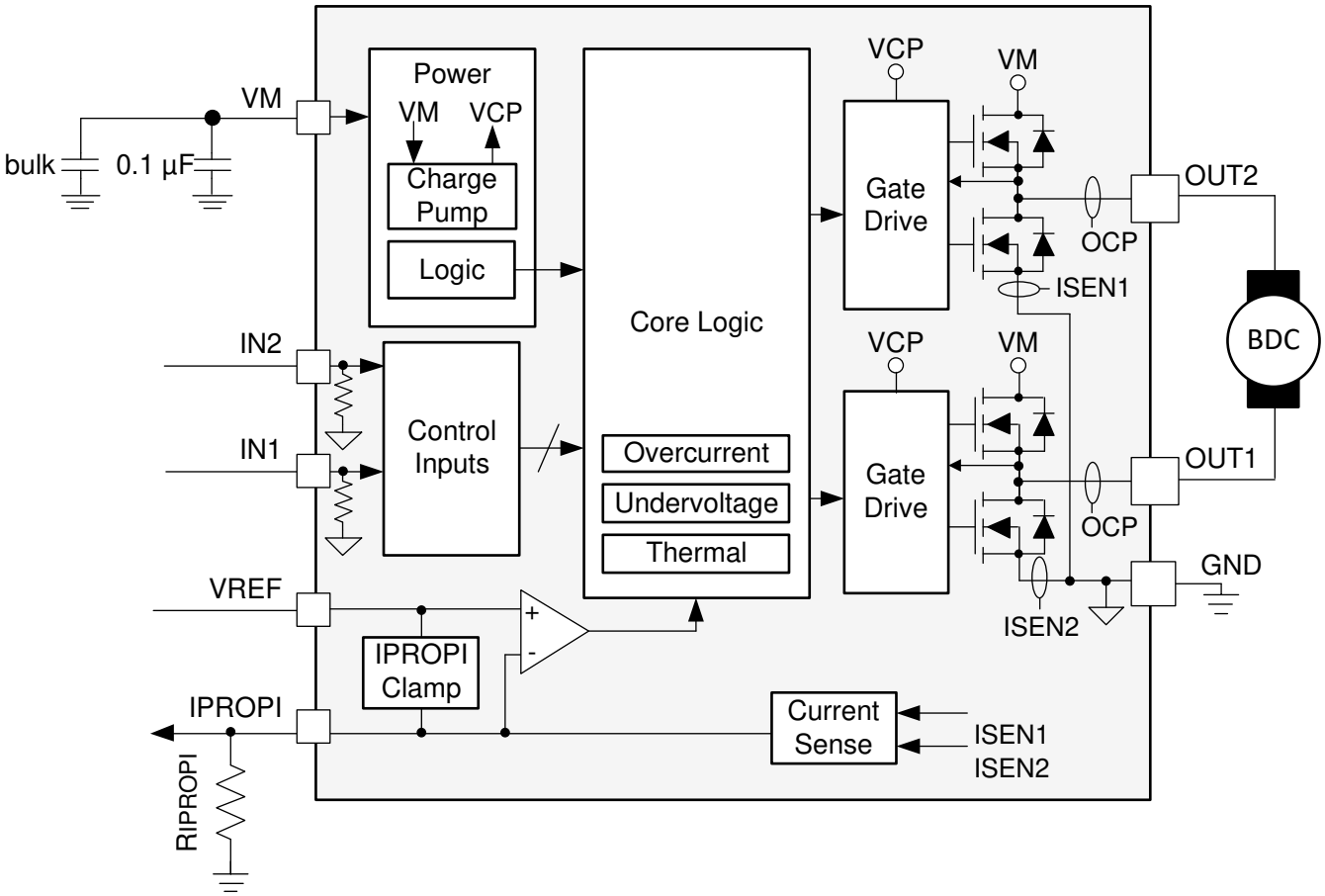
8.1 Overview

The DRV8251A is an 8-pin device for driving brushed DC motors from a 4.5-V to 48-V supply rail. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 450 mΩ (including one high-side and one low-side FET). A single power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation at frequencies between 0 to 200 kHz. The device enters a low-power sleep mode by bringing both inputs low.

The DRV8251A also integrates current sense feedback to a microcontroller using current mirrors on the low-side power MOSFETs. The IPROPI pin sources a small current that is proportional to the current in the MOSFETs. This current can be converted to a proportional voltage using an external resistor (R_{IPROPI}). This integrated current sensing scheme out-performs traditional external shunt resistor sensing by providing current information even during the off-time slow decay recirculating period and removing the need for an external power shunt resistor. The integrated current regulation feature allows the device to limit the output current with a fixed off-time PWM chopping scheme. The VREF pin configures the current regulation level during motor operation to limit the load current.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

8.2 Functional Block Diagram



8.3 External Components

Table 8-1 lists the recommended external components for the device.

Table 8-1. Recommended external components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF, low ESR ceramic capacitor, VM-rated.
C_{VM2}	VM	GND	Section 10.1, VM-rated.

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8.4 Feature Description

8.4.1 Bridge Control

The DRV8251A output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in Table 8-2.

Table 8-2. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast current decay* is also available. Figure 8-1 shows how the motor current flows through the H-bridge. The input pins can be powered before VM is applied.

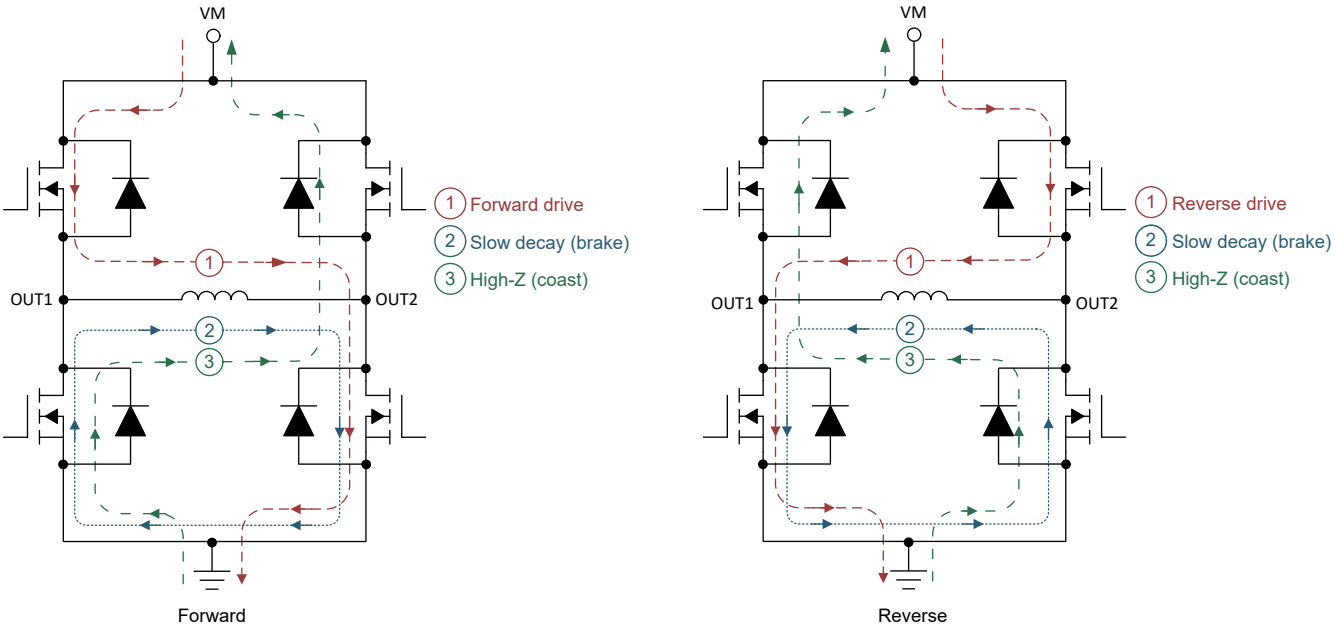


Figure 8-1. H-Bridge Current Paths

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

The propagation delay time (t_{PD}) is measured as the time between an input edge to output change. This time accounts for input deglitch time and other internal logic propagation delays. The input deglitch time prevents noise on the input pins from affecting the output state. Additional output slew delay timing accounts for FET turn on or turn off times (t_{RISE} and t_{FALL}).

Figure 8-2 below shows the timing of the inputs and outputs of the motor driver.

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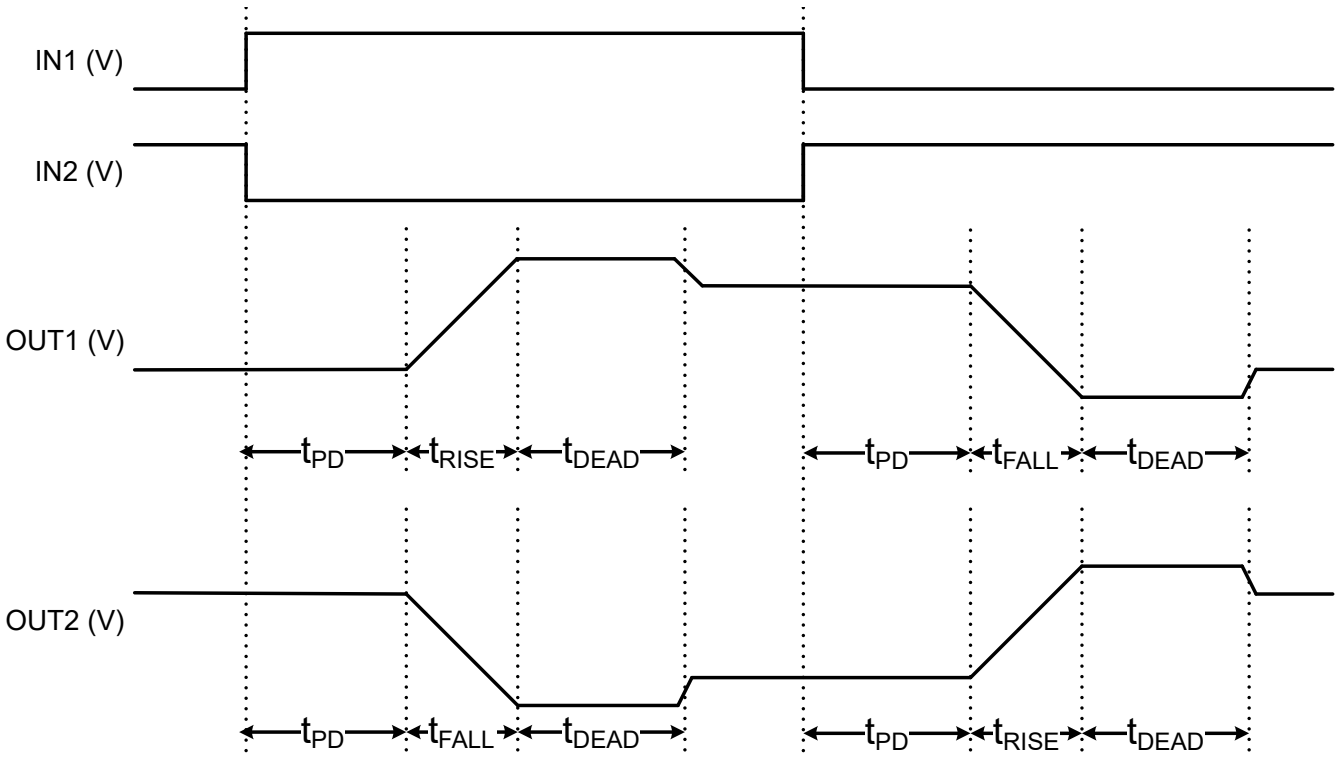


Figure 8-2. H-Bridge Timing Diagram

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8.4.2 Current Sense and Regulation (IPROPI)

The DRV8251A device integrates current sensing, regulation, and feedback as part of the IPROPI feature. These features allow the device to sense the output current without an external sense resistor or sense circuitry reducing system size, cost, and complexity. This also allows for the device to limit the output current in the case of motor stall or high torque events and give detailed feedback to the controller about the load current through a current proportional output. Figure 8-3 shows the IPROPI timings specified in the Electrical Characteristics table.

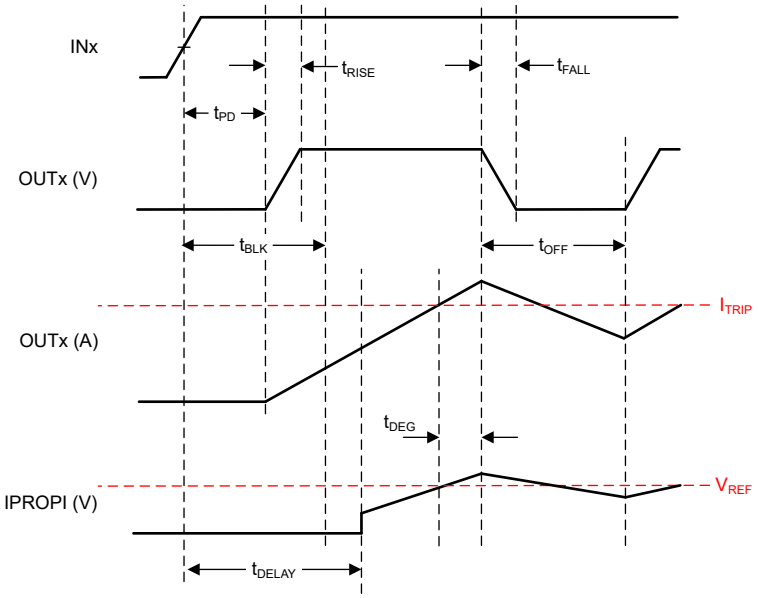


Figure 8-3. Detailed IPROPI Timing Diagram

8.4.2.1 Current Sensing

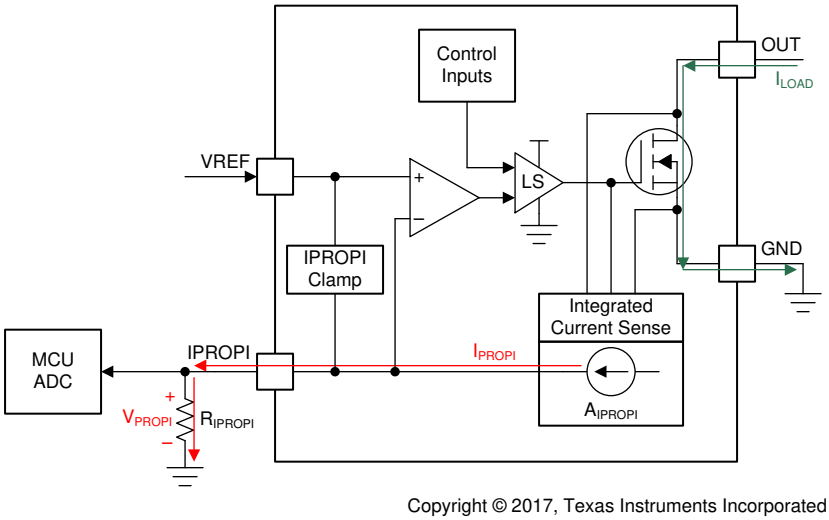
The IPROPI pin outputs an analog current proportional to the current flowing through the low-side power MOSFETs in the H-bridge scaled by A_{IPROPI}. The IPROPI output current can be calculated by Equation 1. The I_{LSx} in Equation 1 is only valid when the current flows from drain to source in the low-side MOSFET. If current flows from source to drain or through the body diode, the value of I_{LSx} for that channel is zero. For instance, if the bridge is in the brake, slow-decay state, then the current out of IPROPI is only proportional to the current in one of the low-side MOSFETs.

$$I_{PROPI}\ (\mu A) = (I_{LS1} + I_{LS2})\ (A) \times A_{IPROPI}\ (\mu A/A) \quad (1)$$

The A_{ERR} parameter in the Electrical Characteristics table is the error associated with the A_{IPROPI} gain. It indicates the combined effect of offset error added to the I_{OUT} current and gain error.

The motor current is measured by an internal current mirror architecture on the low-side FETs which removes the need for an external power sense resistor as shown in Figure 8-4. The current mirror architecture allows for the motor winding current to be sensed in both the drive and brake low-side slow-decay periods allowing for continuous current monitoring in typical bidirectional brushed DC motor applications. In coast mode, the current is freewheeling and cannot be sensed because it flows from source to drain. However, the current can be sampled by briefly reenabling the driver in either drive or slow-decay modes and measuring the current before switching back to coast mode again.

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Figure 8-4. Integrated Current Sensing

The IPROPI pin should be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin with the I_{IPROPI} analog current output. This allows for the load current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized. Additionally, the DRV8251A device implements an internal IPROPI voltage clamp circuit to limit V_{IPROPI} with respect to V_{VREF} on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events.

The corresponding IPROPI voltage to the output current can be calculated by Equation 2.

$$V_{IPROPI}\ (V) = I_{PROPI}\ (A) \times R_{IPROPI}\ (\Omega) \quad (2)$$

The IPROPI output bandwidth is limited by the sense delay time (t_{DELAY}) of the internal current sensing circuit. This time is the delay from the low-side MOSFET enable command (from the INx pins) to the IPROPI output being ready.

If the device is alternating between drive and slow-decay (brake) in an H-bridge PWM pattern then the low-side MOSFET sensing the current is continuously on and the sense delay time has no impact to the IPROPI output. If a command on the INx pins disables the low-side MOSFETs (according to the logic tables in Section 8.4.1), the IPROPI output will disable with the input logic signal. Although the low-side MOSFETs may still conduct current as they disable according to the device slew rate (noted in the Electrical Characteristics table by t_{RISE} time), IPROPI will not represent the current in the low-side MOSFETs during this turnoff time.

8.4.2.2 Current Regulation

The DRV8251A device integrates current regulation using a fixed off-time current chopping scheme. This allows the devices to limit the output current in case of motor stall, high torque, or other high current load events without involvement from the external controller as shown in Figure 8-5.

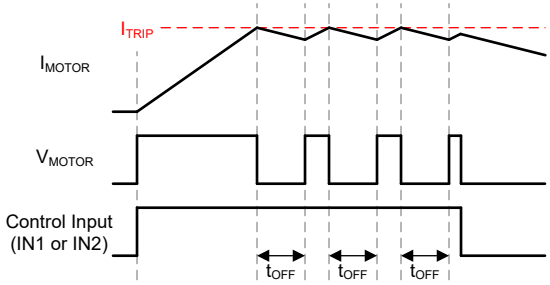


Figure 8-5. Off-Time Current-Regulation

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The current chopping threshold (I_{TRIP}) is set through a combination of the VREF voltage (V_{VREF}) and IPROPI output resistor (R_{IPROPI}). This is done by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} with an internal comparator.

$$I_{TRIP}\ (A) \times A_{IPROPI}\ (\mu A/A) = V_{VREF}\ (V) / R_{IPROPI}\ (\Omega) \quad (3)$$

For example, if V_{VREF} = 3.3 V, R_{IPROPI} = 1310 Ω, and A_{IPROPI} = 1575 µA/A, then I_{TRIP} will be approximately 1.6 A.

The fixed off-time current chopping scheme supports up to 100% duty cycle current regulation since the H-bridge automatically enables after the t_{OFF} period and does not require a new control input edge on the INx pins to reset the outputs. When the motor current exceeds the I_{TRIP} threshold, the outputs will enter a current chopping mode with a fixed off time (t_{OFF}). During t_{OFF}, the H-bridge enters a brake/low-side slow decay state (both low-side MOSFETs ON) for t_{OFF} duration after I_{OUT} exceeds I_{TRIP}. After t_{OFF}, the outputs re-enable according to the control inputs if I_{OUT} is less than I_{TRIP}. If I_{OUT} is still greater than I_{TRIP}, the H-bridge enters another period of brake/low-side slow decay for t_{OFF}. If the state of the INx control pins changes during the t_{OFF} time, the remainder of the t_{OFF} time is ignored, and the outputs will again follow the inputs.

The I_{TRIP} comparator has both a blanking time (t_{BLK}) and a deglitch time (t_{DEG}). The internal blanking time helps to prevent voltage and current transients during output switching from effecting the current regulation. These transients may be caused by a capacitor inside the motor or on the connections to the motor terminals. The internal deglitch time ensures that transient conditions do not prematurely trigger the current regulation. In certain cases where the transient conditions are longer than the deglitch time, placing a 10-nF capacitor on the IPROPI pin, close to the device, will help filter the transients on IPROPI output so current regulation does not prematurely trigger. The capacitor value can be adjusted as needed, however large capacitor values may slow down the response time of the current regulation circuitry.

The internal current regulation and current feedback can be disabled by tying IPROPI to GND and setting the VREF pin voltage greater than GND. If current feedback is required and current regulation is not required, set V_{VREF} and R_{IPROPI} such that V_{IPROPI} never reaches the V_{VREF} threshold. For proper operation of the current regulation circuit, V_{VREF} must be within the range of the VREF pin voltages specified in the Recommended Operating Conditions table.

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8.4.3 Protection Circuits

The DRV8251A device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

8.4.3.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive internally. If this analog current limit persists for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge will disable. The driver re-enables after the OCP retry period (t_{RETRY}) has passed. If the fault condition is still present, the cycle repeats as shown in Figure 8-6.

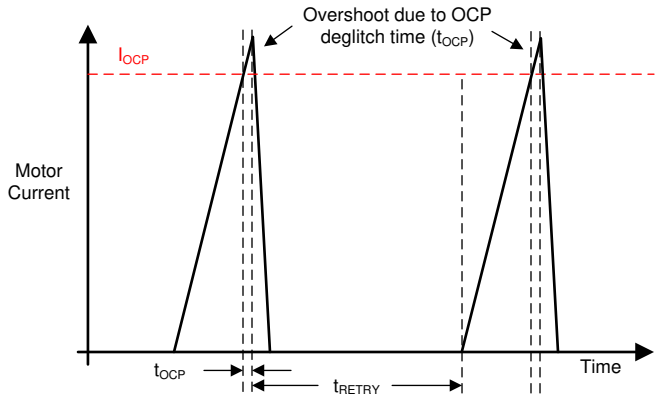


Figure 8-6. OCP Operation

Overcurrent conditions are detected independently on both high- and low-side FETs. This means that a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for current regulation, so it functions regardless of VREF and IPROPI settings.

8.4.3.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

8.4.3.3 VM Undervoltage Lockout (UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, the output FETS are disabled, and all internal logic is reset. Operation continues when the V_{VM} voltage rises above the UVLO rising threshold as shown in Figure 8-7.

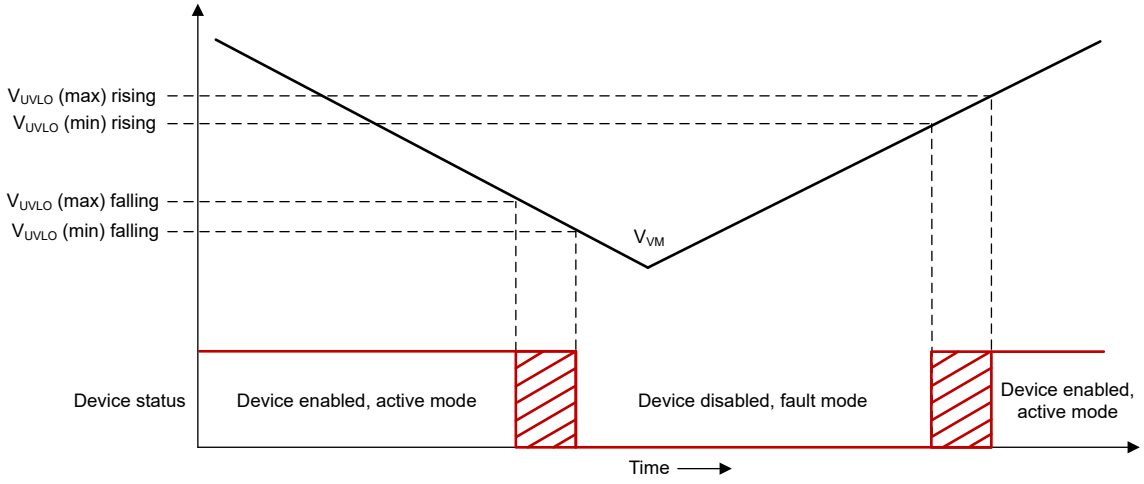


Figure 8-7. VM UVLO Operation

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8.5 Device Functional Modes

Table 8-3 summarizes the DRV8251A functional modes described in this section.

Table 8-3. Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	IN1 or IN2 = logic high	Operating	Operating
Low-Power Sleep Mode	IN1 = IN2 = logic low	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See Table 8-4

8.5.1 Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold V_{UVLO}, the INx pins are in a state other than IN1 = 0 & IN2 = 0, and t_{WAKE} has elapsed, the device enters active mode. In this mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs.

8.5.2 Low-Power Sleep Mode

When the IN1 and IN2 pins are both low for time t_{SLEEP}, the DRV8251A device enters a low-power sleep mode. In sleep mode, the outputs remain High-Z and the device draws minimal current from the supply pin (I_{VMQ}). If the device is powered up while all inputs are low, it immediately enters sleep mode. After any of the input pins are set high for longer than the duration of t_{WAKE}, the device becomes fully operational. Figure 8-8 shows an example timing diagram for entering and leaving sleep mode.

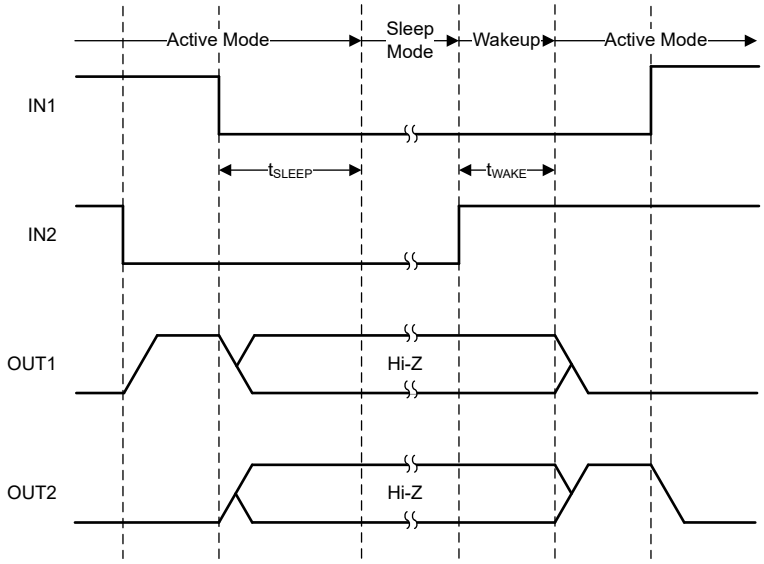


Figure 8-8. Sleep Mode Entry and Wakeup Timing Diagram

8.5.3 Fault Mode

The DRV8251A device enters a fault mode when a fault is encountered. This is utilized to protect the device and the output load. The device behavior in the fault mode is described in Table 8-4 and depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the recovery condition is met.

Table 8-4. Fault Conditions Summary

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	$V_M < V_{UVLO,falling}$	Disabled	Disabled	$V_M > V_{UVLO,rising}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	Operating	$I_{OUT} < I_{OCP}$
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	Disabled	Operating	$T_J < T_{TSD} – T_{HYS}$

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8.6 Pin Diagrams

8.6.1 Logic-Level Inputs

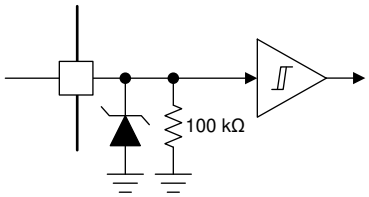


Figure 8-9. Logic-level input

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8251A device is typically used to drive one brushed DC motor.

9.2 Typical Application

9.2.1 Brush DC Motor

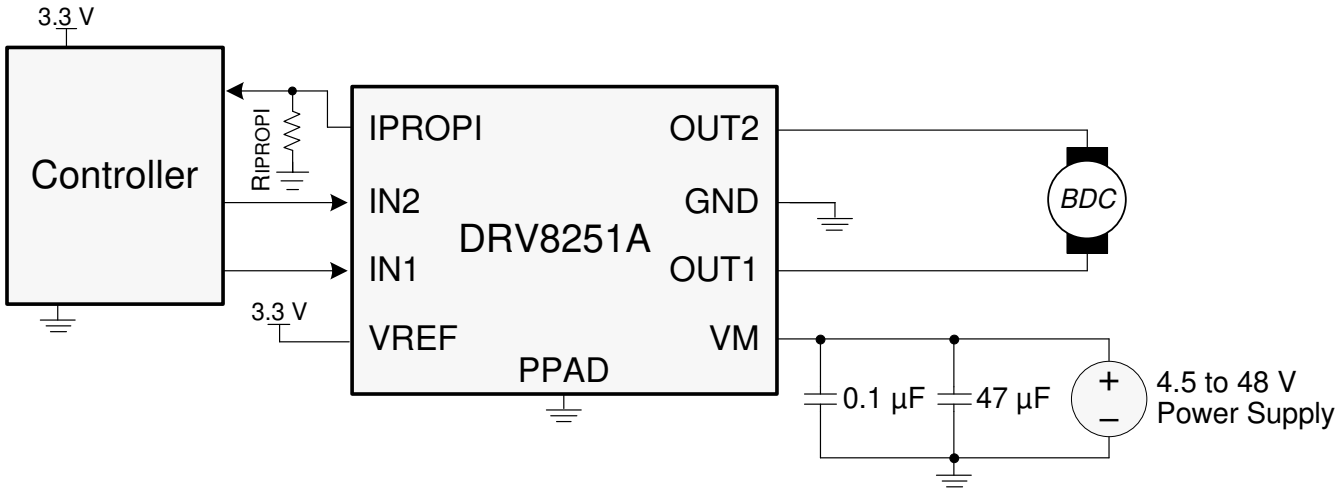


Figure 9-1. Typical Connections

9.2.1.1 Design Requirements

The table below lists the design parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_{VM}	12 V
Average motor current	I_{AVG}	0.8 A
Motor inrush (startup) current	I_{INRUSH}	2.1 A
Motor stall current	I_{STALL}	2.1 A
Motor current trip point	I_{TRIP}	1.9 A
VREF voltage	VREF	3.3 V
IPROPI sense resistance	R_{IPROPI}	1.5 kΩ
PWM frequency	f_{PWM}	50 kHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Motor Voltage

The motor voltage to use depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

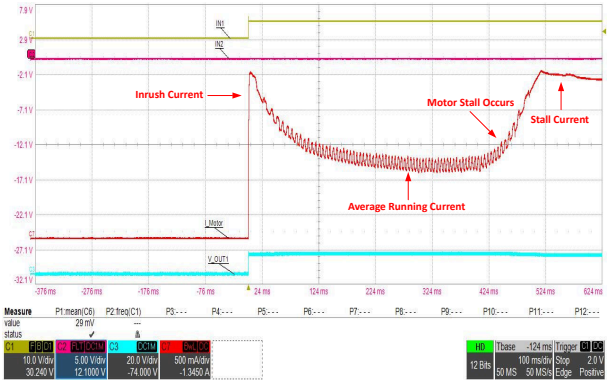
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9.2.1.2.2 Motor Current

Motors experience large currents at low speed, initial startup, and stalled rotor conditions. The large current at motor startup is sometimes called inrush current. The current regulation feature in the DRV8251A can help to limit these large currents. Figure 9-4 and Figure 9-5 show examples of limiting inrush current.

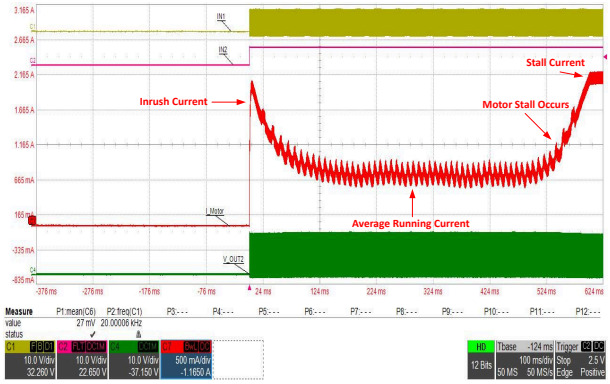
Alternatively, the microcontroller may limit the inrush current by ramping the PWM duty cycle during the startup time.

9.2.1.3 Application Curves



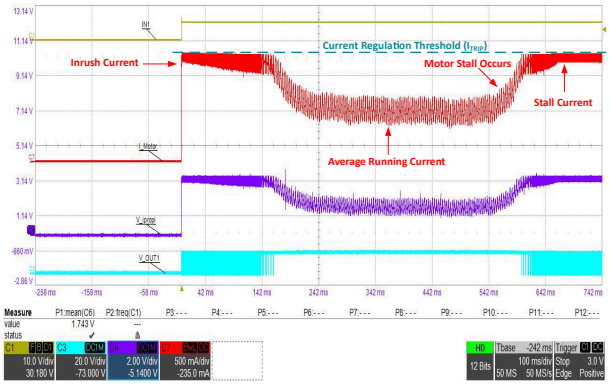
Ch 1 (Yellow) = IN1 Signal Ch 2 (Magenta) = IN2 Signal
Ch 3 (Blue) = OUT1 Voltage Ch 7 (Red) = Motor Current

Figure 9-2. Motor startup at 100% duty cycle



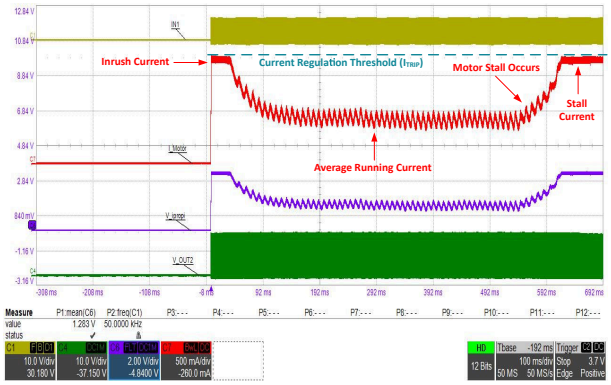
Ch 1 (Yellow) = IN1 Signal Ch 2 (Magenta) = IN2 Signal
Ch 4 (Green) = OUT2 Voltage Ch 7 (Red) = Motor Current

Figure 9-3. Motor startup at 50% duty cycle



Ch 1 (Yellow) = IN1 Signal Ch 3 (Blue) = OUT1 Voltage
Ch 6 (Purple) = IPROPI Signal Ch 7 (Red) = Motor Current

Figure 9-4. Motor startup at 100% duty cycle with current regulation



Ch 1 (Yellow) = IN1 Signal Ch 4 (Green) = OUT2 Voltage
Ch 6 (Purple) = IPROPI Signal Ch 7 (Red) = Motor Current

Figure 9-5. Motor startup at 50% duty cycle with current regulation

9.2.2 Stall Detection

Some applications require stall detection to notify the microcontroller of a locked rotor condition. A stall could be caused by one of two things: unintended mechanical blockage or the load reaching an end-stop in a constrained travel path. By using the IPROPI analog current sense feedback of the DRV8251A, the system can implement a simple stall detection scheme.

The principle of this stall detection scheme relies on the fact that motor current increases during stall conditions as shown in Figure 9-6. To implement stall detection, the microcontroller reads the voltage on the IPROPI pin using an ADC and compares it to a stall threshold set in firmware. Alternatively, a comparator peripheral may be used to set this threshold as well.

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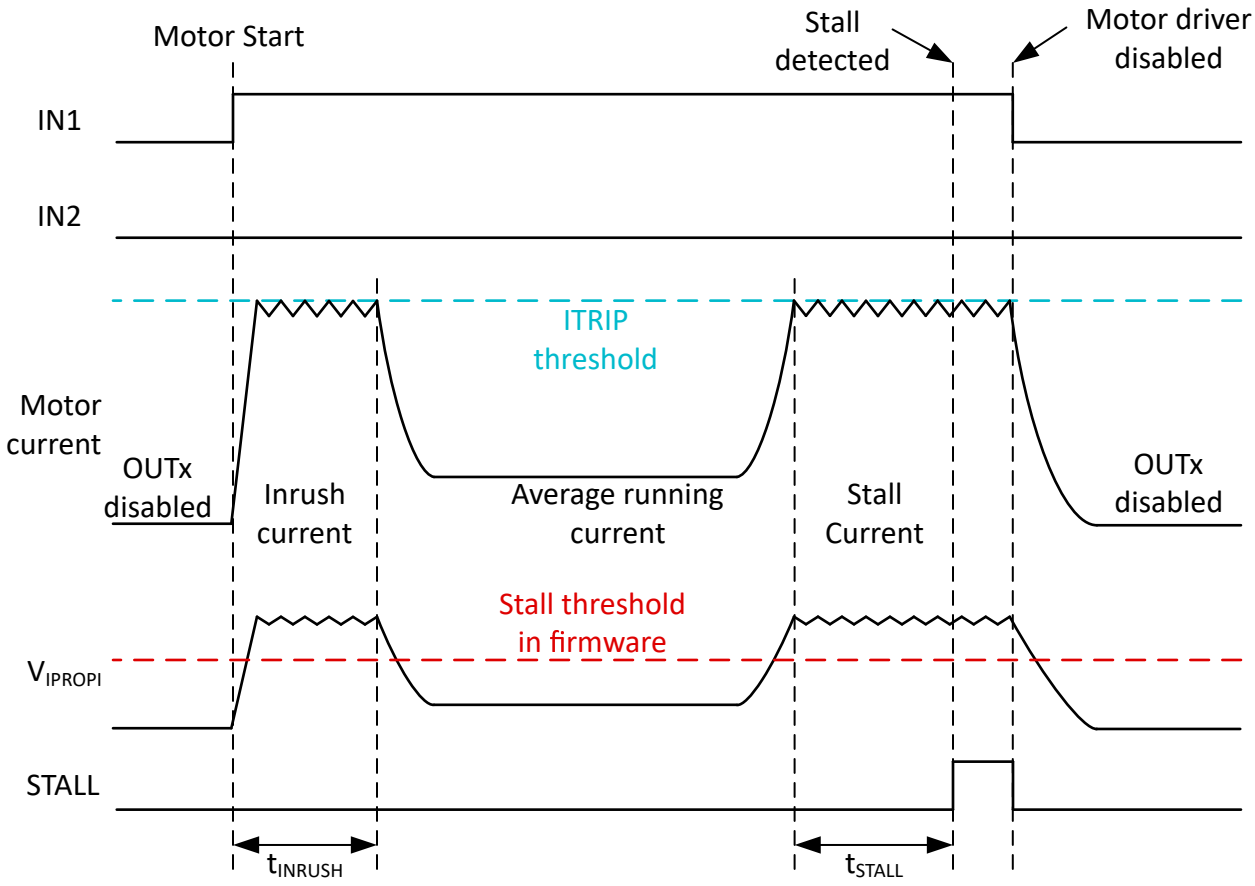


Figure 9-6. Motor Current Profile with STALL Signal

9.2.2.1 Design Requirements

The table below lists the design parameters.

Table 9-2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_M	14.4 V
Motor current trip point	I_{TRIP}	900 mA
VREF voltage	VREF	2 V
IPROPI resistance	R_{IPROPI}	1.5 kΩ
Stall current trip point	I_{STALL}	500 mA
Stall IPROPI voltage trip point	$V_{IPROPI,STALL}$	1 V
Inrush current ignore time	t_{INRUSH}	65 ms
Stall detection time	t_{STALL}	65 ms

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Stall Detection Timing

The microcontroller needs to decide whether or not the IPROPI signal indicates a motor stall. Large inrush current occurs during motor start up because motor speed is low. As the motor accelerates, the motor current drops to an average level because the back electromotive force (EMF) in the motor increases with speed. The inrush current should not be mistaken for a stall condition. One way to do this is for the microcontroller to ignore the IPROPI signal above the firmware stall threshold for the duration of the inrush current, t_{INRUSH}, at startup. The t_{INRUSH} timing should be determined experimentally because it depends on motor parameters, supply voltage, and mechanical load response times.

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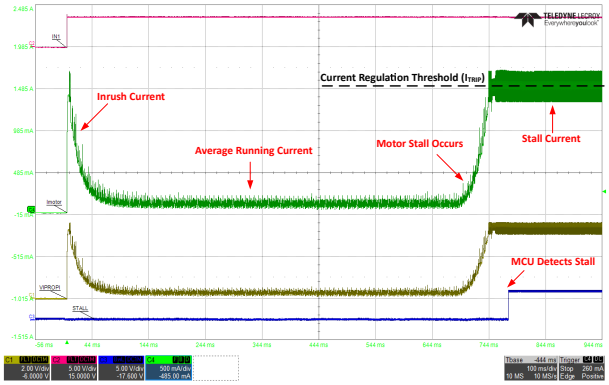
When a stall condition occurs, the motor current will increase from the average running current level because the back EMF is now 0 V. In some cases, it may be desirable to drive at the stall curent for some time in case the motor can clear the blockage on its own. This might be useful for an unintended stall or high-torque condition on the motor. In this case, the system designer can choose a long stall detection time, t_{STALL}, before the microcontroller decides to take action. In other cases, like end-stop detection, a faster response might be desired to reduce power or minimize strong motor torque on the gears or end-stop. This corresponds to setting a shorter t_{STALL} time in the microcontroller.

Figure 9-6 illustrates the t_{INRUSH} and t_{STALL} timings and how they relate to the motor current waveform.

9.2.2.2.2 Stall Threshold Selection

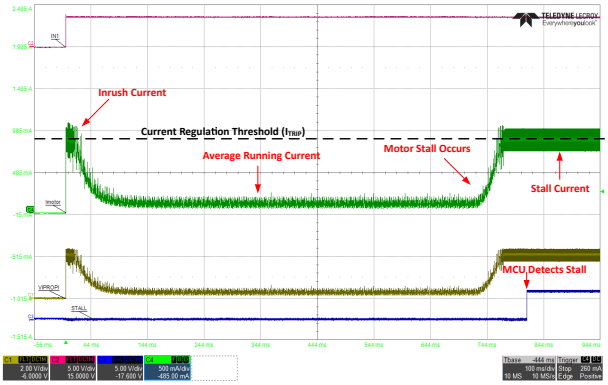
The stall detection threshold in firmware should be chosen at a current level between the maximum stall current and the average running current of the motor as shown in Figure 9-6.

9.2.2.3 Application Curves



Ch 1 (Yellow) = V_{IPROPI} Ch 2 (Magenta) = IN1 Signal
Ch 3 (Blue) = Stall Indication Ch 4 (Green) = Motor Current

Figure 9-7. Example Waveform of Stall Detection



Ch 1 (Yellow) = V_{IPROPI} Ch 2 (Magenta) = IN1 Signal
Ch 3 (Blue) = Stall Indication Ch 4 (Green) = Motor Current

Figure 9-8. Stall Detected on IPROPI While Current Regulation Limits Inrush and Stall Currents

9.2.3 Relay Driving

The PWM interface may also be used to drive single- and dual-coil latching relays, as shown in the figures below.

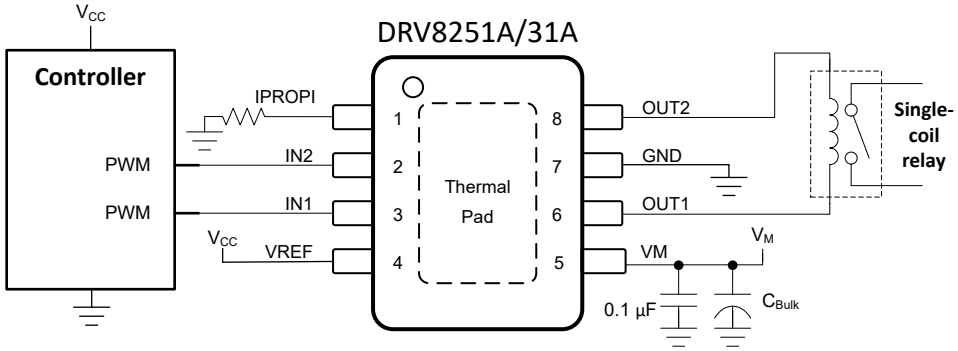


Figure 9-9. Single-Coil Relay Driving

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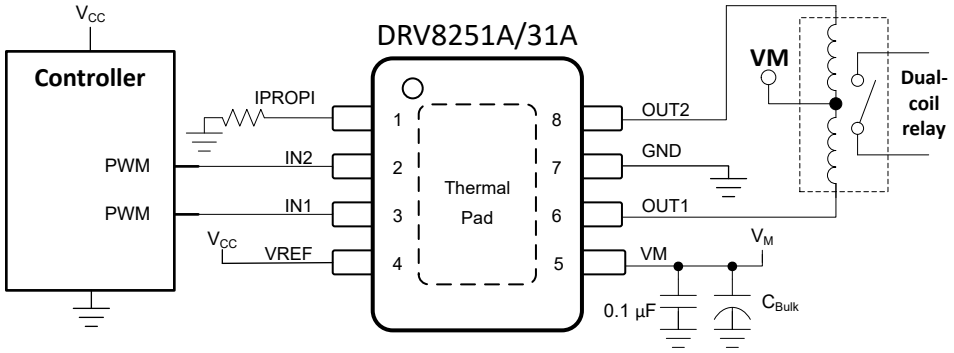


Figure 9-10. Dual-Coil Relay Driving

9.2.3.1 Design Requirements

Table 9-3 provides example requirements for a single- or dual-coil relay application. Current regulation may also be configured to ensure the relay current is within the relay specification. This is important if the VM supply voltage is higher than the voltage rating of the relay.

Table 9-3. System design requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	12 V
Microcontroller supply voltage	V_{CC}	3.3 V
Single coil relay current	I_{Relay}	500 mA pulse for 200 ms
Dual coil relay current	I_{OUT1}, I_{OUT2}	100 mA pulse for 200 ms

9.2.3.2 Detailed Design Procedure

9.2.3.2.1 Control Interface for Single-Coil Relays

The PWM interface can be used to drive single-coil relays. To actuate the relay, the driver needs to drive current with either the forward or reverse states in the PWM table. After driving the relay, the outputs can be disabled (IN1=IN2=0) to put the driver to sleep and save energy. Alternatively, the outputs can be put into brake mode briefly after actuation to avoid back EMF effects from the relay or causing current to flow back from the relay into the VM supply node.

9.2.3.2.2 Control Interface for Dual-Coil Relays

A dual coil relay only require two low-side drivers if the center tap is connected to VM. The body diodes of the unused FETs act as freewheeling diodes, so additional freewheeling diodes are not needed when driving a dual-coil relay with the DRV8251A. The PWM interface can be used to control the dual-coil relay. The following figures show the schematic and timing diagram for driving dual-coil relays.

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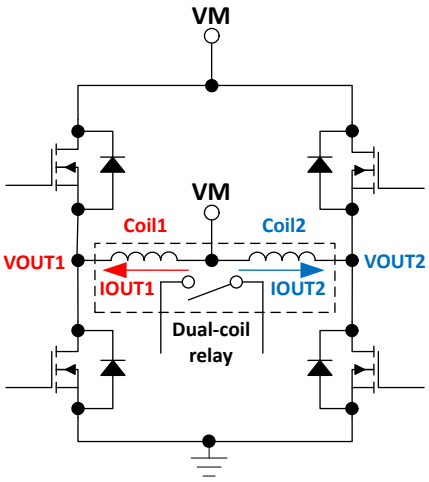


Figure 9-11. Schematic of dual-coil relay driven by the OUTx H-bridge

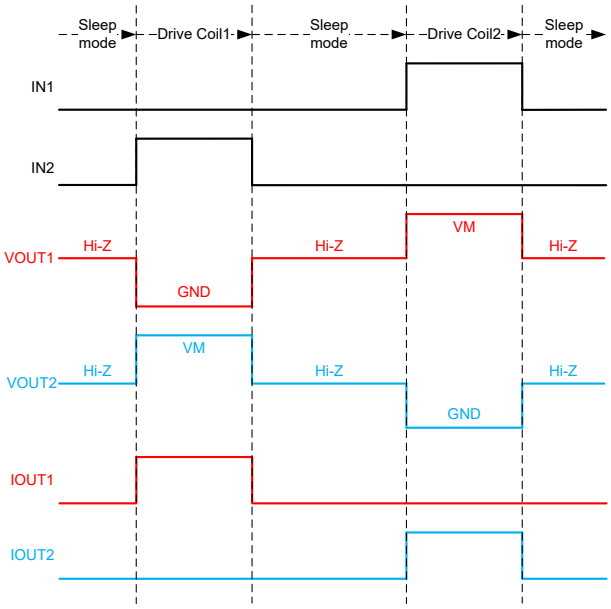


Figure 9-12. Timing diagram for driving a dual-coil relay with PWM interface

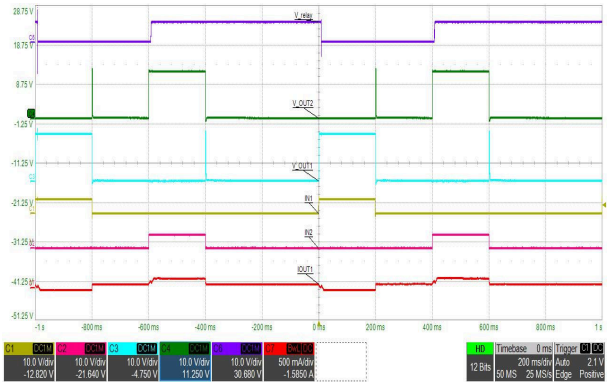
Table 9-4 shows the logic table for the PWM interface. The descriptions in this table reflect how the input and output states drive the dual coil relay. When Coil1 is driven (OUT1 voltage is at GND), The voltage at OUT2 will go to VM. Because the center tap of the relay is also at VM, no current flows through Coil2. The same is true when Coil2 is driven; Coil1 shorts to VM. The body diodes of the high-side FETs act as freewheeling diodes, so extra external diodes are not needed. Figure 9-15 shows oscilloscope traces for this application.

Table 9-4. PWM control table for dual-coil relay driving

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	Hi-Z	Hi-Z	Outputs disabled (H-Bridge Hi-Z)
0	1	L	H	Drive Coil1
1	0	H	L	Drive Coil2
1	1	L	L	Drive Coil1 and Coil2 (invalid state for a dual-coil latching relay)

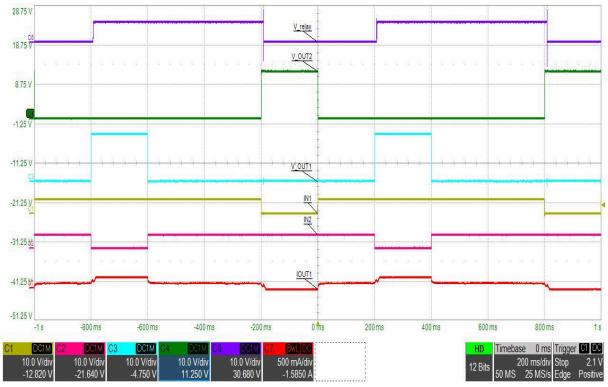
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9.2.3.3 Application Curves



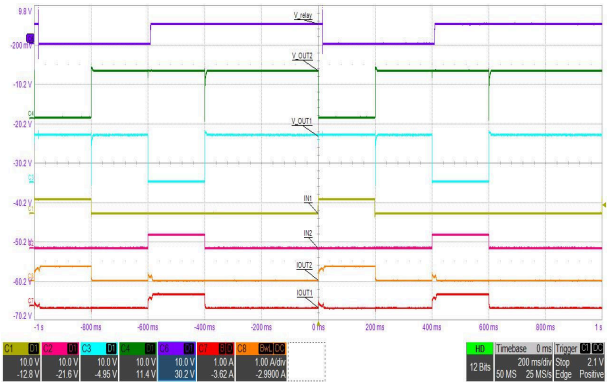
A. Ch 1 = IN1 Ch 2 = IN2 Ch 3 = V_{OUT1} Ch 4 = V_{OUT2} Ch 6 = Relay Switch Ch 7 = Relay Coil Current

Figure 9-13. PWM driving for a single-coil latching relay with driving profile FORWARD → COAST → REVERSE → COAST



A. Ch 1 = IN1 Ch 2 = IN2 Ch 3 = V_{OUT1} Ch 4 = V_{OUT2} Ch 6 = Relay Switch Ch 7 = Relay Coil Current

Figure 9-14. PWM driving for a single-coil latching relay with driving profile FORWARD → BRAKE → REVERSE → BRAKE



A. Ch 1 = IN1 Ch 2 = IN2 Ch 3 = V_{OUT1} Ch 4 = V_{OUT2} Ch 6 = Relay Switch Ch 7 = Relay Coil1 Current Ch 8 = Relay Coil2 Current

Figure 9-15. PWM driving for dual-coil relay

9.2.4 Multi-Sourcing with Standard Motor Driver Pinout

The DRV8870, DRV8251, and DRV8231 devices come in an industry standard package footprint in the DDA package. When the system needs current sensing, a current-sense amplifier may be used across the R_{SENSE} resistor to provide an amplifed signal back to an microcontroller ADC as shown in Figure 9-16. To reduce the size of the system bill of materials and cost, the IPROPI function in DRV8231A/51A can replace the current sense amplifer. During the board design process, both solutions, IPROPI and industry standard shunt devices, can be accomodated in the same board layout by placing and not placing (DNP) components as shown in Figure 9-17. This allows the system to be flexible for lowest cost with the DRV8231A/51A or for use with second-source devices with the same pinout as DRV8870, DRV8231, and DRV8251.

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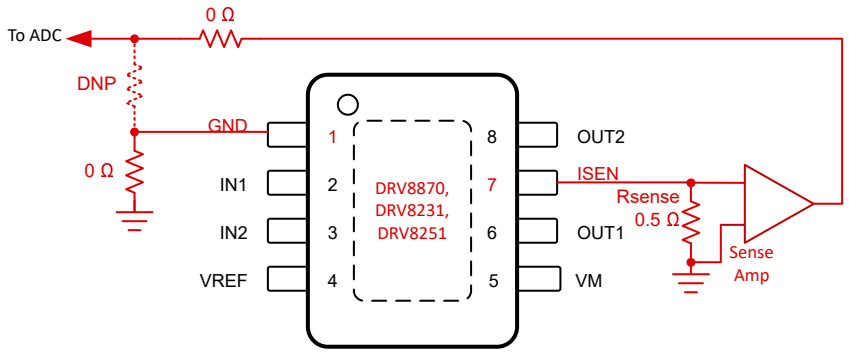


Figure 9-16. Standard Pinout with Current Sense Amplifier

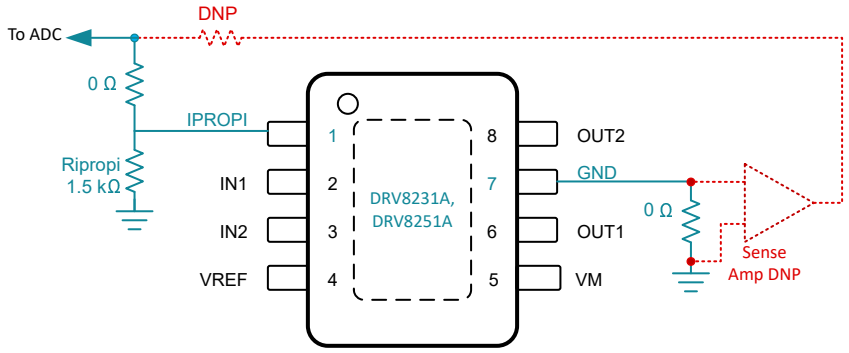


Figure 9-17. DRV8231A/51A Device Using IPROPI to Integrate The Current Sense Function into The Motor Driver

9.3 Current Capability and Thermal Performance

The output current and power dissipation capabilities of the driver depends heavily on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

9.3.1 Power Dissipation and Output Current Capability

Total power dissipation for the device consists of three main components: quiescent supply current dissipation (P_{VM}), the power MOSFET switching losses (P_{SW}), and the power MOSFET $R_{DS(on)}$ (conduction) losses (P_{RDS}). While other factors may contribute additional power losses, they are typically insignificant compared to the three main items.

$$P_{TOT} = P_{VM} + P_{SW} + P_{RDS} \quad (4)$$

P_{VM} can be calculated from the nominal motor supply voltage (V_{VM}) and the I_{VM} active mode current specification.

$$P_{VM} = V_{VM} \times I_{VM} \quad (5)$$

$$P_{VM} = 96\ mW = 24\ V \times 4\ mA \quad (6)$$

P_{SW} can be calculated from the nominal motor supply voltage (V_{VM}), average output current (I_{AVG}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications.

$$P_{SW} = P_{SW_RISE} + P_{SW_FALL} \quad (7)$$

$$P_{SW_RISE} = 0.5 \times V_M \times I_{AVG} \times t_{RISE} \times f_{PWM} \quad (8)$$

$$P_{SW_FALL} = 0.5 \times V_M \times I_{AVG} \times t_{FALL} \times f_{PWM} \quad (9)$$

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$$P_{SW_RISE} = 26.4\ mW = 0.5 \times 24\ V \times 0.5\ A \times 220\ ns \times 20\ kHz \quad (10)$$

$$P_{SW_FALL} = 26.4\ mW = 0.5 \times 24\ V \times 0.5\ A \times 220\ ns \times 20\ kHz \quad (11)$$

$$P_{SW} = 53\ mW = 26.4\ mW + 26.4\ mW \quad (12)$$

P_{RDS} can be calculated from the device $R_{DS(on)}$ and average output current (I_{AVG}).

$$P_{RDS} = I_{AVG}^{2} \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (13)$$

$R_{DS(ON)}$ has a strong correlation with the device temperature. Assuming a device junction temperature of 85 °C, $R_{DS(on)}$ could increase ~1.5x based on the normalized temperature data. The calculation below shows this derating factor. Alternatively, Section 7.6 shows curves that plot how $R_{DS(on)}$ changes with temperature.

$$P_{RDS} = 169\ mW = (0.5\ A)^2 \times (225\ m\Omega \times 1.5 + 225\ m\Omega \times 1.5) \quad (14)$$

Based on the example calculations above, the expressions below calculate the total expected power dissipation for the device.

$$P_{TOT} = P_{VM} + P_{SW} + P_{RDS} \quad (15)$$

$$P_{TOT} = 318\ mW = 96\ mW + 53\ mW + 169\ mW \quad (16)$$

The driver's junction temperature can be estimated using P_{TOT}, device ambient temperature (T_A), and package thermal resistance ($R_{\theta JA}$). The value for $R_{\theta JA}$ depends heavily on the PCB design and copper heat sinking around the device. Section 9.3.2 describes this dependence in greater detail.

$$T_J = (P_{TOT} \times R_{\theta JA}) + T_A \quad (17)$$

$$T_J = 98\ °C = (0.318\ W \times 40.4\ °C/W) + 85°C \quad (18)$$

The device junction temperature should remain below its absolute maximum rating for all system operating conditions. The calculations in this section provide reasonable estimates for junction temperature. However, other methods based on temperature measurements taken during system operation are more realistic and reliable. Additional information on motor driver current ratings and power dissipation can be found in Section 9.3.2 and Section 12.1.1.

9.3.2 Thermal Performance

The datasheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance may be better or worse than this value depending on PCB stackup, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current will also impact power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section was simulated using the following criteria.

Table 9-5. Simulation PCB Stackup Summary for HSOP package

Layer	2-layer	4-layer
Top Layer	HSOP footprint with 1- or 2-oz copper thickness. See Table 9-6 for copper area varied in simulation. Thermally connected with vias (2 vias, 1.2-mm spacing, 0.3-mm diameter, 0.025-mm copper plating) from HSOP thermal pad to bottom layer and internal ground plane (4-layer only).	
Layer 2, internal ground plane	N/A	1-oz copper thickness, 74.2 mm x 74.2 mm copper area, thermally connected to HSOP thermal pad through vias.
Layer 3, internal supply plane	N/A	1-oz copper thickness, 74.2 mm x 74.2 mm copper area, not connected to other layers.

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Table 9-5. Simulation PCB Stackup Summary for HSOP package (continued)

Layer	2-layer	4-layer
Bottom Layer	Ground plane with 1- or 2-oz copper thickness. See Table 9-6 for copper area varied in simulation. Thermally connected to HSOP thermal pad through vias.	1- or 2-oz copper thickness. Copper area fixed at 4.90 mm × 6.00 mm in simulation. Thermally connected to HSOP thermal pad through vias.

Figure 9-18 shows an example of the simulated board for the HSOP package. Table 9-6 shows the dimensions of the board that were varied for each simulation.

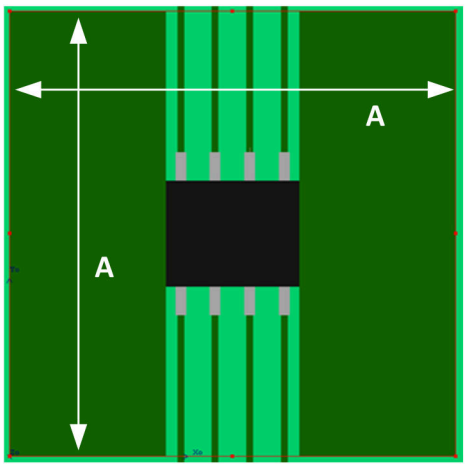


Figure 9-18. HSOP PCB model top layer

Table 9-6. Dimension A for 8-pin HSOP (DDA) package

Cu area (cm^2)	Dimension A (mm)
0.069	Package thermal pad dimensions
2	16.40
4	22.32
8	30.64
16	42.38

9.3.2.1 Steady-State Thermal Performance

"Steady-state" conditions assume that the motor driver operates with a constant average current over a long period of time. The figures in this section show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB}, which indicate better thermal performance from the PCB layout.

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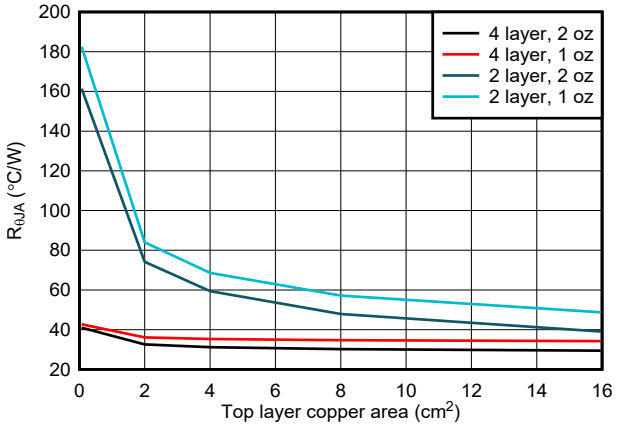


Figure 9-19. HSOP, PCB junction-to-ambient thermal resistance vs copper area

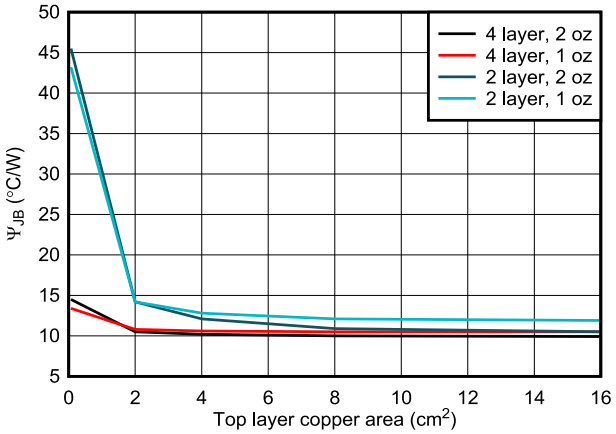


Figure 9-20. HSOP, junction-to-board characterization parameter vs copper area

9.3.2.2 Transient Thermal Performance

The motor driver may experience different transient driving conditions that cause large currents to flow for a short duration of time. These may include

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance in addition to copper area and thickness. In transient cases, the thermal impedance parameter $Z_{\theta JA}$ denotes the junction-to-ambient thermal performance. The figures in this section show the simulated thermal impedances for 1-oz and 2-oz copper layouts for the HSOP package. These graphs indicate better thermal performance with short current pulses. For short periods of drive time, the device die size and package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and copper area as the duration of the drive pulse duration increases. Long pulses can be considered steady-state performance.

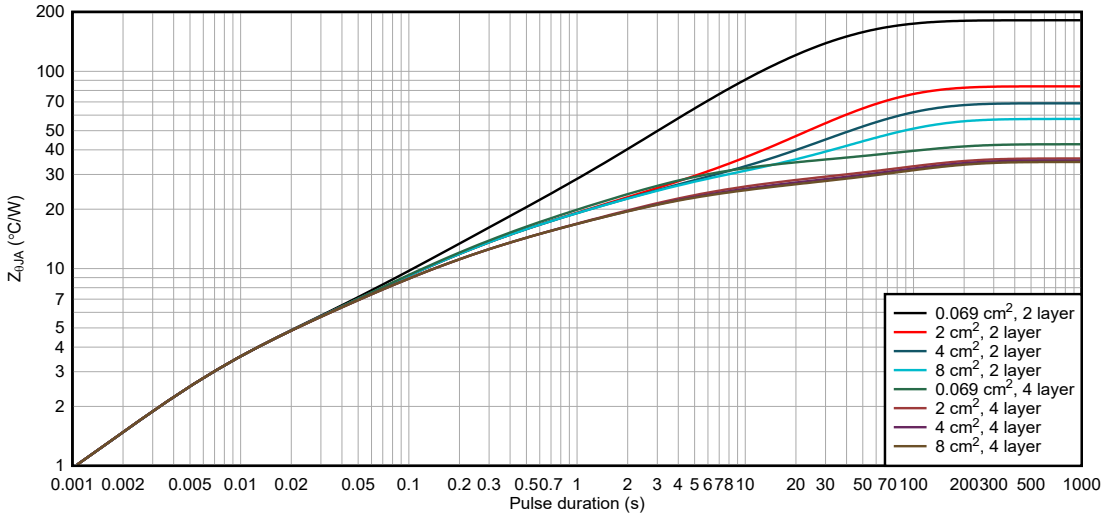


Figure 9-21. HSOP package junction-to-ambient thermal impedance for 1-oz copper layouts

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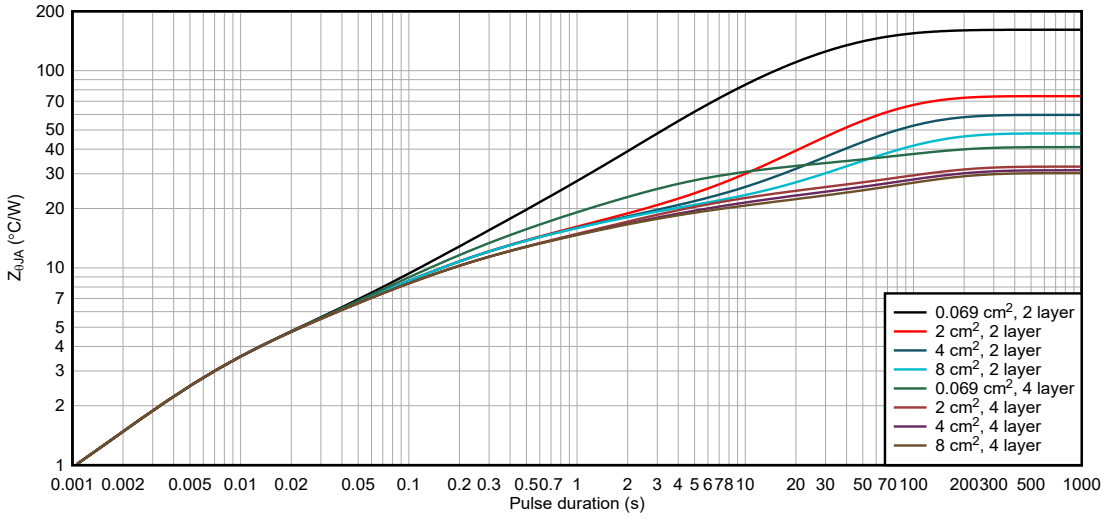


Figure 9-22. HSOP package junction-to-ambient thermal impedance for 2-oz copper layouts

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10 Power Supply Recommendations

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

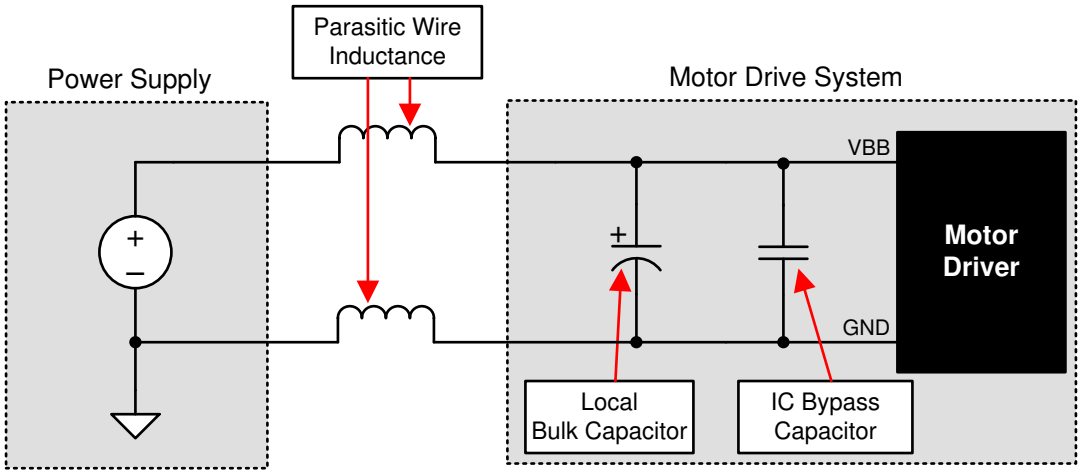


Figure 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

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11 Layout

11.1 Layout Guidelines

Since the DRV8251A integrates power MOSFETs capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below.

- Low ESR ceramic capacitors should be utilized for the VM to GND bypass capacitor. X5R and X7R types are recommended.
- The VM power supply capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and GND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- A recommended land pattern for the thermal vias is provided in the package drawing section.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

11.2 Layout Example

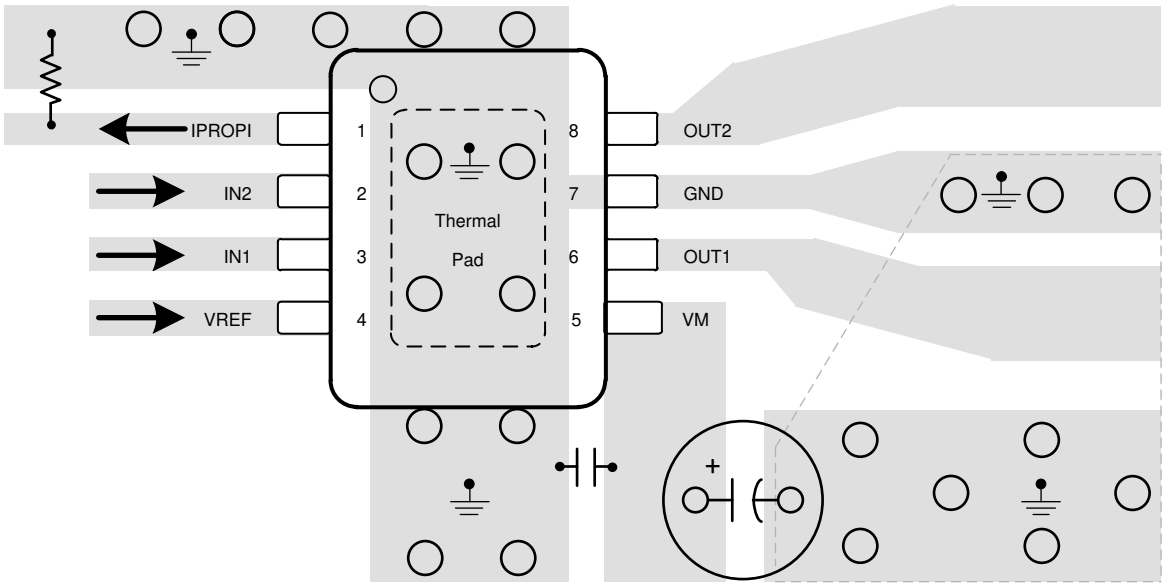


Figure 11-1. Layout Recommendation for DDA Package

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

12.4 Trademarks

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8251ADDAR	ACTIVE	SO PowerPAD	DDA	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV 8251A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

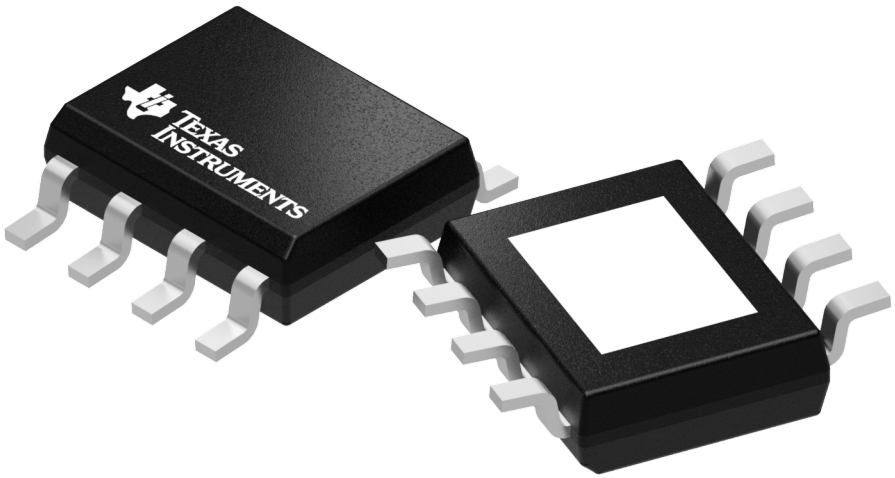
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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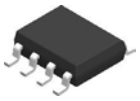
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DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

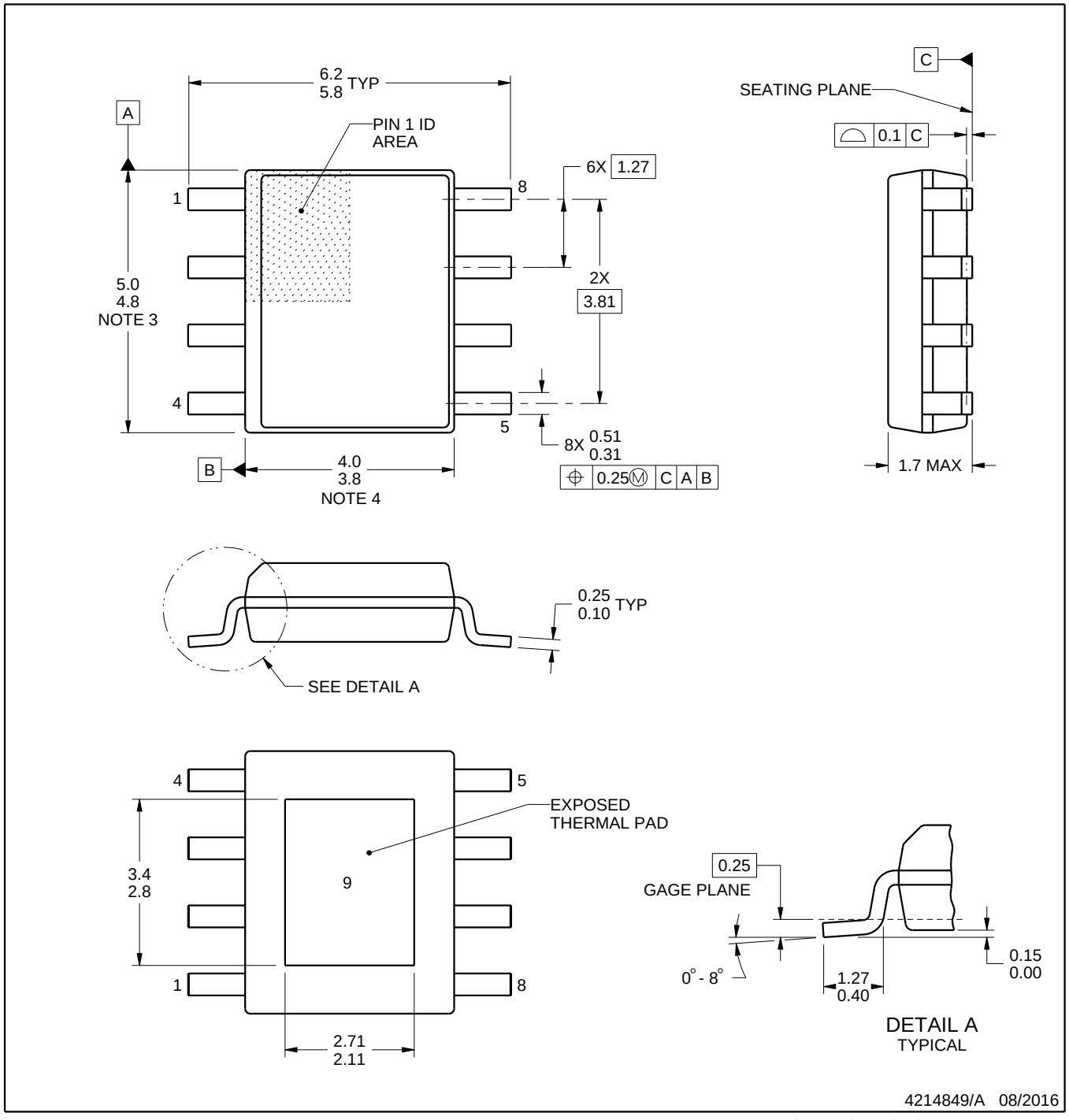


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

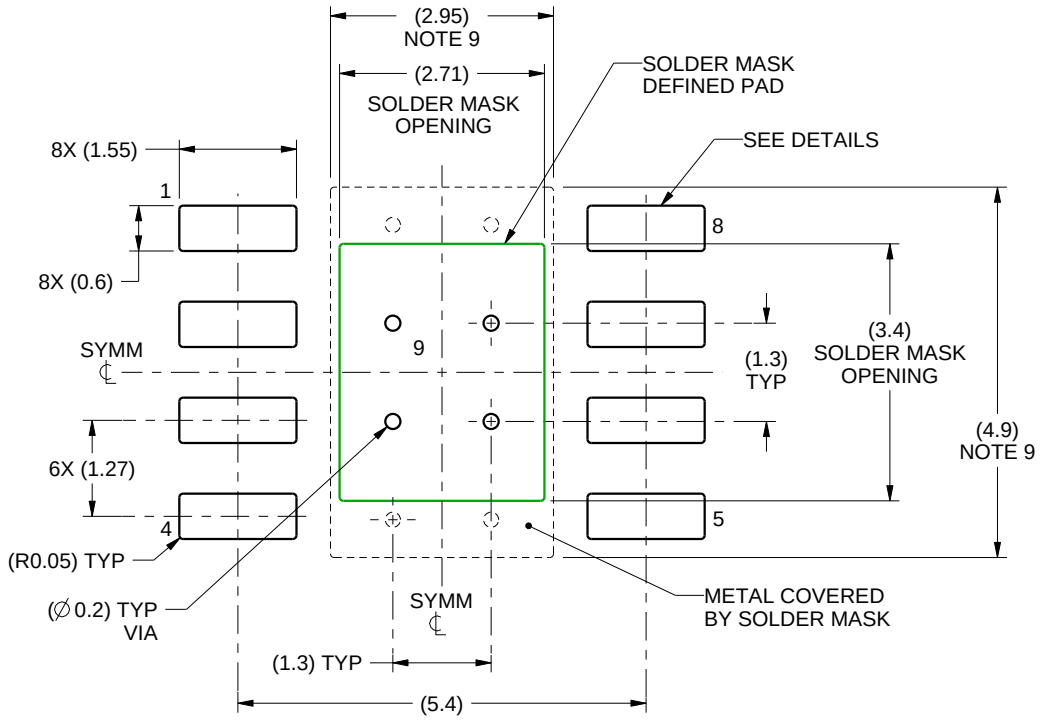
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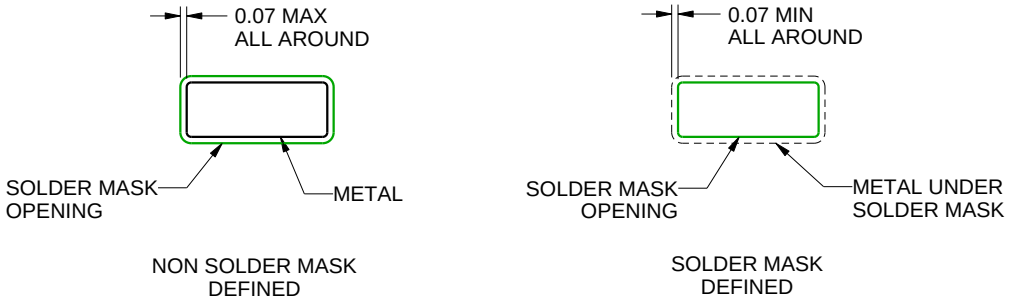
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

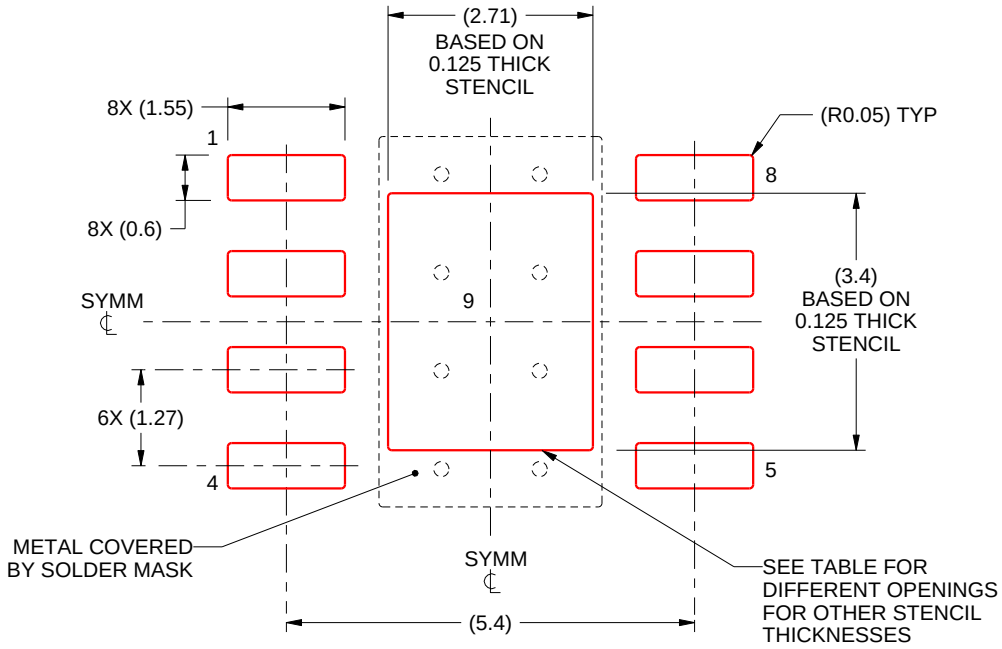
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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