Ultra-Low Power Adjustable Supervisor with Power-Fail Output

FEATURES

- **500nA Quiescent Current**
- **±1.5% (Max) Accuracy over Temperature**
- **Operates Down to 1.6V Supply**
- **Adjustable Reset Threshold**
- **Adjustable Power-Fail Threshold**
- Early Warning Power-Fail Output
- Selectable 15ms or 200ms Reset Timeout
- Manual Reset Input
- Compact 8-Lead, 2mm × 2mm DFN and TSOT-23 (ThinSOT™) Packages

APPLICATIONS

- Portable Equipment
- Battery-Powered Equipment
- Security Systems
- Point-of-Sale Devices
- Wireless Systems

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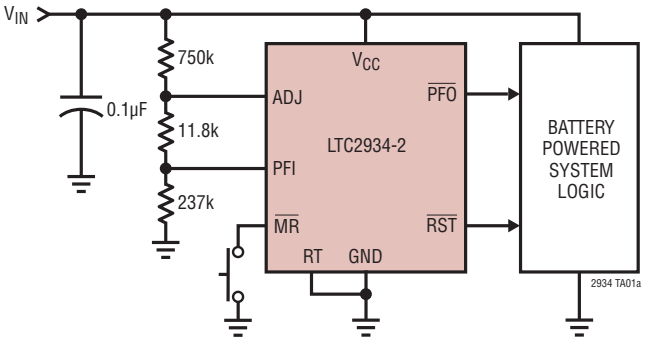
DESCRIPTION

The LTC®2934 ultra-low power voltage monitor provides system initialization, power-fail warning and reset generation functions. Low quiescent current (500nA typical) makes the LTC2934 an ideal choice for battery-operated applications.

Precision power-fail and reset voltages can be configured independently. Early warning of an impending low voltage condition is provided at the power-fail output ($\overline{PFO}$) when the PFI input falls below 0.4V. Supervisory circuits monitor the ADJ input and pull $\overline{RST}$ low when ADJ falls below 0.4V. When ADJ is rising from an under-threshold condition, an internal reset timer is started after exceeding the ADJ threshold by 5%. The reset timeout delays the return of the $\overline{RST}$ output to a high state. A pushbutton switch connected to the $\overline{MR}$ input is typically used to force a manual reset. Outputs $\overline{RST}$ and $\overline{PFO}$ are available with open-drain (LTC2934-1) or active pull-up circuits (LTC2934-2). Operating temperature range is from –40°C to 85°C.

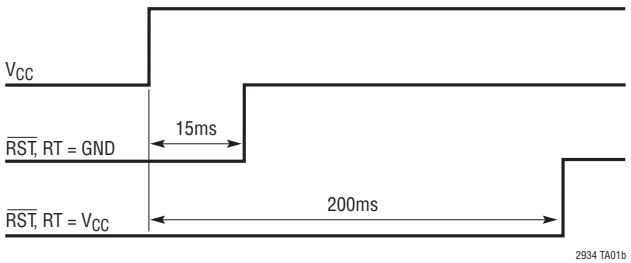
TYPICAL APPLICATION

Configurable Low Power Voltage Supervisor



POWER FAIL FALLING THRESHOLD = 1.686V
RESET FALLING THRESHOLD = 1.606V

Selectable Reset Timeout Period



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltages
- V_{CC} ..... –0.3V to 6V
- ADJ, PFI ..... –0.3V to 6V
- RT, $\overline{MR}$ ..... –0.3V to (V_{CC} + 0.3V)

Output Voltages
- $\overline{PFO}$, $\overline{RST}$ (LTC2934-1) ..... –0.3V to 6V
- $\overline{PFO}$, $\overline{RST}$ (LTC2934-2) ..... –0.3V to (V_{CC} + 0.3V)

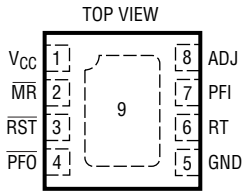
RMS Currents
- $\overline{PFO}$, $\overline{RST}$ ..... ±5mA

Operating Ambient Temperature Range
- LTC2934C ..... 0°C to 70°C
- LTC2934I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

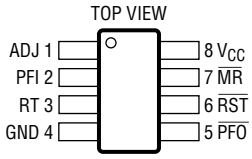
Lead Temperature (Soldering, 10 sec)
- TSOT-23 Package ..... 300°C

PIN CONFIGURATION



DC PACKAGE
8-LEAD (2mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 102°C/W
EXPOSED PAD (PIN 9) PCB GND CONNECTION OPTIONAL



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 125°C, θ_{JA} = 195°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2934CTS8-1#TRMPBF	LTC2934CTS8-1#TRPBF	LTDKR	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2934ITS8-1#TRMPBF	LTC2934ITS8-1#TRPBF	LTDKR	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2934CTS8-2#TRMPBF	LTC2934CTS8-2#TRPBF	LTDKS	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2934ITS8-2#TRMPBF	LTC2934ITS8-2#TRPBF	LTDKS	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2934CDC-1#TRMPBF	LTC2934CDC-1#TRPBF	LDKT	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2934IDC-1#TRMPBF	LTC2934IDC-1#TRPBF	LDKT	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2934CDC-2#TRMPBF	LTC2934CDC-2#TRPBF	LDKV	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2934IDC-2#TRMPBF	LTC2934IDC-2#TRPBF	LDKV	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.6V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Input Supply Voltage		●	1.6		5.5	V
I_{CC}	V_{CC} Input Supply Current		●	225	500	1000	nA
Threshold Adjustment Inputs: ADJ, PFI							
V_{TH}	Input Threshold (Monitored Voltage Falling)		●	394	400	406	mV
V_{THM}	ADJ to PFI Threshold Matching		●		±2	±8	mV
$V_{ADJ(HYST)}$	Reset Threshold Hysteresis (Monitored Voltage Rising)		●	18	20	25	mV
$V_{PFI(HYST)}$	Power-Fail Threshold Hysteresis (Monitored Voltage Rising)		●	8	10	15	mV
t_{UV}	Undervoltage Detect to $\overline{RST}$ or $\overline{PFO}$ Falling	V_{ADJ} or V_{PFI} = V_{TH} – 4mV (Note 3)			1		ms
$I_{TH(LKG)}$	Threshold Adjustment Input Leakage Current	V_{ADJ} or V_{PFI} = 420mV	●		0.1	±1	nA
Control Inputs: $\overline{MR}$, RT							
$V_{IN(TH)}$	Control Input Threshold	RT $\overline{MR}$	● ●	0.3 • V_{CC} 0.4		0.7 • V_{CC} 1.4	V V
t_{PW}	Input Pulse Width	$\overline{MR}$	●	20			µs
t_{PD}	Propagation Delay to $\overline{RST}$ Falling	Manual Reset Falling	●	2	5	20	µs
R_{PU}	Internal Pull-Up Resistance	$\overline{MR}$	●	600	900	1200	kΩ
I_{LK}	Input Leakage Current (RT Input)	RT = V_{CC} or GND	●		±1	±10	nA
Reset and Power Fail Outputs: $\overline{RST}$, $\overline{PFO}$							
V_{OL}	Voltage Output Low	V_{CC} = 1V, 200µA Pull-Up Current V_{CC} = 3V, 3mA Pull-Up Current	● ●		25 50	100 150	mV mV
V_{OH}	Voltage Output High (LTC2934-2)	–200µA Pull-Down Current	●	0.7 • V_{CC}			V
I_{OH}	Leakage Current, Output High (LTC2934-1)	$V_{\overline{RST}}$, $V_{\overline{PFO}}$ = 3.6V	●		±1	±10	nA
t_{RST}	Reset Timeout Period	RT Input High RT Input Low	● ●	140 10	200 15	260 25	ms ms

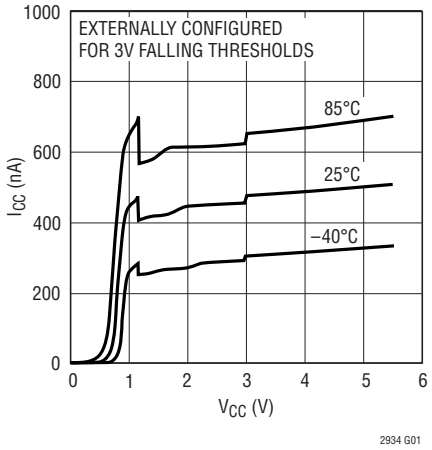
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

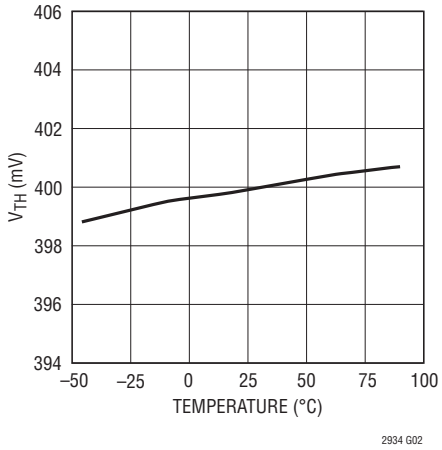
Note 3. Guaranteed by design. Characterized, but not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

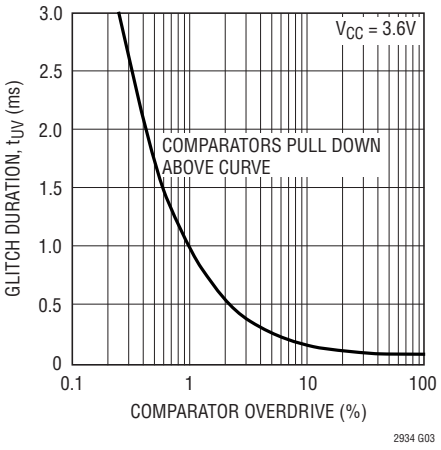
Supply Current vs Supply Voltage



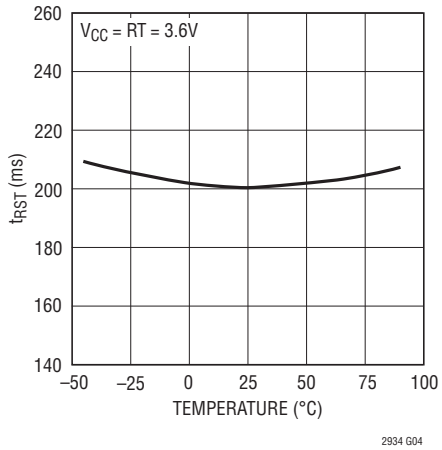
ADJ, PFI Threshold vs Temperature



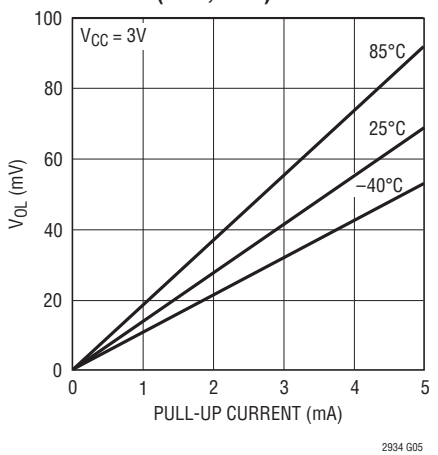
Comparator Undervoltage Glitch Immunity



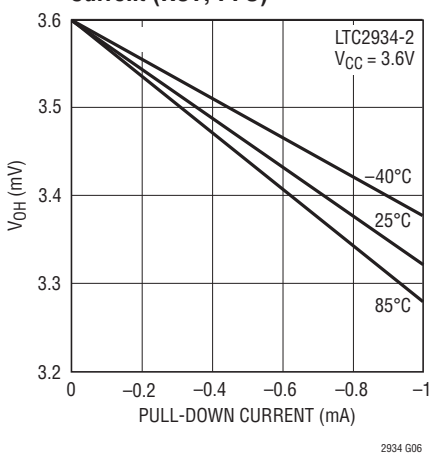
Reset Timeout Period vs Temperature



Voltage Output Low vs Pull-Up Current ($\overline{RST}$, $\overline{PFO}$)

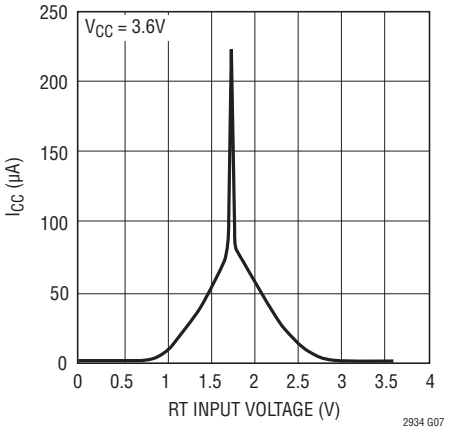


Voltage Output High vs Pull-Down Current ($\overline{RST}$, $\overline{PFO}$)

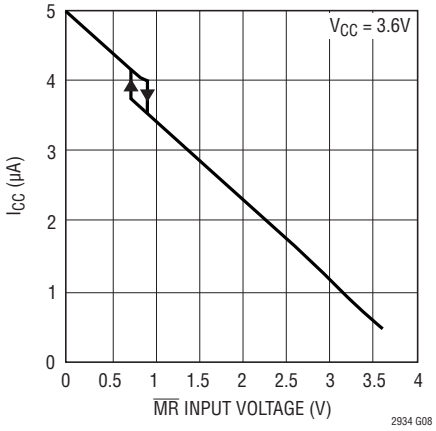


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Supply Current vs RT Input Voltage



Supply Current vs $\overline{MR}$ Input Voltage



PIN FUNCTIONS

ADJ: Reset Threshold Adjustment Input. Tie to resistive divider between monitored voltage and GND to configure desired reset threshold. See the Applications Information section for details. Tie to V_{CC} if unused.

Exposed Pad (DFN Only): Exposed Pad may be left floating or connected to device ground.

GND: Device Ground.

$\overline{MR}$: Manual Reset Input. Attach a push-button switch between this input and ground. A logic low on this input pulls $\overline{RST}$ low. When the $\overline{MR}$ input returns to logic high, $\overline{RST}$ returns high after the reset timer has expired. Tie to V_{CC} if unused.

PFI: Power-Fail Threshold Adjustment Input. Tie to resistive divider between monitored voltage and GND to configure desired power-fail threshold. See the Applications Information section for details. Tie to V_{CC} or GND if unused.

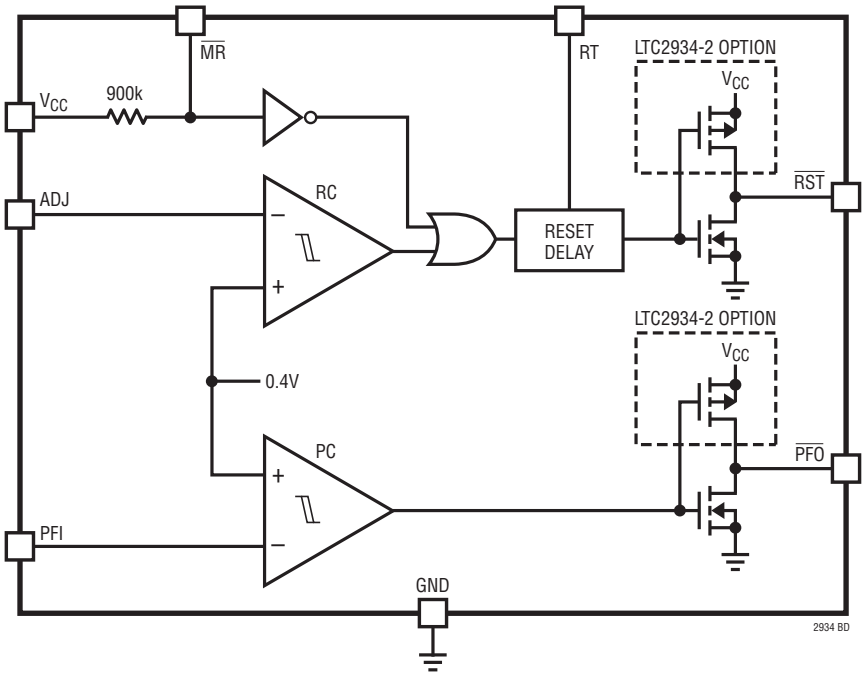
$\overline{PFO}$: Power-Fail Output. $\overline{PFO}$ pulls low when monitored voltage falls below the power-fail (PFI) threshold. $\overline{PFO}$ is released when the PFI voltage rises above the power-fail threshold by 2.5%. $\overline{PFO}$ is available with open-drain (LTC2934-1) or active pull-up (LTC2934-2) outputs. Leave open if unused.

$\overline{RST}$: Reset Output. $\overline{RST}$ pulls low when monitored voltage falls below the reset threshold. $\overline{RST}$ is released after monitored voltage exceeds the reset threshold plus 5% hysteresis and after reset timer has expired. $\overline{RST}$ is available with open-drain (LTC2934-1) or active pull-up (LTC2934-2) outputs. Leave open if unused.

RT: Reset Timeout Selection Input. Tie to GND or V_{CC} for desired reset timeout. Tie low for 15ms delay or high for 200ms delay.

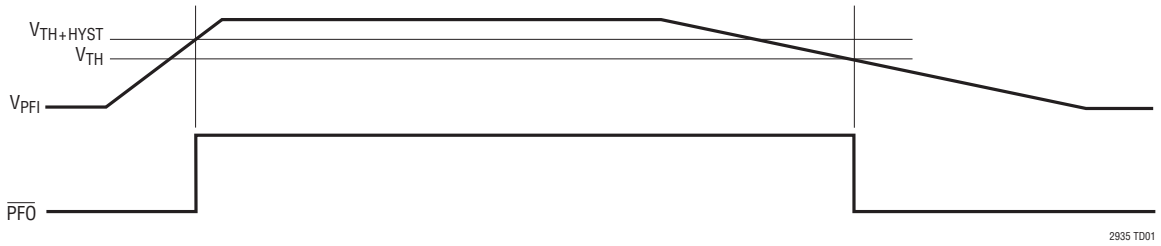
V_{CC}: Power Supply Input. Bypass V_{CC} with 0.1µF to GND.

BLOCK DIAGRAM

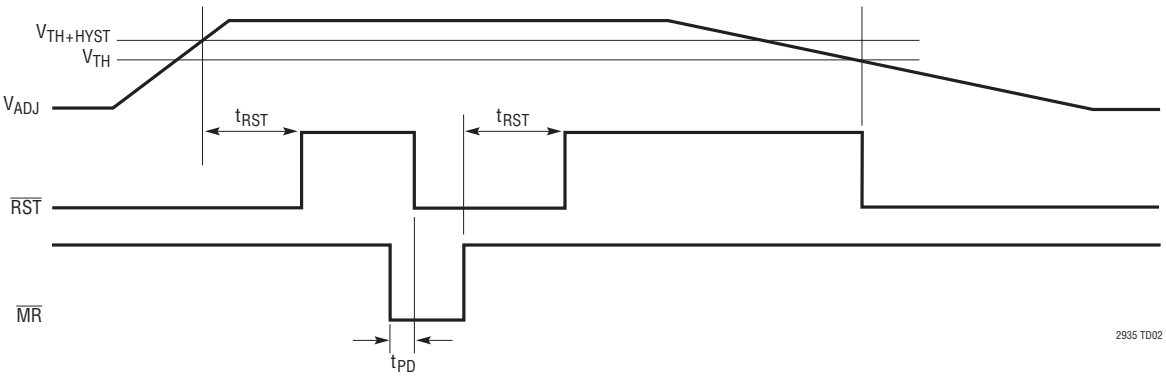


TIMING DIAGRAM

PFI / $\overline{\text{PFO}}$ Timing



ADJ / $\overline{\text{RST}}$ Timing



APPLICATIONS INFORMATION

VOLTAGE MONITORING

Unmanaged power can cause various system problems. At power-up, voltage fluctuation around critical thresholds can cause improper system or processor initialization. The LTC2934 provides power management capabilities for the system power-up phase. The supervisory device issues a system reset after the monitored voltage has stabilized. Built-in hysteresis and filtering ensures that fluctuations due to load transients or supply noise do not cause chattering of the status outputs. Comparator undervoltage glitch immunity is shown in the Typical Performance Characteristics section. The curve demonstrates the transient amplitude and width required to switch the comparators.

Because many batteries exhibit large series resistance, load currents can cause significant voltage drops. The low DC current draw of the LTC2934 (at any input voltage) does not add to the loading problem. When voltage is initially applied to V_{CC}, $\overline{RST}$ and $\overline{PFO}$ pull low once there is enough voltage to turn on the pull-down devices (1V maximum).

If the monitored supply voltage falls to the power-fail threshold, the built-in power-fail comparator pulls $\overline{PFO}$ low. $\overline{PFO}$ remains low until the PFI input rises above 0.4V plus 2.5% hysteresis. $\overline{PFO}$ is typically used to signal preparation for controlled shutdown. For example, the $\overline{PFO}$ output may be connected to a processor nonmaskable interrupt. Upon interrupt, the processor begins shutdown procedures such as supply sequencing and/or storage/erasure of system state in nonvolatile memory.

If the monitored voltage drops below the reset threshold, $\overline{RST}$ pulls low until the ADJ input rises above 0.4V plus 5% hysteresis. This may occur through battery charging or replacement. An internal reset timer delays the return of the $\overline{RST}$ output to a high state to provide settling and initialization time. The $\overline{RST}$ output is typically connected to processor reset input.

Few, if any external components are necessary for reliable operation. However, a decoupling capacitor between V_{CC} and ground is recommended (0.01µF minimum).

Threshold Configuration

The LTC2934 monitors voltage applied to its inputs PFI and ADJ. A resistive divider connected between a monitored voltage and ground is used to bias the inputs. Figure 1 demonstrates how the monitor inputs can be made dependent upon a single voltage (V1). Only three resistors are required. To calculate their values, specify desired falling power fail (V_{PF}) and reset voltages (V_R) with $V_{PF} > V_R$. For example:

V_{PF} = 1.72V, V_R = 1.62V

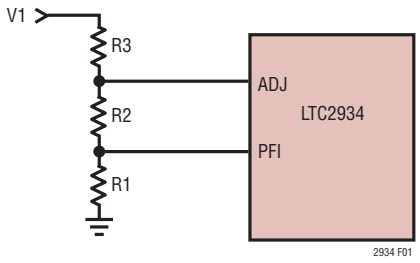


Figure 1. Configuration for Single Voltage Monitoring

The solution for R1, R2, and R3 provides three equations and three unknowns. Maximum resistor size is governed by maximum input leakage current. For the LTC2934, the maximum input leakage current over temperature is 1nA. For a maximum error of 1% due to both input currents, the resistor divider current should be 100 times the sum of the leakage currents, or 0.2µA. At the reset threshold, V1 = 1.62V, so R_{SUM} = V1/0.2µA = 8.1M where:

$R_{SUM} = R1 + R2 + R3$

The falling monitor thresholds (V_{TH}) are 0.4 volts, so:

$$R1 = \frac{V_{TH} \bullet R_{SUM}}{V_{PF}} = \frac{0.4V \bullet 8.1M}{1.72V} = 1.88M$$

The closest 1% value is 1.87M. R2 can be determined from:

$$R2 = \frac{V_{TH} \bullet R_{SUM}}{V_R} - R1 = \frac{0.4V \bullet 8.1M}{1.62V} - 1.87M$$

$R2 = 130k$

APPLICATIONS INFORMATION

R3 is easily obtained from:

$$R3 = R_{SUM} - R1 - R2 = 8.1M - 1.87M - 130k = 6.1M$$

The closest 1% value is 6.04M. Plugging the standard values back into the equations yields the design values for the falling power-fail and reset voltages:

$$V_{PF} = 1.720V,\ V_R = 1.608V$$

Figure 2 demonstrates how the inputs can be biased to monitor two voltages (V1, V2). In this example, four resistors are required. Calculate each divider ratio for the desired falling threshold (V_{FT}) using:

$$\frac{RnB}{RnA} = \frac{V_{FT}}{V_{TH}} - 1 = \frac{V_{FT}}{0.4V} - 1$$

In Figure 2, $\overline{PFO}$ is tied back to the $\overline{MR}$ input, making the state of the $\overline{RST}$ output dependent upon both V1 and V2. If V1 and V2 are both above the configured falling threshold plus hysteresis, $\overline{RST}$ is allowed to pull high. If independent operation of the status outputs is desired, simply omit the $\overline{PFO}$ to $\overline{MR}$ connection.

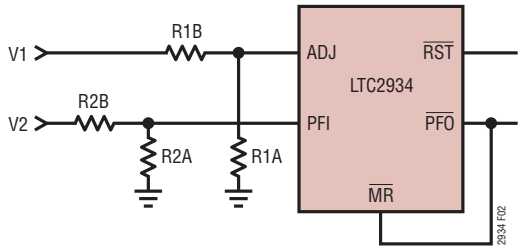


Figure 2. Dual Voltage Monitoring

Selecting Output Logic Style

The LTC2934 status outputs are available in two options: open-drain (LTC2934-1) or active pull-up (LTC2934-2). The open-drain option (LTC2934-1) allows the outputs to be pulled up to a user defined voltage with a resistor. The open-drain pull-up voltage may be greater than V_{CC} (5.5V maximum), which is not always possible with inferior battery supervisors, due to internal diode clamps. When the status outputs are low, power is dissipated in the pull-up resistors. Recommended resistor values lie in the range between 10k and 470k. Figure 3 demonstrates typical LTC2934-1 $\overline{RST}$ output behavior.

The active pull-up option (LTC2934-2) eliminates the need for external pull-up resistors on the status outputs. Integrated pull-up devices pull the outputs up to V_{CC}. Actively pulled up outputs may not be driven above V_{CC}.

Some applications require the $\overline{RST}$ and/or $\overline{PFO}$ outputs to be valid with V_{CC} down to ground. Active pull-up handles this requirement with the addition of an external resistor from the output to ground. The resistor provides a path for leakage currents, preventing the output from floating to undetermined voltages when connected to high impedance (such as CMOS logic inputs). The resistor value should be small enough to provide effective pull-down without excessively loading the pull-up circuitry. A 100k resistor from output to ground is satisfactory for most applications. When the status outputs are high, power is dissipated in the pull-down resistors. Figure 4 demonstrates typical LTC2934-2 $\overline{RST}$ output behavior.

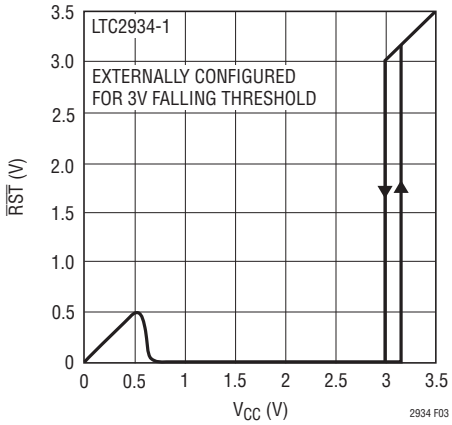


Figure 3. $\overline{RST}$ vs V_{CC} with 10k Pull-Up

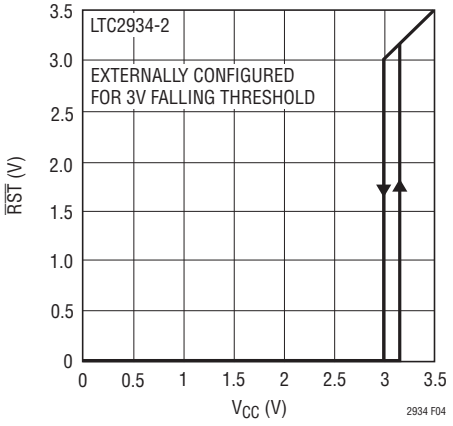


Figure 4. $\overline{RST}$ vs V_{CC}

APPLICATIONS INFORMATION

Manual Reset Input

When V_{CC} is above its reset threshold, and the manual reset input ($\overline{MR}$) is pulled low, the $\overline{RST}$ output is forced low. $\overline{RST}$ remains low for the selected reset timeout period after the manual reset input is released and pulled high. The manual reset input is pulled up internally through 900k to V_{CC}. If external leakage currents have the ability to pull down the manual reset input below its logic threshold, a lower value pull-up resistor, placed between V_{CC} and $\overline{MR}$ will fix the problem.

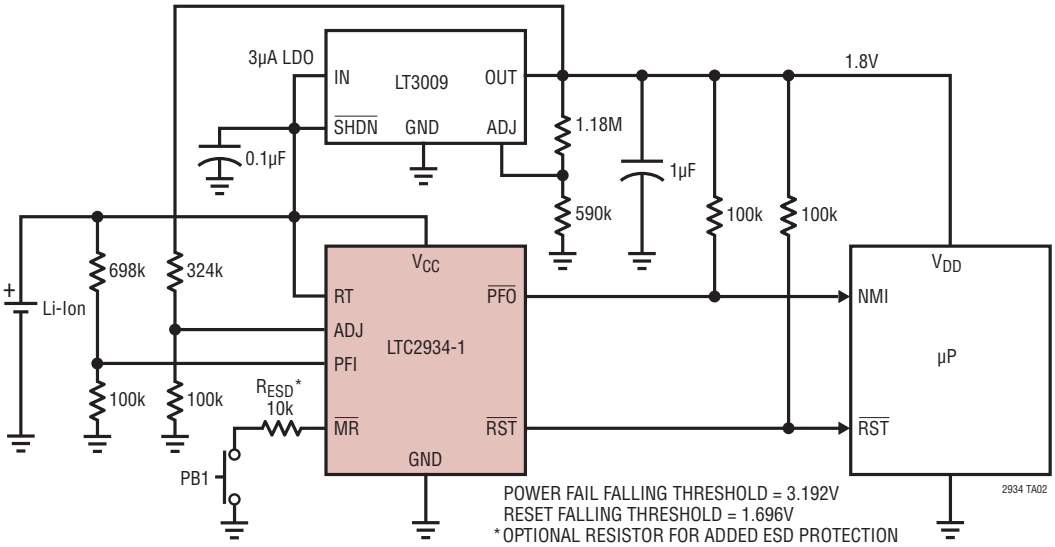
Input $\overline{MR}$ is often pulled down through a pushbutton switch requiring human contact. If extended ESD tolerance is required, series resistance between the switch and the input is recommended. For most applications a 10k resistor provides sufficient current limiting.

Selecting the Reset Timeout Period

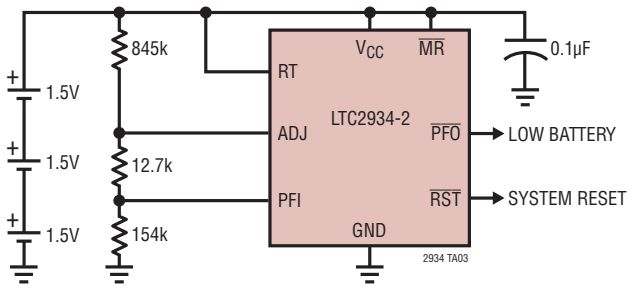
Use the RT input to select between two fixed reset timeout periods. Connect RT to ground for a 15ms timeout. Connect RT to V_{CC} for a 200ms timeout. The reset timeout period occurs after the ADJ input is driven above threshold. After the reset timeout period, the $\overline{RST}$ output is allowed to pull up to a high state.

TYPICAL APPLICATIONS

Battery Monitor with Interface to Low Voltage Logic

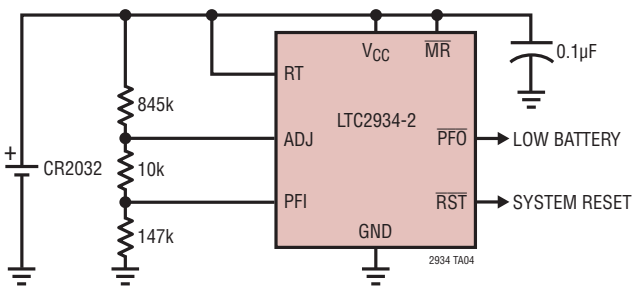


Alkaline Cell Stack Voltage Monitor



POWER FAIL THRESHOLD = 2.628V
RESET THRESHOLD = 2.428V

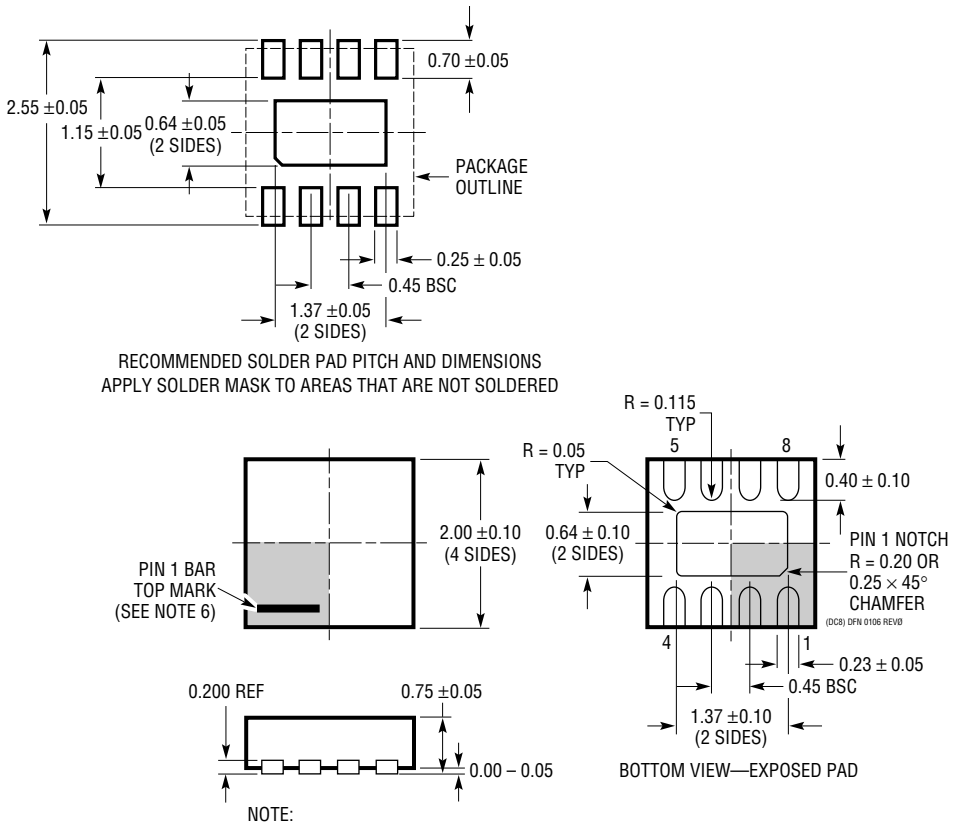
Coin Cell Voltage Monitor



POWER FAIL THRESHOLD = 2.727V
RESET THRESHOLD = 2.553V

PACKAGE DESCRIPTION

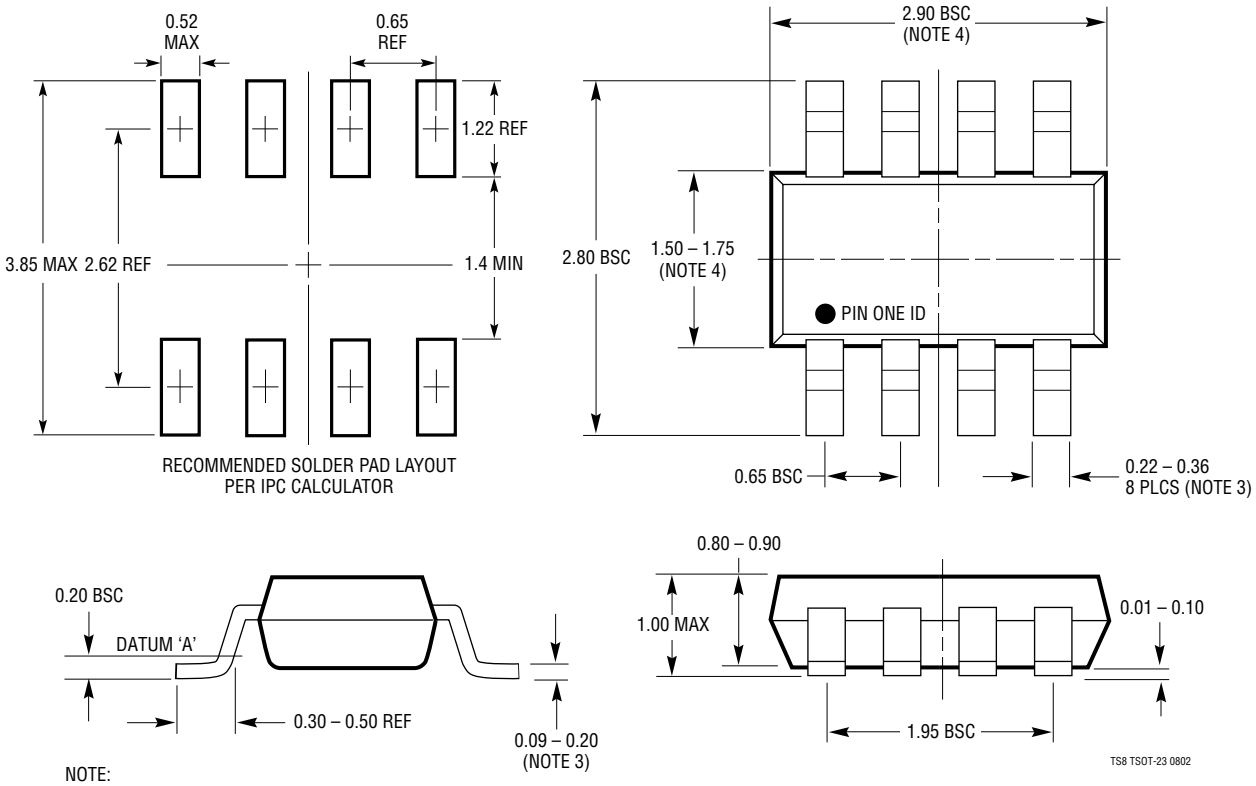
DC Package
8-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1719 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)

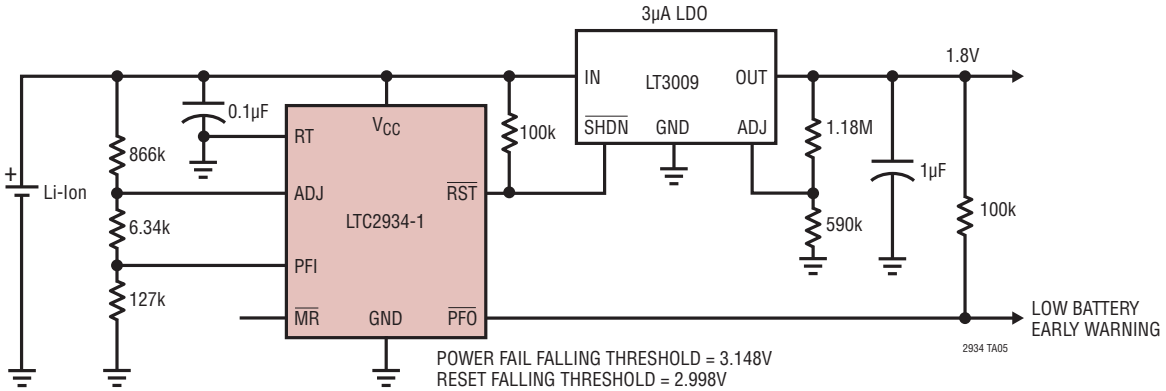


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Portable Device Battery Monitor



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Pushbutton Reset	4.37V/4.62V Threshold
LTC1326	Micropower Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%) and ADJ
LTC1726	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable Reset and Watchdog Timeouts
LTC1727	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1985	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable Reset, 10-Lead MSOP and DFN Packages
LTC2901	Programmable Quad Supply Monitor	Adjustable Reset and Watchdog Timer
LTC2902	Programmable Quad Supply Monitor	Adjustable Reset and Tolerance
LTC2903	Precision Quad Supply Monitor	6-Lead SOT-23 Package
LTC2904/LTC2905/ LTC2906/LTC2907	Three-State Programmable Precision Dual Supply Monitor	8-Lead SOT-23 and DFN Packages
LTC2908	Precision Six-Supply Monitor (Four Fixed and Two Adjustable)	8-Lead TSOT-23 and DFN Packages
LTC2909	Precision Triple/Dual Input UV, OV and Negative Voltage Monitor	Shunt Regulated V_{CC} Pin, Adjustable Threshold and Reset, 8-Lead SOT-23 and DFN Packages
LTC2910	Octal Positive/Negative Voltage Monitor	Separate V_{CC} Pin, Eight Inputs, Up to Two Negative Monitors Adjustable Reset Timer, 16-Lead SSOP and DFN Packages
LTC2912/LTC2913/ LTC2914	Single/Dual/Quad UV and OV Voltage Monitors	Separate V_{CC} Pin, Adjustable Reset Timer
LTC2915/LTC2916/ LTC2917/LTC2918	Single Voltage Supervisors with 27 Pin-Selectable Thresholds	Manual Reset and Watchdog Functions, 8- and 10-Lead TSOT-23, MSOP and DFN Packages
LTC2935	Ultralow Power Supervisor with Eight Pin-Selectable Thresholds	500nA Quiescent Current, 2mm × 2mm 8-Lead DFN and TSOT-23 Packages

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