ES_LPC407x/8x

Errata sheet LPC407x/8x

Rev. 1 — 24 September 2012 **Errata sheet**

Document information

Info	Content
Keywords	LPC407x, LPC408x, errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
1	20120924	• Initial version

Contact information

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1. Product identification

The LPC407x/8x devices typically have the following top-side marking:

LPC40xxXXX

xxxxxxx

xxYYWWR[x]

The last digit in the last line (field 'R') will identify the device revision. Note: pre-production parts are marked differently and this system does not apply. This Errata Sheet covers the following revisions of the LPC407x/8x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.	'-'	Section 5.1

3. Functional problems detail

n/a

4. AC/DC deviations detail

n/a

5. Errata notes

5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the V_{DD} level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.

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